Data Sheet

1.0625 Gbit/sec Fibre Channel Transmitter/Receiver Chipset

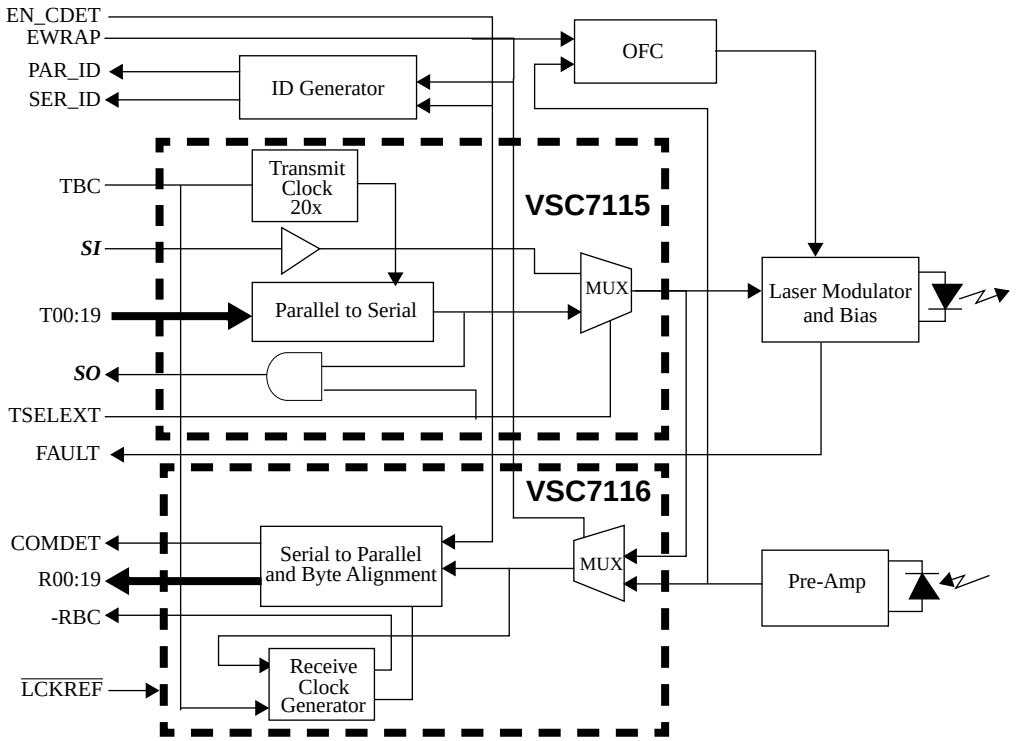
Features

- ANSI X3T11 Fibre Channel Compatible at 1.0625 Gbps
- Compliant With FCSI Gigabaud Link Module Specification
- On-chip Clock Multiplication Relieves System of High Speed Clock Generation
- 20 Bit TTL Compatible Parallel Interface
- Serial I/O Function on VSC7115 Transmitter for Class 1 Fibre Channel Switch
- High Sensitivity Differential Receiver Suitable For Both Coaxial And Optical Link Applications
- Single +3.3V Supply Operation

General Description

The VSC7115/VSC7116 chipset is compatible with the ANSI X3T11 Fibre Channel Standard and the FCSI Gigabaud Link Module specification (FCSI-301-Rev 1.0). It is ideal for building cost effective, very high speed point-to-point communications links. The chipset is designed for 1.0625 Gb/s operation. The VSC7115 accepts 8B/10B encoded TTL input data. Two parallel 10B characters are clocked into the device at 1/20 of the desired baud rate and are serialized for transmission. The VSC7116 accepts differential high speed serial inputs, extracts the clock and retimes the data from the input serial bit stream. The VSC7116 then outputs 20 bit TTL level parallel data.

Gigabaud Link Module Block Diagram



VSC7115 Transmitter Functional Description

The VSC7115 is an ANSI X3T11 (FC-PH) compatible Fibre Channel (FC) transmitter designed to work at the FC baud rate of 1.0625 Gb/s. The VSC7115 accepts 8B/10B encoded TTL input data as two parallel 10-bit characters clocked into the device at 1/20 of the desired baud rate. The VSC7115 has an on-chip PLL clock multiplier that uses the 53.125 MHz Transmit Byte Clock (TBC) to generate a 1.0625 GHz bit clock. This PLL requires no external components. Two high speed outputs are provided to facilitate loopback testing and an additional serial bypass path is provided as well. The serial bypass path is intended for use in Class I Fibre Channel switches. See Figure #1 for a block diagram of the VSC7115.

Parallel data is latched into the transmitter on the rising edge of TBC. The internally generated 53.125 MHz byte clock is the select line on a 20 to 10 bit mux which selects one of T00:09 or T10:19 to load into the 10 bit serial shift register. The shift register is clocked out to the serial outputs by the bit clock which is 20x the TBC input frequency with T00 clocked out first.

Output Enable controls are provided for each of the serial output ports. OE0 controls the primary outputs, TX+ and TX-, while OE1 controls the secondary outputs, TLX+ and TLX-. When an OE control is brought HIGH, it enables the differential output to transmit serial data. When an OE control is brought LOW, the respective output is forced to a logical HIGH state. A logical HIGH on the differential outputs will cause TX- to be LOW and TX+ to be HIGH. The secondary outputs can be used as a local loopback for system testing.

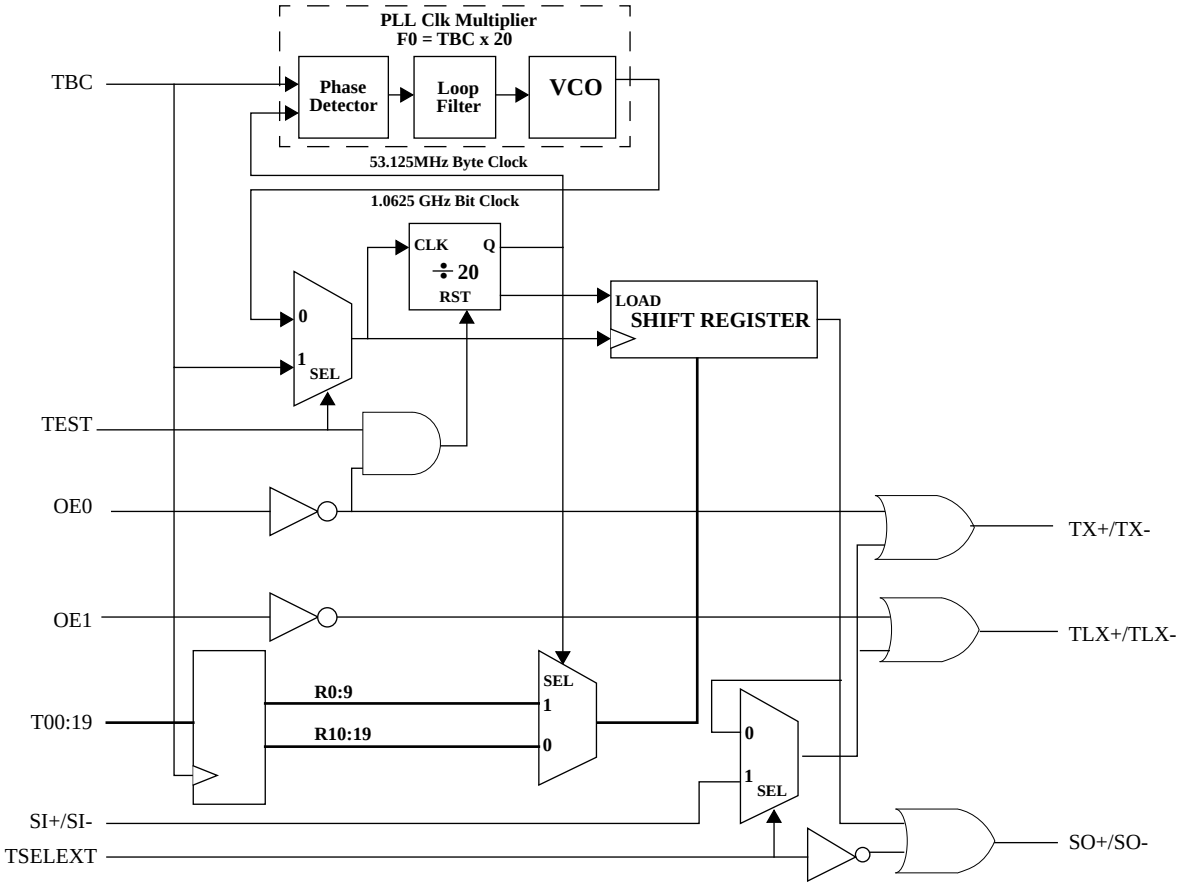
The VSC7115 controls the serial input (SI) and serial output (SO) functions defined in the Gigabaud Link Module specification through the TSELEXT signal. When TSELEXT is HIGH, data from the differential serial input, SI, is routed to the primary and loopback serial data outputs TX and TLX respectively and serialized 20-bit parallel data is routed onto the serial output SO+/SO-. When TSELEXT is LOW, the serialized 20-bit data is routed to the TX and TLX outputs and the differential SO output is set to a logical HIGH state. Shown in Table 1 are how the VSC7115 outputs are effected by TSELEXT and OE.

A TEST input is provided which replaces the PLL generated bit clock by TBC to facilitate functional testing when asserted HIGH. For normal operation, this input should be pulled LOW.

Table 15: Output Control

VSC7115 INPUTS			*VSC7115 OUTPUTS*		
TSELEXT	***OE1***	***OE0***	***SO***	***TLX***	***TX***
0	0	0	HIGH	HIGH	HIGH
0	0	1	HIGH	HIGH	T00:19
0	1	0	HIGH	T00:19	HIGH
0	1	1	HIGH	T00:19	T00:19
1	0	0	T00:19	HIGH	HIGH
1	0	1	T00:19	HIGH	SI
1	1	0	T00:19	SI	HIGH
1	1	1	T00:19	SI	SI

Figure 15: VSC7115 Transmitter Block Diagram

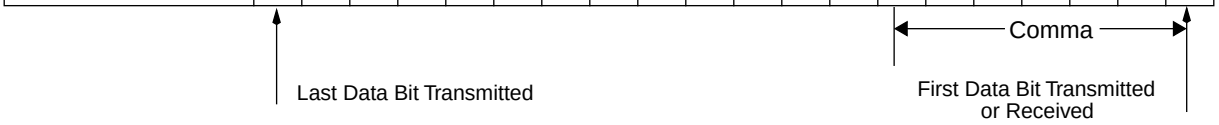


Transmission Character Interface

In Fibre Channel, an encoded byte is 10 bits and is referred to as a transmission character. A Fibre Channel word is 32 bits which is encoded into a transmission word of 40 bits. The 20 bit interface on the VSC7115 corresponds to a half transmission word. The bit ordering and its relationship to Fibre Channel bit position is shown in Figure for the VSC7115.

Figure 16: Transmission Order and Mapping to Fibre Channel Character

Parallel Data Bits	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
8B/10B Bit Position	j	h	g	f	i	e	d	c	b	a	j	h	g	f	i	e	d	c	b	a
Valid Comma Position											0	1	0	1	1	1	1	1	0	0



VSC7116 Receiver Functional Description

The VSC7116 is an ANSI compatible Fibre Channel (FC) receiver designed to work at the FC baud rate of 1.0625 Gb/s. This device is compliant with ANSI X3T11 Fibre Channel Physical Layer (FC-PH, Rev 4.4) receiver specifications. The VSC7116 accepts differential high speed serial inputs, extracts the clock and retimes the data from the input serial bit stream. The VSC7116 has internal PLL-based clock recovery circuitry which requires no external components. The serial input stream is the result of the serialization of 8B/10B encoded data by a FC compatible transmitter or any other source which produces a data stream with a transition density of 40% or greater and has a maximum run length less than 6 bit times. The retimed serial bit stream is converted into a 20 bit parallel output word. Figure 17 shows a block diagram of the VSC7116.

Serial data is received on the RX, RLX differential pairs. The PLL clock recovery circuit will lock to the serial data stream if the clock to be recovered is within 1.0% of the internally generated bit rate clock. The recovered byte clock, -RBC, is used to retime the input data stream. The 20 bit wide TTL data output (R00:19) is staggered by 5 bit times to reduce noise caused by simultaneously switching outputs. Refer to Figure 18 for the timing waveform. Staggering the 5 bit time reduces the output noise and meets the GLM receive data valid times.

Word synchronization is enabled in the VSC7116 by tying the EN_CDET pin HIGH or to V_{DD}. When synchronization is enabled, the VSC7116 constantly examines the serial data for the presence of the Fibre Channel negative beginning disparity “Comma” pattern. This pattern is “0011111”. The comma pattern is not a normal data character, but the first seven bits of special characters defined specifically for synchronization or testing by Fibre Channel. Improper alignment is defined as any of the following conditions:

1) The comma sequence is not properly aligned within a the 10-bit transmission character such that R00...R06 does not equal “0011111.”
2) The comma sequence straddles the boundary between two 10 bit transmission characters.

When the parallel data alignment changes in response to a comma pattern, some data which would have been presented on the parallel output port will be lost. The detection of the comma is pipelined. Depending on the required new output phase, the sync character itself may be destroyed by the synchronization operation. Nonetheless, data following the sync character will be correctly aligned. Thus if downstream logic requires detection of the sync character (for example, to accomplish ordered set alignment) then more than one sync character must be transmitted in order to guarantee that one will be forwarded out of the VSC7116 uncorrupted. Fibre Channel compliant systems require the receipt of a minimum of three ordered sets called IDLE’s for word

synchronization. Ordered sets are special Fibre Channel transmission words (40-bits) that have the K28.5 sync character as the first character received. The first of these ordered sets will cause resynchronization in the VSC7116. The subsequent two ordered sets will be correctly aligned when they are received. In systems where synchronization is undesired, a LOW on EN_CDET will disable the comma detect function, and the data will be unframed.

On encountering a comma, a pulse is generated on the COM_DET output to signal that realignment of the parallel data field may have occurred. The COM_DET pulse is presented simultaneously with the actual synchronization bit sequence, (which may be corrupted as discussed above,) and has a duration equal to the data. Functional waveforms for synchronization in both modes are given in Figure 18 and Figure 19. Figure 18 shows the case when a comma is detected and no phase adjustment is necessary. It illustrates the position of the COM_DET pulse in relation to the sync character. Figure 19 shows the case where the K28.5 is detected, but out of alignment and a change in -RBC and the output data is required. Note that the VSC7116 always stretches the -RBC so it will never create a clock sliver on resynchronization.

Figure 17: VSC7116 Receiver Block Diagram

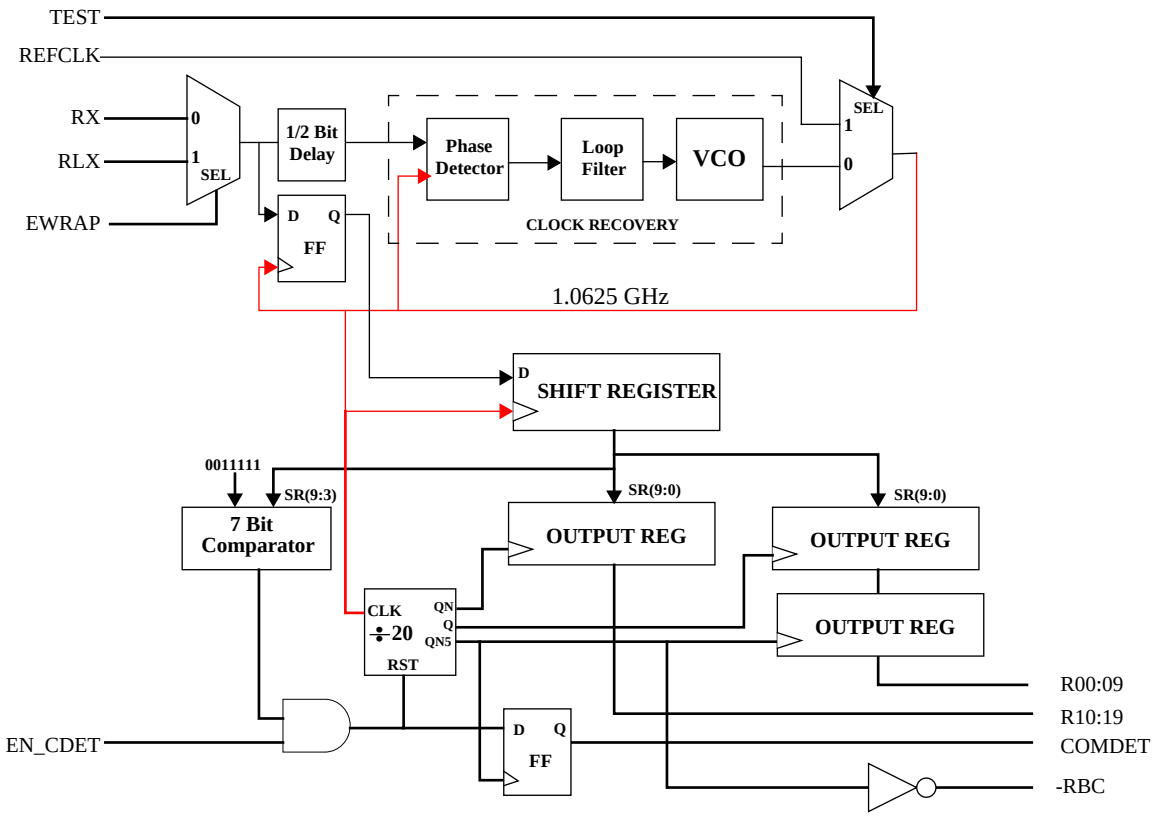


Figure 18: Data and COM_DET Timing While In Sync

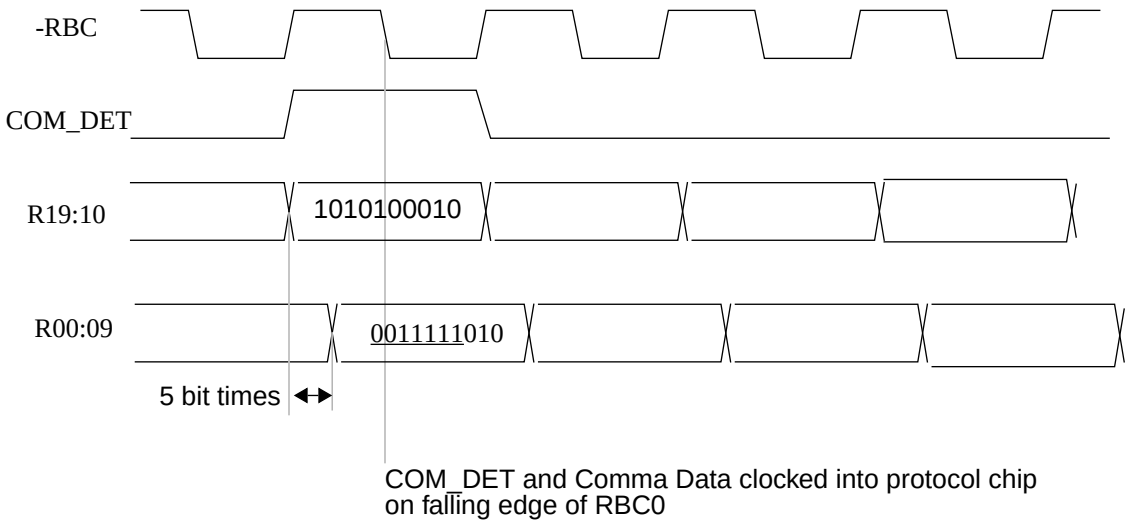
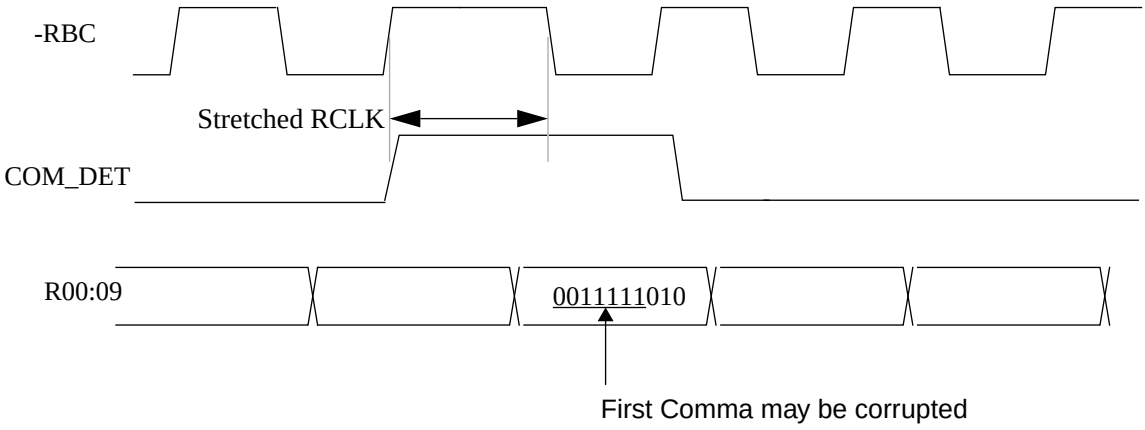


Figure 19: COM_DET and RCLK Timing When Resynchronization



-RBC is stretched and not slivered when resynchronizing

Figure 20: VSC7115 Timing Waveforms

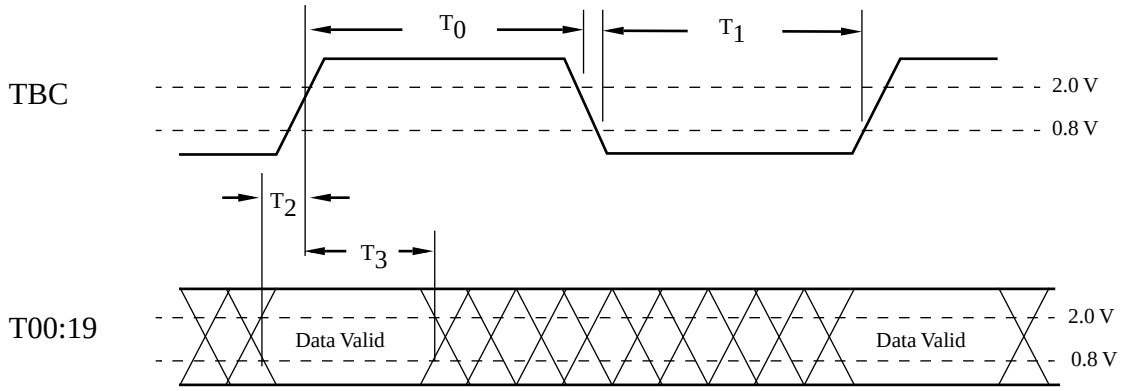
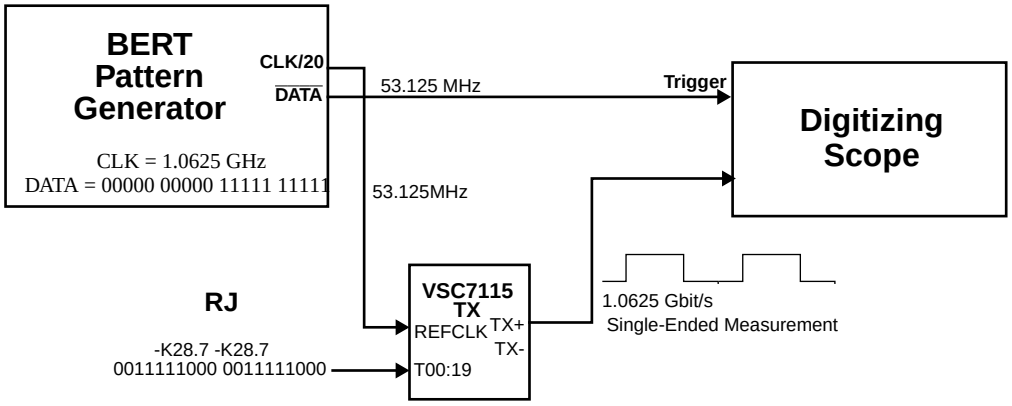


Table 16: VSC7115 AC Characteristics

Parameters	*Description*	*Min*	*Max*	*Unit*	Conditions
T_0	TBC min clock pulsewidth HIGH	6.0	—	ns	Measured 2.0V to 2.0V
T_1	TBC min clock period LOW	6.0	—	ns	Measured 0.8V to 0.8V
T_2	Data setup w.r.t. TBC rising edge	2.0	—	ns	Measured from TBC midpoint to a valid HIGH (2.0V) or valid LOW (0.8V) level.
T_3	Data hold w.r.t. TBC rising edge	3.3	—	ns	Measured from TBC midpoint to a valid HIGH (2.0V) or valid LOW (0.8V) level.
T_{TCR},T_{TCF}	TBC Rise and Fall Time	0.5	3.2	ns	0.6V to 2.2V
T_{SDR},T_{SDF}	TX+/TX-/TLX+/TLX-/SO+/SO- Rise and Fall Time		300	ps	20% to 80%, tested on a sample basis 50Ω load to V_{DD}-2V
T_{TBCJ}	TBC Jitter (Peak to Peak)		TBD	ps	
FT	TBC Frequency Tolerance		$\pm$.01	%	
T_{DC}	TBC Duty Cycle	35	65	%	Refer to GLM Duty Cycle Calculation
Transmitter Output Jitter Allocation					
T_{RJ} (RMS)	Serial data output random jitter (RMS)	—	20	ps	RMS, tested on a sample basis
T_{DJ}	Serial data output deterministic jitter (p-p)	—	100	ps	Peak to peak, tested on a sample basis

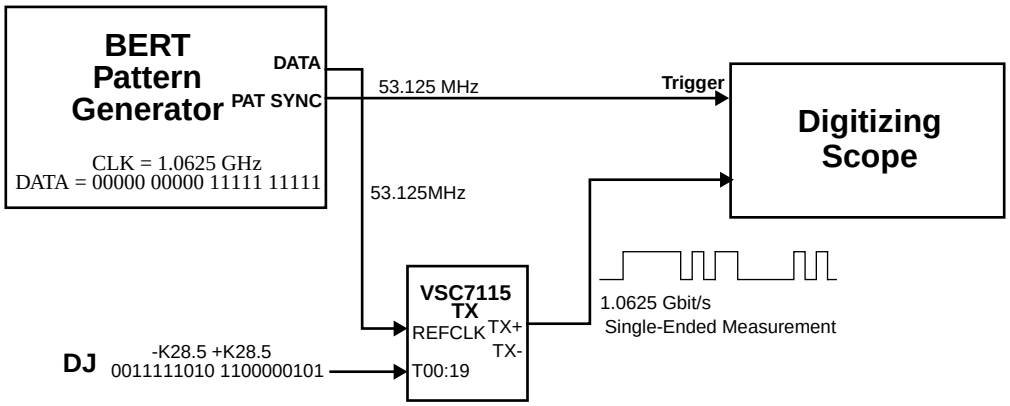
Figure 21: Jitter Measurement Method

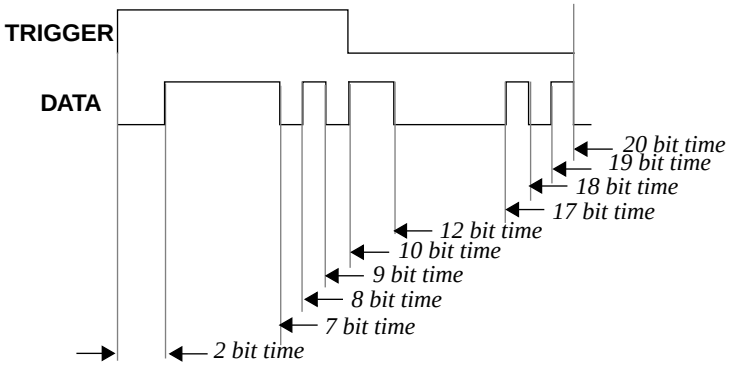
Random Jitter Measurement



Random jitter (RJ) measurements performed according to Fibre Channel 4.1 Annex A, Test Methods, Section A.4.4. Measure standard deviation of all 50% crossing points. Peak to peak RJ is ±

Deterministic Jitter Measurement





Note:
Deterministic jitter (DJ) measurements performed according to Fibre Channel 4.1 Annex A, Test Methods, Section A.4.3. Measure time of all the 50% points of all ten transitions. DJ is the range of the timing variation from expected.

Figure 22: VSC7116 AC Timing Waveforms

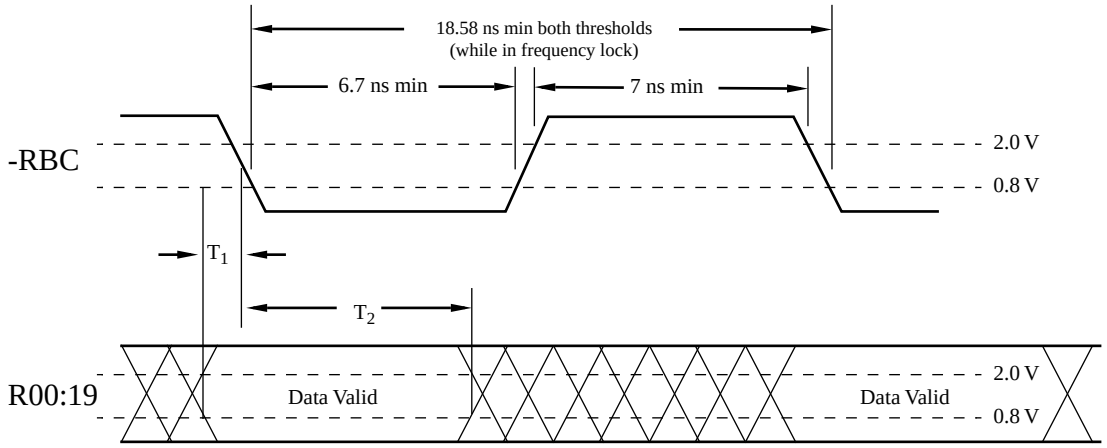


Table 17: VSC7116 AC Characteristics

Parameters	*Description*	*Min*	*Max*	*Unit*	*Conditions*
T_1	Data valid setup prior to -RBC fall	2.5	—	ns	Measured from -RBC midpoint to a valid HIGH (2.0V) or valid LOW (0.8V).
T_2	Data valid hold after -RBC fall	6.0	—	ns	Measured from -RBC midpoint to a valid HIGH(2.0V) or valid LOW (0.8V)
T_{RCR},T_{RCF}	-RBC rise and fall time	0.7	2.4	ns	0.8V to 2.0V, tested on a sample basis, 10pF load
T_{DR},T_{DF}	Data output rise and fall time	—	4.0	ns	0.8V to 2.0V, tested on a sample basis, 10pF load
T_{LOCK}	Data acquisition lock time @ 1.0625Gb/s	—	2.4	µs	8B/10B IDLE pattern, tested on a sample basis
Input Jitter Tolerance	Input data eye opening allocation at receiver input for BER ≤ 1E-12	30%	—	bit time	As specified in Fibre Channel FC-PH standard eye diagram jitter mask.

Absolute Maximum Ratings (1)

Power Supply Voltage, (V_{DD}) ..... 0.5V to +4V
PECL DC Input Voltage, (V_{INP}) ..... -0.5V to V_{DD} +0.5V
TTL DC Input Voltage, (V_{INT}) ..... -0.5V to 6.0V
DC Voltage Applied to Outputs for High Output State, ($V_{IN\ TTL}$) ..... -0.5V to V_{DD} + 0.5V
TTL Output Current (I_{OUT}), (DC, Output High) 50mA
PECL Output Current, (I_{OUT}), (DC, Output High) ..... -50mA
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature, (T_{STG}) ..... -65° to + 150°C
Maximum Input ESD ..... 1500 V

Recommended Operating Conditions(2)

Power Supply Voltage, (V_{DD}) ..... +3.3V $\pm$ 5%
Operating Temperature Range, (T) (3) ..... 0°C to +110°C

Notes:

1) *CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.*
2) *Vitesse guarantees the functional and parametric operation of the part under "Recommended Operating Conditions" except where specifically noted in the AC and DC Parametric Tables.*
3) *Lower limit is ambient temperature and upper limit is case temperature.*

Table 18: VSC7115 DC Characteristics *(Over recommended operating conditions).*

Parameters	*Description*	*Min*	*Typ*	*Max*	*Unit*	*Conditions*
$V_{IH(TTL)}$	Input HIGH voltage (TTL)	2.0	—	5.5	V	$I_{IH} \leq 6.6$ mA @ $V_{IH} = 5.5$ V
$V_{IL(TTL)}$	Input LOW voltage (TTL)	0	—	0.8	V	—
$I_{IH(TTL)}$	Input HIGH current (TTL)	—	—	50	µA	$V_{IN} = 2.4$ V
$I_{IL(TTL)}$	Input LOW current (TTL)	-500	—	-50	µA	$V_{IN} = 0.5$ V
V_{DD}	Supply voltage	3.14	3.3	3.47	V	±5% of $V_{DD} = 3.30$V
I_{DD}	Supply current	—	—	350	mA	Outputs open, $V_{DD} = V_{DD}$ max
P_D	Power dissipation	—	1.0	1.2	W	Outputs open, $V_{DD} = V_{DD}$ max
$\Delta V_{IN(DF)}$	Serial data differential peak to peak input swing SI+/SI-	300		2600	mVpp	AC Coupled Internally biased at $V_{DD}/2$
ΔV_{OUT}	TX+/TX-/TLX+/TLX-/SO+/SO- Single-ended output differential peak to peak voltage swing	1200	—	2200	mVpp	50Ω to $V_{DD} - 2.0$ V

Table 19: VSC7116 DC Characteristics *(Over recommended operating conditions).*

Parameters	*Description*	*Min*	*Typ*	*Max*	*Unit*	*Conditions*
$V_{OH(TTL)}$	Output HIGH voltage (TTL)	2.4	—	—	V	$I_{OH} = -1.2$ mA
$V_{OL(TTL)}$	Output LOW voltage (TTL)	—	—	0.6	V	$I_{OL} = +1.2$ mA
$V_{IH(TTL)}$	Input HIGH voltage (TTL)	2.0	—	5.5	V	$I_{IH} \leq 6.6$ mA @ $V_{IH} = 5.5$ V
$V_{IL(TTL)}$	Input LOW voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH current (TTL)	—	—	50	µA	$V_{IN} = 2.4$ V
I_{IL}	Input LOW current (TTL)	-500	—	-50	µA	$V_{IN} = 0.5$ V
V_{DD}	Supply voltage	3.14	3.3	3.47	V	±5% of $V_{DD} = 3.30$v
I_{DD}	Supply current	—	—	520	mA	Outputs open, $V_{DD} = V_{DD}$ max
P_D	Power dissipation	—	1.6	1.8	W	Outputs open, $V_{DD} = V_{DD}$ max
V_{IB}	Input Bias Voltage for HS Differential Inputs	1.630	1.65	1.670	V	$V_{DD} = 3.30$V, Measure open input voltage
ΔV_{INSI}	Serial data differential peak to peak input (RX/RLX) swing	300	—	3200	mV	AC coupled Internally biased at $V_{DD}/2$

Figure 23: VSC7115 Pin Diagram

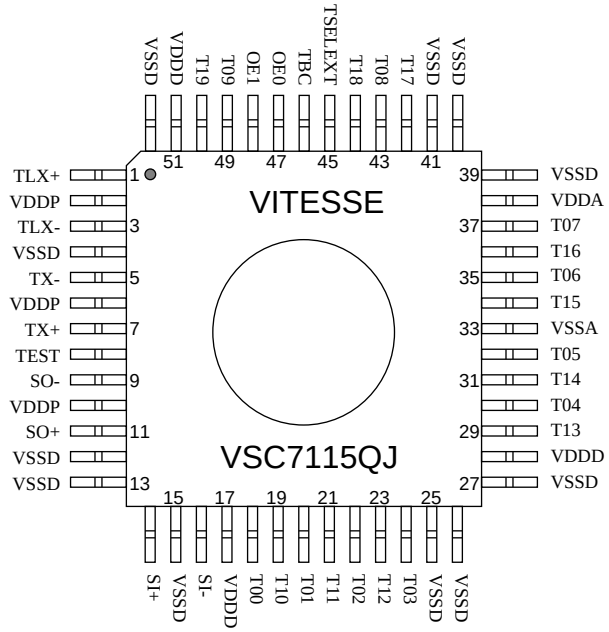
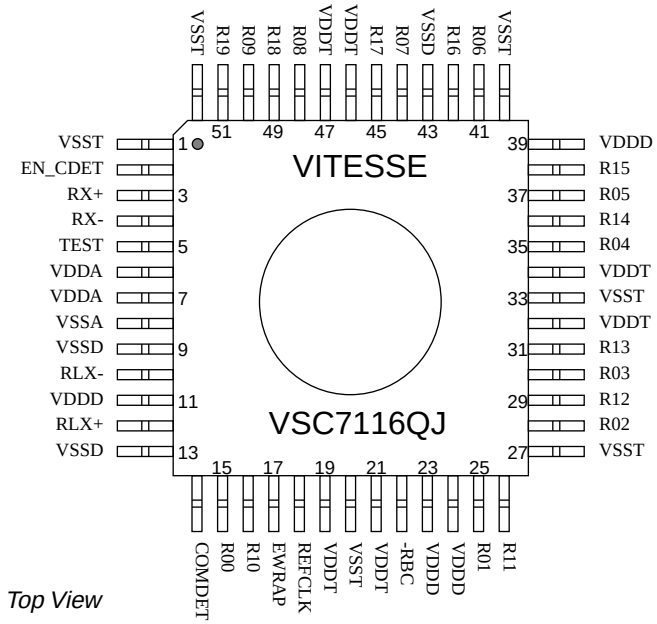


Figure 24: VSC7116 Pin Diagram



Top View

Table 20: VSC7115 Pin Description

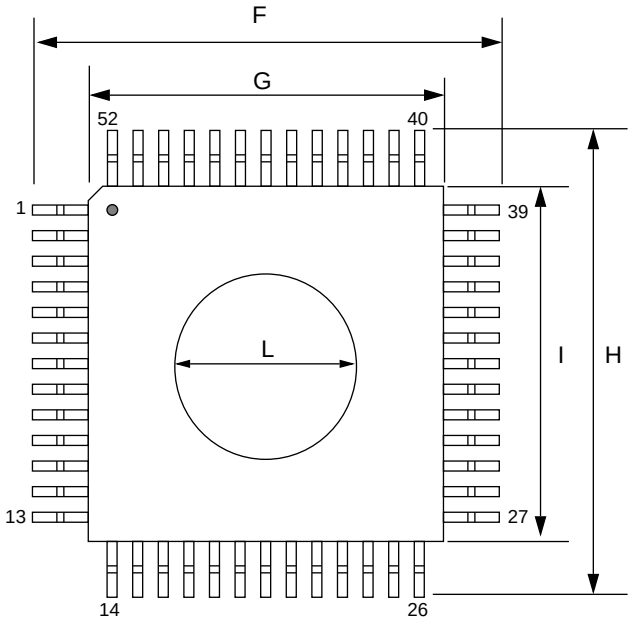
Pin #	*Name*	*Description*
18, 20, 22, 24, 30, 32, 35, 37, 43, 49, 19, 21, 23, 29, 31, 34, 36, 42, 44, 50	T00:19	INPUT - TTL Parallel data on the T00:19 bus is clocked in on the rising edge of TBC. Bit T00 corresponding to 8b/10b bit a for the first character is transmitted first.
45	TSELEXT	INPUT - TTL Transmit SELEct EXTernal control. When HIGH, data from the serial inputs SI+, SI- is multiplexed onto the primary outputs TX and TLX, and serialized data from T00:19 is gated onto SO+, SO-. When LOW, SO+ is driven HIGH and SO- is driven LOW, and TX and TLX transmit the serialized data.
8	TEST	INPUT - TTL When HIGH, this pin puts the transmitter in test mode for factory testing. In this mode, TBC is used to serialize 20 bit input data, and the internal PLL/VCO are bypassed. In normal mode this test pin is low.
11, 9	SO+, SO-	OUTPUTS - Differential (PECL Levels Referenced to 3.3V) High speed serial outputs. When TSELEXT is high, these pins carry the serialized T00:19 data. When TSELEXT is low, these pins are gated to a valid high logic level. AC coupling recommended.
14, 16	SI+, SI-	INPUTS - Differential (Biased at VDD/2) High speed serial inputs. When TSELEXT is HIGH, this data is muxed onto the TX and TLX outputs.
47, 48	OE0, OE1	INPUT - TTL Output Enable inputs. When OE0 is high, it enables the primary outputs TX+, TX-. In test mode, when OE0 is low it is mapped to a reset for internal registers. When OE1 is high it enables the loopback outputs of TLX+, TLX-.
46	TBC	TRANSMIT BYTE CLOCK INPUT - TTL Reference Clock for the PLL clock multiplier, nominally at 53.125 MHz. Parallel data on T00:19 is latched in on the rising edge of TBC. The rising edge is also used to phase lock the internal VCO clock.
1, 3	TLX+, TLX-	OUTPUTS - DIFFERENTIAL (Biased at VDD-1.32V) Transmitter loop back outputs, enabled when OE1 is high, otherwise driven to a valid high logic level. Logic high is TLX+ = high and TLX- = low. AC coupled is required when tying TX to TLX.
7, 5	TX+, TX-	OUTPUTS - DIFFERENTIAL (Biased at VDD-1.32V) Primary transmitter outputs. These outputs carry the serialized data in the normal mode of operation. Enabled when OE0 is high. When OE0 is low, TX+ and TX- are disabled and driven to a valid high logic level. Logic high is TX+ = high and TX- = low. When TSELEXT is high, these outputs carry serial data from the SO+, SO- lines. AC coupling recommended.
17, 28, 51	VDDD	Digital Power Supply
4, 12, 13, 15, 25, 26, 27, 39, 40, 41, 52	VSSD	Digital Ground
2, 6, 10	VDDP	PECL Power Supply
38	VDDA	Analog Power Supply
33	VSSA	Analog Ground

Table 21: VSC7116 Pin Description

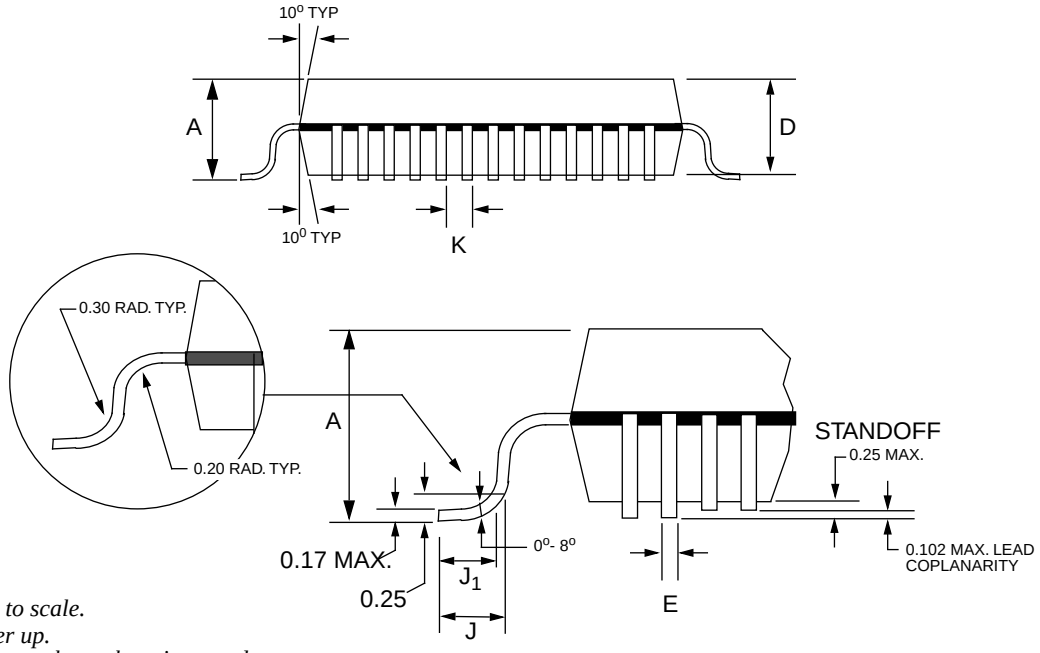
Pin #	*Name*	*Description*
15, 25, 28, 30, 35, 37, 41, 44, 48, 50, 16, 26, 29, 31, 36, 38, 42, 45, 49, 51	R00:19	OUTPUTS - TTL R0 is the first bit received on the serial data stream. The data bus R00:19 meets a setup and hold time specification with respect to the falling edge of the recovered clock -RBC. To minimize bounce due to SSO noise, bits R00:09 are clocked out 5 bit periods earlier than bits R10:19.
18	REFCLK	INPUT - TTL REFerence ClocK for the PLL clock multiplier, nominally at 53.125 MHz. The PLL will lock if the incoming serial baud rate is ±1.0% of 20X the REFCLK. For GLM applications this input will be tied to the system supplied TBC.
17	EWRAP	INPUT - TTL Loopback Enable, Electrical WRAP enable. When HIGH this pin selects the loopback serial inputs RLX for serial to parallel conversion. When low, the RX inputs are selected.
22	-RBC	OUTPUT - TTL Recovered byte clock, nominally at 53 MHz, supplied to strobe the parallel output data. On recognizing a +comma sync character in the serial data stream, -RBC is stretched, if necessary, to re-sync, and outputs the sync character on bits R00:06. The recovered clock is always extended, never truncated when resynchronization occurs
14	COMDET	OUTPUT - TTL Upon detection of a positive comma (0011111) this output goes high for one -RBC period if EN_CDET is HIGH. This output meets the same setup and hold time specified for the R00:19 parallel data outputs with respect to the falling edge of -RBC.
12, 10	RLX+, RLX-	INPUT - DIFFERENTIAL (Biased at VDD/2) Serial loopback data inputs. AC coupling recommended
3, 4	RX+, RX-	INPUT - DIFFERENTIAL (Biased at VDD/2) Received serial data inputs, AC coupling recommended.
2	EN_CDET	INPUT - TTL ENable Comma DETect. When pulled high, enables word synchronization. Word synchronization occurs when the VSC7116 detects a positive comma (0011111) in the serial data stream. In systems where the word synchronization is undesired, a low on the EN_CDET input disables the synchronization function and the data will be “un-framed”.
5	TEST	INPUT - TTL When high, this pin puts the 7116 in test mode. REFCLK replaces the internal bitclk for factory testing. Normally LOW.
11, 23, 24, 39	VDDD	Digital Power Supply
9, 13, 43	VSSD	Digital Ground
19, 21, 32, 34, 46, 47	VDDT	TTL Power Supply
1, 20, 27,33, 40, 52	VSST	TTL Ground
6, 7	VDDA	Analog Power Supply
8	VSSA	Analog Ground

Package Information

52 Pin PQFP Package Drawings



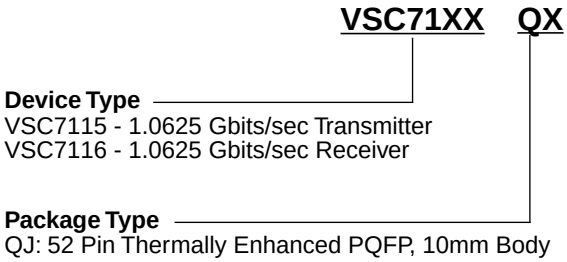
Item	*mm*	*Tol.*
A	2.45	MAX
D	2.00	+0.10/-.05
E	0.30	±.05
F	13.20	±.25
G	10.00	±.10
H	13.20	±.25
I	10.00	±.10
J	0.88	+.15 / -.10
K	0.65	BASIC
L	3.56	±.50 DIA.



NOTES:
Drawing not to scale.
Heat spreader up.
All units in mm unless otherwise noted.
Heat spreader is connected to V_{SS}.

Ordering Information

The order number for this product is formed by a combination of the device number and package type.



Notice

Vitesse Semiconductor Corporation reserves the right to make changes in its products specifications or other information at any time without prior notice. Therefore, the reader is cautioned to confirm that this datasheet is current prior to placing any orders. The company assumes no responsibility for any circuitry described other than circuitry entirely embodied in a Vitesse product.

Warning

Vitesse Semiconductor Corporation's product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without the written consent is prohibited.