CMOS 4-Bit Microcontroller

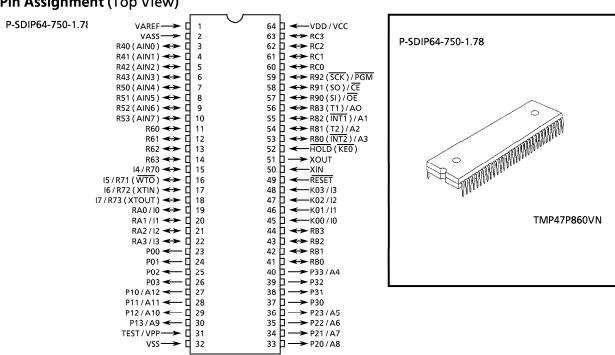
TMP47P860VN TMP47P860VF

The TMP47P860V is the system evaluation LSI of TMP47C660A/860A with 64 Kbits one-time PROM. The TMP47P860V programs / verifies using an adapter socket to connect with PROM programmer, as it is in TMM2764AD.

In addition, the TMP47P860V and the TMP47C660A/860A are pin compatible. The TMP47P860V operates as the same as the TMP47C660A/860A by programming to the internal PROM.

Part No.	ROM	RAM	Package	Adapter Socket
TMP47P860VN	ОТР	512 × 4-bit	P-SDIP64-750-1.78	BM1130
TMP47P860VF			P-QFP64-1420-1.00A	BM1132

Pin Assignment (Top View)



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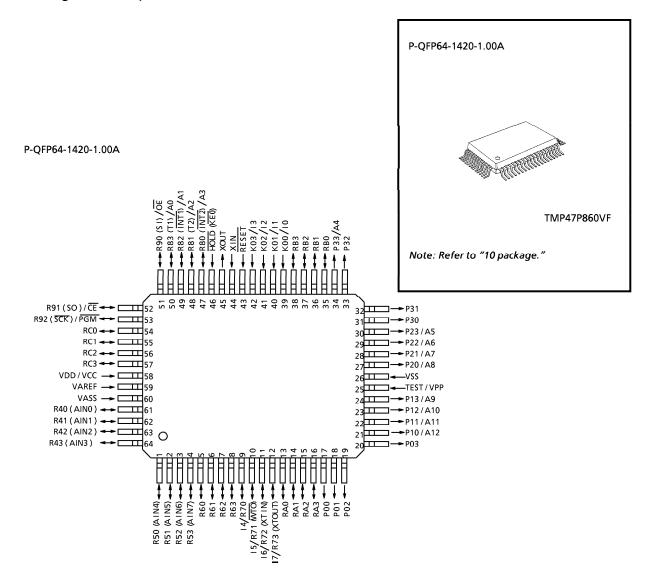
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Pin Assignment (Top View)



Pin Function

The TMP47P860V has MCU mode and PROM mode.

(1) MCU mode

The TMP47C660A/860A and the TMP47P860V are pin compatible (TEST pin for out-going test. Be fixed to low level.).

(2) PROM mode

Pin Name	Input / Output	Functions	Pin Name (MCU mode)					
A12 to A9			P10 to P13					
A8 to A5	INPUT	Address inputs	P20 to P23					
A4	1141 01	Address in parts	P33					
A3 to A0			R80 to R83					
17 to 14	I/O	Data outputs (Inputs)	R73 to R70					
13 to 10	"0	Data outputs (inputs)	K03 to K00					
PGM		Program control input	R92					
CE	Input	Chip Enable input	R91					
ŌĒ		Output Enable input	R90					
VPP		+ 21 V / 5 V (Program supply voltage)	TEST					
vcc	Power supply	+5V	VDD					
VSS		0 V	VSS					
P03 to P00	atat							
P32 to P30	output	Open						
RA3 to RA0								
RB3 to RB0								
RC3 to RC0	I/O							
R43 to R40	1/0	Be fixed to Low Level						
R53 to R50								
R63 to R60								
RESET	Input	PROM mode setting pin. Be fixed to low level.						
HOLD	Input	The straining plant be threat to low level.						
XIN	Input	Resonator connecting pin						
хоит	output	nesonator connecting pin						
VAREF VASS	Power supply	Be fixed to low level						

Operational Description

The following is an explanation of hardware configuration and operation in relation to the TMP47P860V. The TMP47P860V is the same as the TMP47C660A/860A except that an OTP is used instead of a built-in mask ROM.

1. Operation mode

The TMP47P860V has an MCU mode and a PROM mode.

1.1 MCU mode

The MCU mode is set by fixing the TEST/VPP pin at the "L" level. Operation in the MCU mode is the same as for the TMP47C660A/860A, except that the TEST / VPP pin does not have built in pull-down resistor and cannot be used open.

1.1.1 Program memory

The program storage area is the same as for the TMP47C860A. Data conversion tables must be set in two locations when using the TMP47P860V to check TMP47C660A operation.

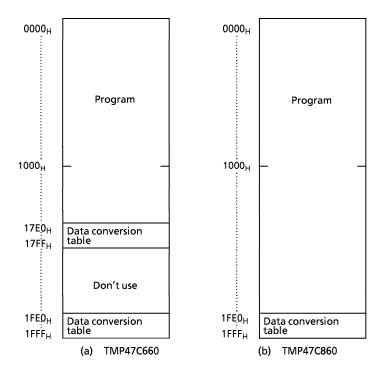


Figure 1-1. Program area

1.1.2 Data memory

The TMP47P860V has two built-in 256 x 4-bit data memory banks (Bank0, Bank1).

When using the TMP47P860V as a TMP47C660A evaluator, do not write data to address $80_{\rm H}$ and following, even though the Bank1 addresses are 00, to FF_H. There is no necessity to take into consideration a special common function area because one is built in Bank0.

Electrical Characteristics

Absolute Maximum Ratings $(V_{SS} = 0 V)$

Parameter	Symbol	Pins	Ratings	Unit	
Supply Voltage	V_{DD}		– 0.3 to 6.5	V	
Program Voltage	V_{PP}	TEST / VPP pin	– 0.3 to 13.0	٧	
Input Voltage	V_{IN}		– 0.3 to V _{DD} + 0.3	٧	
Outrot Valtage	V _{OUT1}	Ports R4, R5, R7, push-pull	-0.3 to $V_{DD} + 0.3$	V	
Output Voltage	V _{OUT2}	Ports P1, P2, R6, R8, R9	– 0.3 to V _{DD} + 0.3	V	
Output (Per 1 pin)	I _{OUT1}	Port R	3.2		
	I _{OUT2}	Ports P1, P2	30	mA	
	I _{OUT3}	Ports P0, P3	15		
Output Correct (Total)	Σ I _{OUT1}	Ports P0, P1	120		
Output Current (Total)	Σ I _{OUT2}	Ports P2, P3	120	mA	
Power Dissipation [Topr = 70°C)	PD		600	mW	
Soldering Temperature (time)	Tsld		260 (10 s)	°C	
Storage Temperature	Tstg		– 55 to 125	°C	
Operating Temperature	Topr		– 40 to 70	°C	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant.

Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Opeating Conditions

$$(V_{SS} = 0 \text{ V}, \text{ Topr} = -40 \text{ to } 70^{\circ}\text{C})$$

Parameter	Symbol	Pins	Conditions	Min	Max	Unit
			fc = 6.0 MHz	4.5		
Cumplu Valtage	.,		fc = 4.2 MHz	2.7		_v
Supply Voltage	V_{DD}		In the SLOW mode	7 2.7	5.5	'
			In the HOLD mode	2.0		
	V_{IH1}	Except Hysteresis Input	resis Input			
Input High Voltage	V_{IH2}	Hysteresis Input	$V_{DD} \ge 4.5 V$	V _{DD×} 0.75	V_{DD}	V
	V _{IH3}		V_{DD} < 4.5 V	$V_{DD} \times 0.9$		
	V _{IL1}	Except Hysteresis Input	$V_{DD} \ge 4.5 V$		$V_{DD} \times 0.3$	
Input Low Voltage	V_{IL2}	Hysteresis Input	V _{DD} ≦ 4.5 V	0	$V_{DD} \times 0.25$	V
V _{IL3}			V_{DD} < 4.5 V		$V_{DD} \times 0.1$	
Clash Fasanian an	fc		High-freq.clock	0.4	6.0	MHz
Clock Frequency	fs		Low-freq.clock	30	34	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Input voltage V_{IH3} , V_{IL3} : In the SLOW or HOLD mode.

DC Characteristics

 $(V_{SS} = 0 \text{ V, Topr} = -40 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Pins	Conditions	Min	Тур.	Max	Unit
Hysteresis Voltage	V _{HS}	Hysteresis input		_	0.7	_	٧
	I _{IN1}	Port K0, TEST, RESET, HOLD	V _{DD} = 5.5 V				
Input Current	I _{IN2}	Ports R (open-drain)	V _{IN} = 5.5 V / 0 V	_	_	± 2	μΑ
Input Resistance	R _{IN2}	RESET		100	220	450	kΩ
Low Level Input Current	I _{IL}	Ports R (push-pull)	$V_{DD} = 5.5 \text{ V}, \ V_{IN} = 0.4 \text{ V}$	_	_	- 2	mA
Output Leakage Current	I _{LO}	Ports R (open drain)	V _{DD} = 5.5 V, V _{OUT} = 5.5 V	_	_	2	μA
Output Level High Voltage	V _{OH}	Push-pull ports	$V_{DD} = 4.5 \text{ V}, \ I_{OH} = -200 \ \mu\text{A}$	2.4	_	_	>
Output Level Low Voltage	V _{OL}	Except XOUT, P ports	V _{DD} = 4.5 V, I _{OL} = 1.6 mA	_	_	0.4	
Low Level Output Current	I _{OL2}	Ports P1, P2	$V_{DD} = 4.5 \text{ V}, V_{OI} = 1.0 \text{ V}$	_	20	_	mA
Low Level Output Current	I _{OL3}	Ports P0, P3	V _{DD} = 4.5 V, V _{OL} = 1.0 V	_	7	_	IIIA
Supply Current (in the Nomal mode)	I _{DD}		V _{DD} = 5.5 V fc = 4 MHz	_	3	6	mA
Supply Current (in the SLOW mode)	I _{DDS}		V _{DD} = 5.0 V fs = 32.768 kHz	_	30	60	mA
Supply Current (in the HOLD mode)	I _{DDH}		V _{DD} = 5.5 V	_	0.5	10	μΑ

Note 1: Typ. values show those at Topr = 25° C, VDD = 5 V.

Note 2: Input Current IIN1; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3: IDD, IDDH; VIN = 5.3 V / 0.2 V

The KO port is opened when the input resistor is contained. The voltage applied to the R port is within the valid range.

IDDS; VIN = 2.8 V / 0.2 V, low frequency clock is only oscillated (connecting XTIN, XTOUT).

AD Conversion Characterristics

 $(Topr = -40 \text{ to } 70^{\circ}C)$

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
Analog Reference	V _{AREF}		V _{DD} – 1.5	-	V _{DD}	,,
	V _{ASS}		V _{SS}	_	1.5	V
Analog Reference Voltage Range	ΔV_{AREF}	V _{AREF} – V _{ASS}	2.5	_	_	V
Analog input Voltage	V _{AIN}		V _{ASS}	_	V _{AREF}	V
Analog Supply Current	I _{REF}		_	0.5	1.0	mA
Nonlinearity Error		V - F0V V - 00V	_	_	± 1	
Zero pornt Error		$V_{DD} = 5.0 \text{ V}, V_{SS} = 0.0 \text{ V}$	_	_	± 1	LSB
Full scale Error		V _{AREF} = 5.000 V	_	_	± 1	
Totar Error		V _{ASS} = 0.000 V	-	_	± 2	1

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AC Characteristics

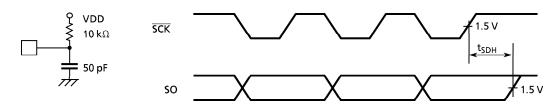
 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 6.0 \text{ V}, Topr = -40 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Instruction Cycle Time	tcy	in the Normal mode	1.3	-	20	
instruction cycle rime	icy	in the SLOW mode	235	_	267	μS
High level Clock Pulse Width	t _{WCH}	For external clock operation	80	_	_	ns
Low level Clock Pulse Width	t _{WCL}	To external clock operation	00			113
AD Conversion Sampling Time	t _{AIN}	fc = 4 MHz	_	2	_	μS
Shift Data Hold Time	t _{SDH}		0.5 tcy – 0.3	_	-	μS

Note: Shift data Hold Time:

External circuit for SCK pin and SO pin

Serial port (completion of transmission)



Recommended Oscillating Conditions

 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, \text{ Topr } = -40 \text{ to } 70^{\circ}\text{C})$

Recommended oscillating conditions of the TMP47P860V are equal to the TMP47C860A's.

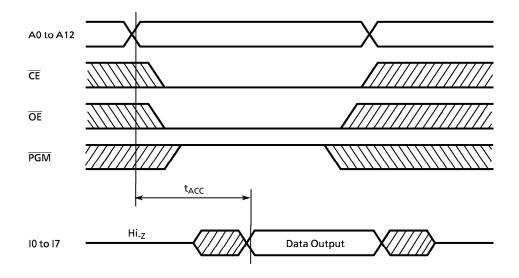
DC/AC Characteristics

 $(V_{SS} = 0 V)$

(1) Read operation

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Output Level High Voltage	V _{IH4}		V _{CC} × 0.7	_	V _{CC}	V
Output Level Low Voltage	V _{IL4}		0	_	V _{CC} × 0.1	V
Supply Voltage	V _{CC}		4.75		6.0	V
Programming Voltage	V_{PP}		4.73	_	6.0	v
Address Access Time	t _{ACC}	V _{CC} = 5.0 ± 0.25 V	0	-	350	ns

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(2) High speed programming operation

Parameter	Sybol	Condition	Min	Тур.	Max	Unit
Input High Voltage	V _{IH4}		V _{CC} × 0.7	-	V _{CC}	V
Input Low Voltage	V _{IL4}		0	_	V _{CC} × 0.12	V
Supply Voltage	V _{CC}		4.75	-	6.0	V
V _{PP} Power Supply Voltage	V _{PP}		12.25	12.50	12.75	V
Programming Pulse Width	t _{PW}	V _{CC} = 6.0 ± 0.25 V	0.95	1.0	1.05	ms

