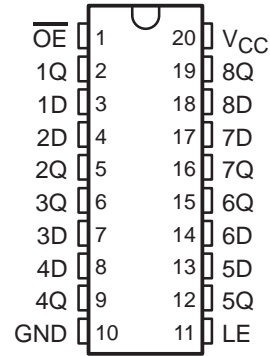


SN54BCT373, SN74BCT373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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- State-of-the-Art BiCMOS Design Significantly Reduces Standby Current
- Full Parallel Access for Loading
- 3-State True Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds 2000 V Per MIL-Std-883C, Method 3015
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic and Ceramic 300-mil DIPs (J, N)

SN54BCT373 . . . J OR W PACKAGE
SN74BCT373 . . . DB, DW, OR N PACKAGE
(TOP VIEW)



description

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'BCT373 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs will follow the data (D) inputs. When the latch enable is taken low, the Q outputs will be latched at the logic levels that were set up at the D inputs.

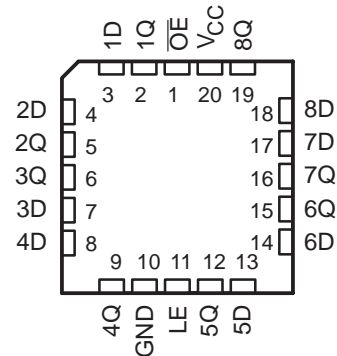
A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output enable (\overline{OE}) does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74BCT373 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54BCT373 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74BCT373 is characterized for operation from 0°C to 70°C .

SN54BCT373 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each latch)

| INPUTS | | | OUTPUT Q |
|-----------------|----|---|-------------|
| \overline{OE} | LE | D | |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q_0 |
| H | X | X | Z |

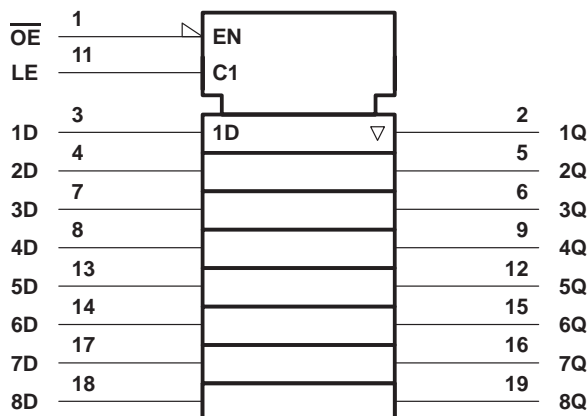
SN54BCT373, SN74BCT373

OCTAL TRANSPARENT D-TYPE LATCHES

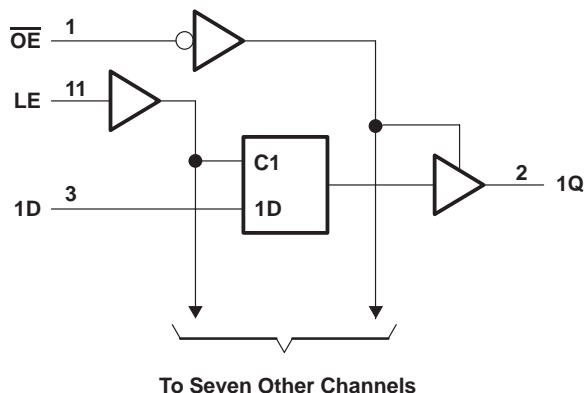
WITH 3-STATE OUTPUTS

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logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|---|---------------------|
| Supply voltage range, V_{CC} | – 0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | – 0.5 V to 7 V |
| Voltage range applied to any output in the disabled or power-off state, V_O | – 0.5 V to 5.5 V |
| Voltage range applied to any output in the high state, V_O | – 0.5 V to V_{CC} |
| Input clamp current | –30 mA |
| Current into any output in the low state: SN54BCT373 | 96 mA |
| SN74BCT373 | 128 mA |
| Power dissipation (DB package only) (see Note 2) | 650 mW |
| Operating free-air temperature range: SN54BCT373 | – 55°C to 125°C |
| SN74BCT373 | 0°C to 70°C |
| Storage temperature range | – 65°C to 150°C |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. Power dissipation is application dependent and is a function of supply voltage, operating temperature, the number of outputs switching simultaneously, and output duty cycle. Because the thermal resistance of the DB package is higher than that of the DW or N packages, the DB package may not be suitable for some applications.

recommended operating conditions

| | | SN54BCT373 | | | SN74BCT373 | | | UNIT |
|----------|--------------------------------|------------|-----|-----|------------|-----|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I_{IK} | Input clamp current | | | –18 | | | –18 | mA |
| I_{OH} | High-level output current | | | –12 | | | –15 | mA |
| I_{OL} | Low-level output current | | | 48 | | | 64 | mA |
| T_A | Operating free-air temperature | –55 | | 125 | 0 | | 70 | °C |



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54BCT373 | | | SN74BCT373 | | | UNIT |
|-------------------|---|--------------------------|------------|------|------|------------|------|------|---------------|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| V_{IK} | $V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$ | | | | -1.2 | | | -1.2 | V |
| V_{OH} | $V_{CC} = 4.5\text{ V}$ | $I_{OH} = -3\text{ mA}$ | 2.4 | 3.3 | | 2.4 | 3.3 | | V |
| | | $I_{OH} = -12\text{ mA}$ | 2 | 3.2 | | | | | |
| | | $I_{OH} = -15\text{ mA}$ | | | | 2 | 3.1 | | |
| V_{OL} | $V_{CC} = 4.5\text{ V}$ | $I_{OL} = 48\text{ mA}$ | | 0.38 | 0.55 | | | | V |
| | | $I_{OL} = 64\text{ mA}$ | | | | | 0.42 | 0.55 | |
| I_I | $V_{CC} = 5.5\text{ V}$, $V_I = 5.5\text{ V}$ | | | | 0.4 | | | 0.4 | mA |
| I_{IH} | $V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$ | | | | 20 | | | 20 | μA |
| I_{IL} | $V_{CC} = 5.5\text{ V}$, $V_I = 0.5\text{ V}$ | | | | -0.6 | | | -0.6 | mA |
| I_{OS}^\ddagger | $V_{CC} = 5.5\text{ V}$, $V_O = 0$ | | -100 | | -225 | -100 | | -225 | mA |
| I_{OZH} | $V_{CC} = 5.5\text{ V}$, $V_O = 2.7\text{ V}$ | | | | 50 | | | 50 | μA |
| I_{OZL} | $V_{CC} = 5.5\text{ V}$, $V_O = 0.5\text{ V}$ | | | | -50 | | | -50 | μA |
| I_{CCL} | $V_{CC} = 5.5\text{ V}$ | | | 37 | 60 | | 37 | 60 | mA |
| I_{CCH} | $V_{CC} = 5.5\text{ V}$ | | | 2 | 5 | | 2 | 5 | mA |
| I_{CCZ} | $V_{CC} = 5.5\text{ V}$ | | | 5 | 8 | | 5 | 8 | mA |
| C_i | $V_{CC} = 5\text{ V}$, $V_I = 2.5\text{ V}$ or 0.5 V | | | 6 | | | 6 | | pF |
| C_o | $V_{CC} = 5\text{ V}$, $V_O = 2.5\text{ V}$ or 0.5 V | | | 11 | | | 11 | | pF |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ | | SN54BCT373 | | SN74BCT373 | | UNIT |
|----------|-----------------------------|---|-----|------------|-----|------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_w | Pulse duration, LE high | 7.5 | | 7.5 | | 7.5 | | ns |
| t_{su} | Setup time, data before LE↓ | 2 | | 2 | | 2 | | ns |
| t_h | Hold time, data after LE↓ | 5.5 | | 5.5 | | 5.5 | | ns |



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OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

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switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C | | | V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX† | | | | UNIT |
|------------------|-----------------|----------------|--|-----|------|--|------|------------|------|------|
| | | | 'BCT373 | | | SN54BCT373 | | SN74BCT373 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} | D | Q | 2 | 5.9 | 7.7 | 1.5 | 10.1 | 2 | 9.3 | ns |
| t _{PHL} | | | 2 | 6.7 | 8.5 | 1 | 10.3 | 1.5 | 9.5 | |
| t _{PLH} | LE | Q | 2 | 6.2 | 8.2 | 2 | 10.1 | 2 | 9.3 | ns |
| t _{PHL} | | | 2 | 5.9 | 7.8 | 2 | 9.2 | 2 | 8.8 | |
| t _{PZH} | \overline{OE} | Q | 1 | 7.8 | 9.6 | 1 | 12.3 | 1 | 11.8 | ns |
| t _{PZL} | | | 1 | 8.2 | 10.2 | 1 | 12.5 | 1 | 12 | |
| t _{PHZ} | \overline{OE} | Q | 1 | 4.9 | 6.6 | 1 | 7.4 | 1 | 7 | ns |
| t _{PLZ} | | | 1 | 5 | 6.7 | 1 | 8.1 | 1 | 7.4 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

SN54BCT373, SN74BCT373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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TYPICAL CHARACTERISTICS†

Figures 1 through 4 show the typical power dissipation for an SN74BCT373 over variations in outputs switching, output frequency, and capacitive load.

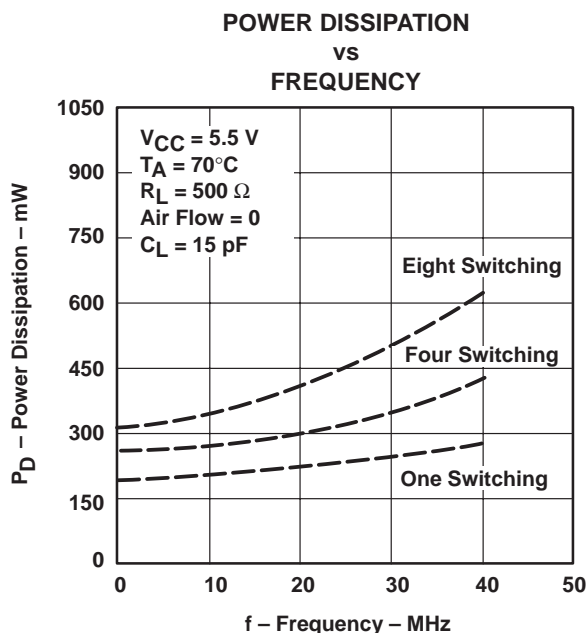


Figure 1

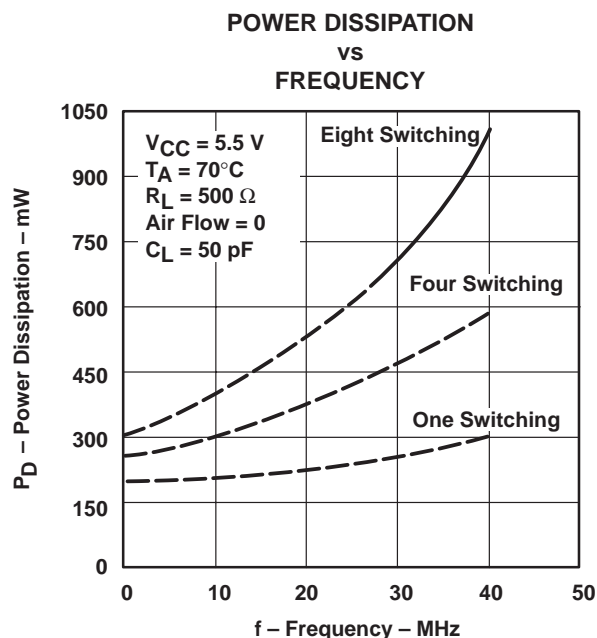


Figure 2

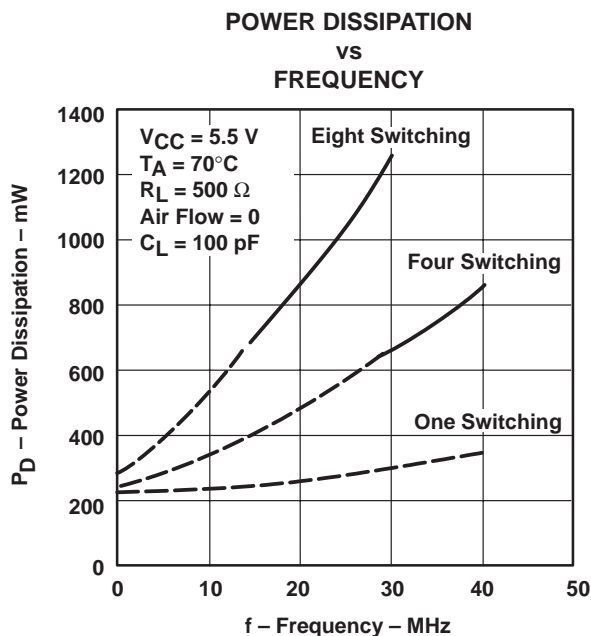


Figure 3

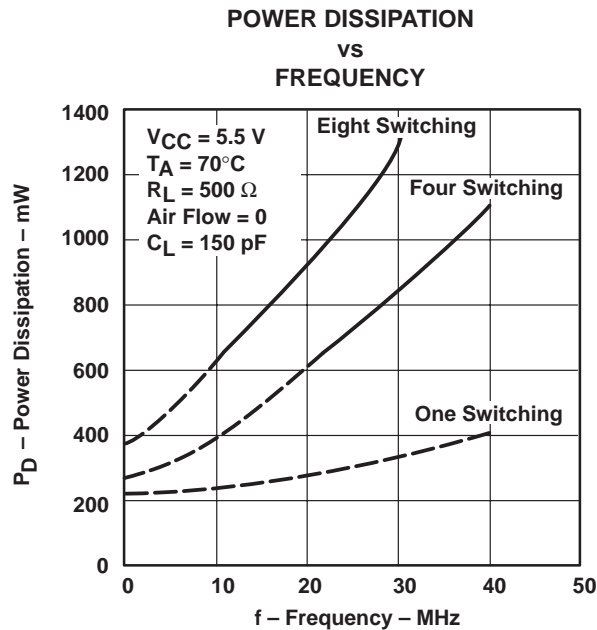


Figure 4

† The dashed lines are for the DB package only.

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