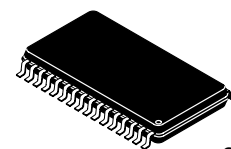


MC143120E2

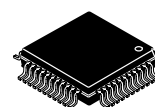
Neuron[®] Chip Distributed Communications and Control Processor

The MC143120E2 contains the LonTalk[®] protocol in 10K ROM. It differs from the MC143120B1 in that it contains only 21 I/O models. Bit Shift, Serial Input, and Serial Output I/O models are not in the ROM firmware, but can be loaded into EEPROM by the LonBuilder[®] tool if needed.

- Three 8-Bit Pipelined Processors for Concurrent Processing of Application Code and Network Packets
- 11-Pin I/O Port Programmable in 34 Modes for Fast Application Program Development
- Two 16-Bit Timer/Counters for Measuring and Generating I/O Device Waveforms
- 5-Pin Communications Port that Supports Direct Connect and Network Transceiver Interfaces
- 2048 Bytes of Static RAM for Buffering Network Data and Storing Network Variables
- 2048 Bytes of EEPROM for Flexible Storage of Address and Binding Data
- Programmable Pull-Ups on IO4 – IO7 and 20 mA Sink Current on IO0 – IO3
- Unique 48-Bit ID Number in Every Device to Facilitate Network Installation and Management — ID Number Stored Redundantly for Guaranteed 20-Year Data Retention
- 32-Pin SOG or 44-Pin PQFP Package
- Low Operating Current: 16 mA (Typical) at 10 MHz Frequency
1.8 mA (Typical) at 625 kHz Frequency
- Sleep Mode Operation Reduced Current Consumption (9 μ A Typical)
- Maximum Clock Operation of 10 MHz, Over a – 40 to + 85°C Temperature Range
- Either LonBuilder Release 3.x or NodeBuilder[®] Software is Required for Programming
- On-Chip LVI Circuit Enabled Reset Below 4.1 V \pm 300 mV Range



DW SUFFIX
SOG PACKAGE
CASE 1116-0



FB SUFFIX
PQFP PACKAGE
CASE 824E-02

ORDERING INFORMATION

MC143120E2DW	SOG Package
MC143120E2FB	PQFP Package

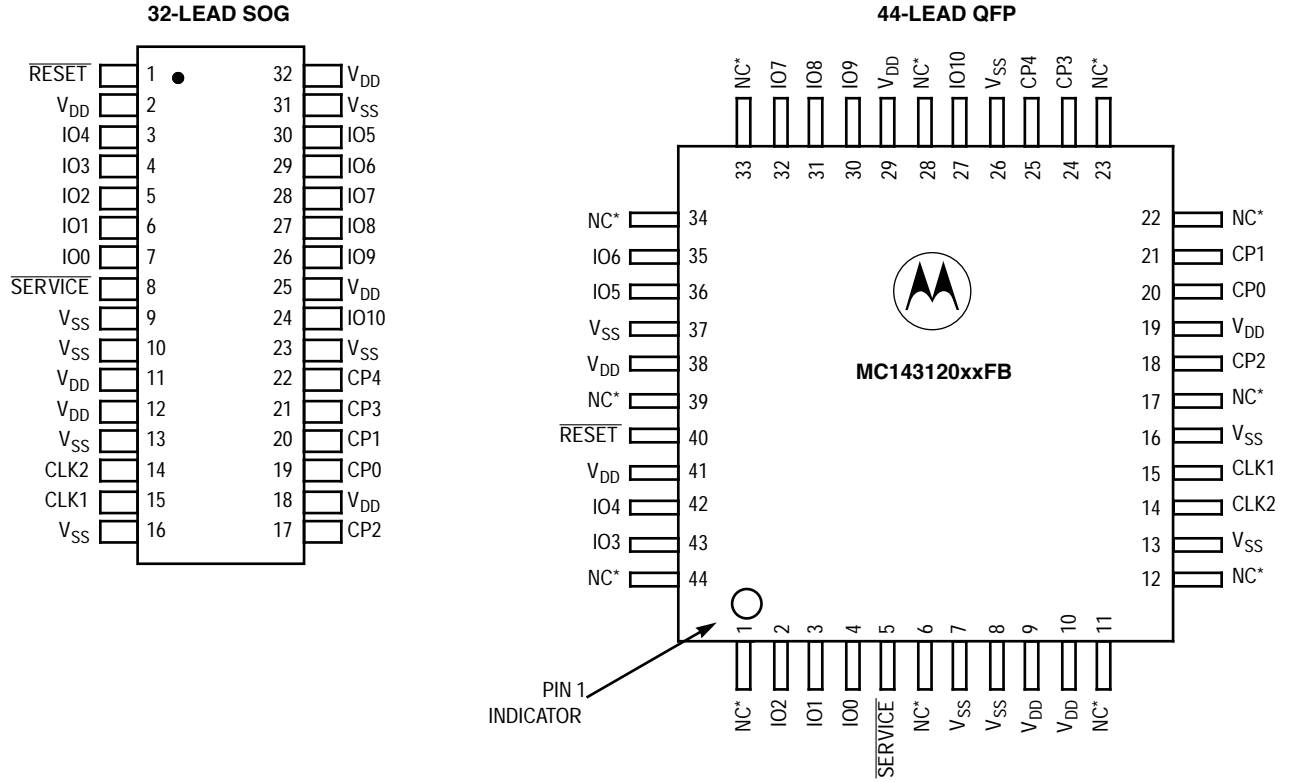
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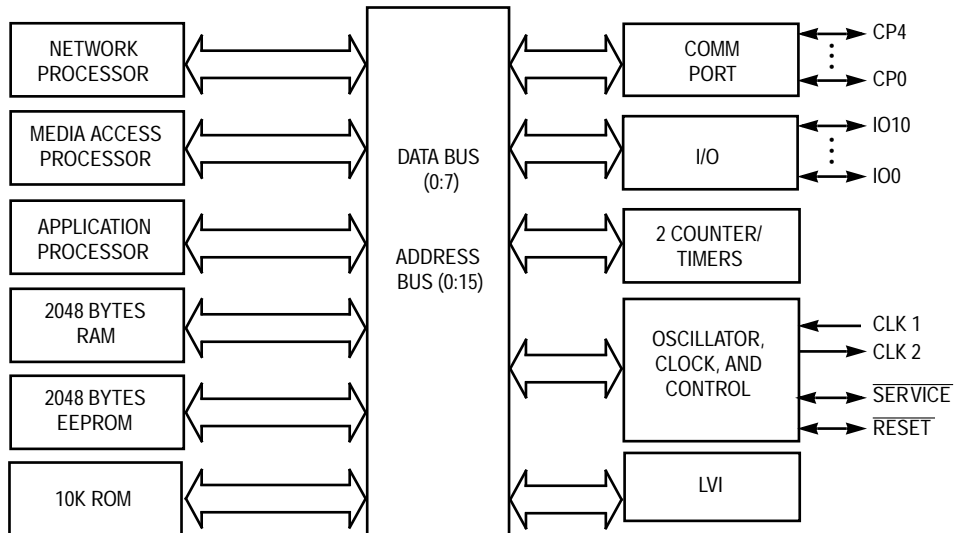
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PIN ASSIGNMENTS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage Range (Referenced to V_{SS})	V_{DD}	– 0.3 to 7.0 V	V
Input Voltage Range (Referenced to V_{SS})	V_{in}	– 0.3 to $V_{DD} + 0.3$	V
Maximum Drain Current	I_{DD}	200	mA
Maximum Source Current	I_{SS}	300	mA
Maximum Power Dissipation	P_D	800	mW
Operating Temperature	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} , $T_A = -40$ to + 85°C)

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	4.5	5.5	V
TTL Low-Level Input Voltage	V_{IL}	V_{SS}	0.8	V
TTL High-Level Input Voltage	V_{IH}	2.0	V_{DD}	V
Operating Free-Air Temperature	T_A	– 40	+ 85	°C

ELECTRICAL CHARACTERISTICS ($V_{DD} = 4.5$ to 5.5 V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Low Voltage IO0 – IO10, CP0, CP3, CP4, <u>SERVICE</u> CP0, CP1 (Differential) RESET	V_{IL}	—	—	0.8 Programmable 0.8	V
Input High Voltage IO0 – IO10, CP0, CP3, CP4, <u>SERVICE</u> CP0, CP1 (Differential) RESET	V_{IH}	2.0 Programmable $V_{DD} - 0.7$	—	—	V
Low-Level Output Voltage $I_{out} \leq 20 \mu A$ Standard Outputs ($I_{OL} = 1.4$ mA) (Note 1) High Sink (IO0 – IO3), <u>SERVICE</u> , RESET ($I_{OL} = 20$ mA) High Sink (IO0 – IO3), <u>SERVICE</u> , RESET ($I_{OL} = 10$ mA) Maximum Sink (CP2, CP3) ($I_{OL} = 40$ mA) Maximum Sink (CP2, CP3) ($I_{OL} = 15$ mA)	V_{OL}	—	—	0.1 0.4 0.8 0.4 1.0 0.4	V
High-Level Output Voltage $I_{out} \leq 20 \mu A$ Standard Outputs ($I_{OH} = -1.4$ mA) (Note 1) High Sink (IO0 – IO3), <u>SERVICE</u> ($I_{OH} = -1.4$ mA) Maximum Source (CP2, CP3) ($I_{OH} = -40$ mA) Maximum Source (CP2, CP3) ($I_{OH} = -15$ mA)	V_{OH}	$V_{DD} - 0.1$ $V_{DD} - 0.4$ $V_{DD} - 0.4$ $V_{DD} - 1.0$ $V_{DD} - 0.4$	—	—	V
Hysteresis (Excluding CLK1, RESET)	V_{hys}	175	—	—	mV
Input Current (Excluding Pull-Ups) (V_{SS} to V_{DD}) (Note 2)	I_{in}	—	—	± 10	μA
Pull-Up Source Current ($V_{out} = 0$ V, Output = High-Z) (Note 2)	I_{pu}	60	—	260	μA
Operating Mode Supply Current (Notes 3, 4)					mA
10 MHz Clock		—	16	N/A	
5 MHz Clock		—	8		
2.5 MHz Clock		—	5.0		
1.25 MHz Clock		—	3.5		
0.625 MHz Clock		—	1.8		
Sleep Mode Supply Current (Notes 3, 4)		—	9	100	μA

NOTES:

- Standard outputs are IO4 – IO10, CP0, CP1, and CP4. (RESET is an open drain input/output. CLK2 must have ≤ 15 pF.)
- IO4 – IO7 and SERVICE have configurable pull-ups. RESET has a permanent pull-up.
- Supply current measurement conditions: all outputs under no-load conditions, all inputs ≤ 0.2 V or $\geq (V_{DD} - 0.2)$ V, configurable pull-ups off, crystal oscillator clock input, differential receiver disabled. The differential receiver adds approximately 200 μA typical and 600 μA maximum when enabled. It is enabled on either of the following conditions:
 - Neuron Chip in Operating mode **and** Comm Port in Differential mode.
 - Neuron Chip in Sleep mode **and** Comm Port in Differential mode **and** Comm Port Wakeup not masked.
- Typical values are at midpoint of voltage range and 25°C only.

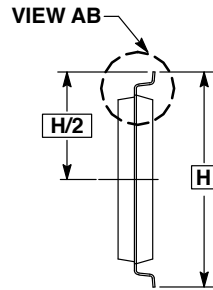
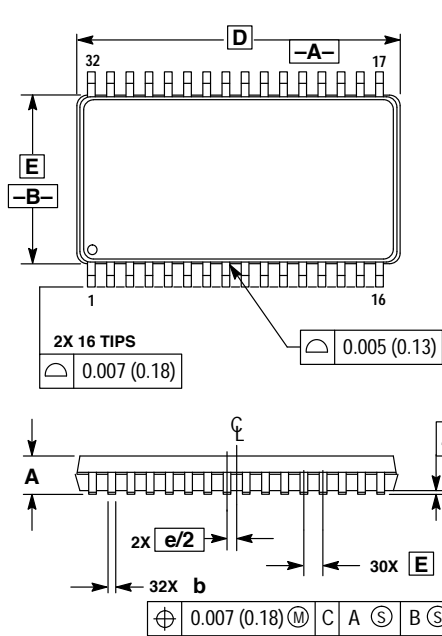
RESET TRIP POINT (V_{DD})

Part Number	Min	Typ	Max	Unit
On-Chip LVI Trip Point	3.8	4.1	4.4	V

Table 1. Pin Descriptions

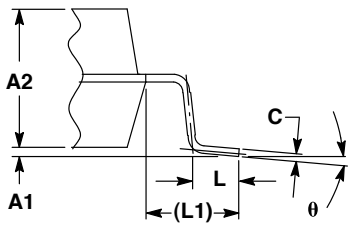
Pin Name	I/O	Pin Function	DW Suffix Pin Number	FB Suffix Pin Number
CLK1	Input	Oscillator connection or external clock input.	15	15
CLK2	Output	Oscillator connection. Leave open when external clock is input to CLK1. Capable of driving one CMOS load (≤ 15 pF load).	14	14
RESET	I/O	Reset pin (active low).	1	40
SERVICE	I/O (Built-In Configurable Pull-Up)	Service pin. Indicator output during operation.	8	5
IO0 – IO3	I/O	Large current-sink capacity (20 mA). General I/O port.	4 – 7	2 – 4, 43
IO4 – IO7	I/O (Built-In Configurable Pull-Up)	General I/O port. One of IO4 to IO7 can be specified as No. 1 timer/counter input with IO0 as output. IO4 can be used as the No. 2 timer/counter input with IO1 as output.	3, 28 – 30	32, 35, 36, 42
IO8 – IO10	I/O	General I/O port. Can be used for serial communication with other devices.	24, 26, 27	27, 30, 31
V_{DD}	Input	Power input (5 V nom). All V_{DD} pins must be connected together externally.	2, 11, 12, 18, 25, 32	9, 10, 19, 29, 38, 41
V_{SS}	Input	Power input (0 V, GND). All V_{SS} pins must be connected together externally.	9, 10, 13, 16, 23, 31	7, 8, 13, 16, 26, 37
CP0 – CP4	Communication Network Interface	Bidirectional port that supports communications protocols by specifying mode.	17, 19 – 22	18, 20, 21, 24, 25
NC	N/A	These pins must not have any external connection.	N/A	1, 6, 11, 12, 17, 22, 23, 28, 33, 34, 39, 44

DW SUFFIX
SOG PACKAGE
CASE 1116-01



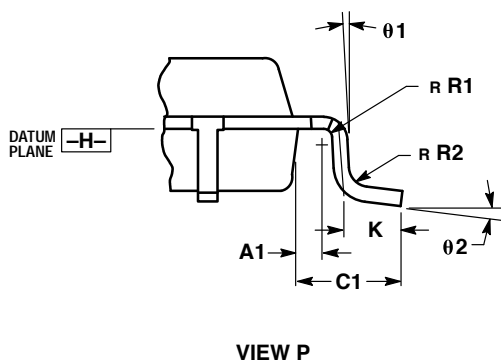
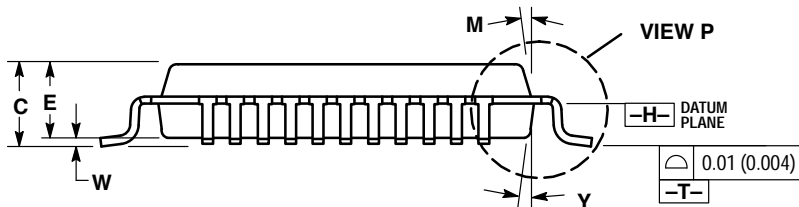
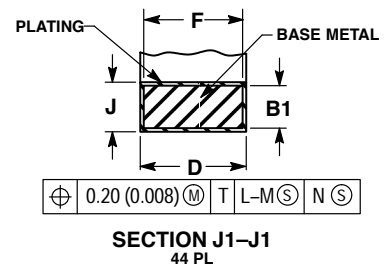
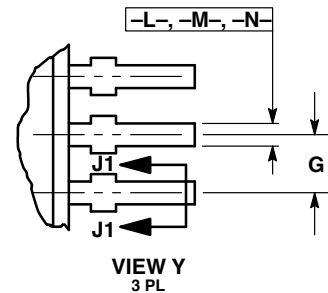
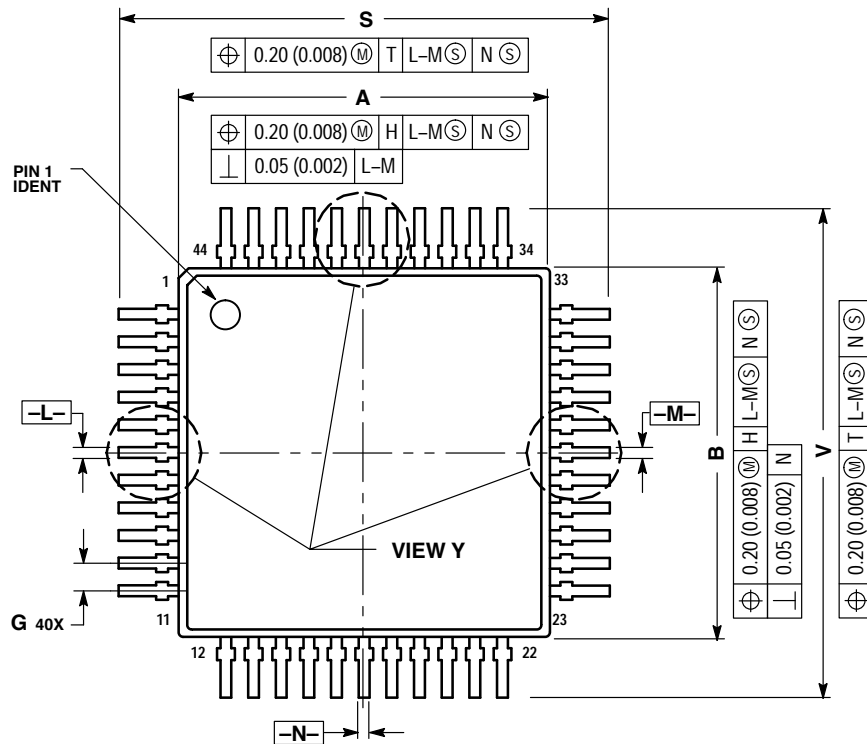
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCHES.
 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSIONS SHALL NOT EXCEED 0.006 (0.15) PER SIDE.
 4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.026 (0.65).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.090	0.100	2.29	2.54
A1	0.004	0.010	0.10	0.25
A2	0.086	0.090	2.18	2.29
b	0.014	0.020	0.35	0.51
C	0.004	0.009	0.10	0.22
D	0.825 BSC		20.96 BSC	
E	0.430 BSC		10.92 BSC	
e	0.050 BSC		1.27 BSC	
H	0.560 BSC		14.22 BSC	
L	0.021	0.041	0.33	1.04
L1	0.120 REF		3.048 REF	
θ	0°	8°	0°	8°



VIEW AB

FB SUFFIX
PQFP PACKAGE
CASE 824E-02

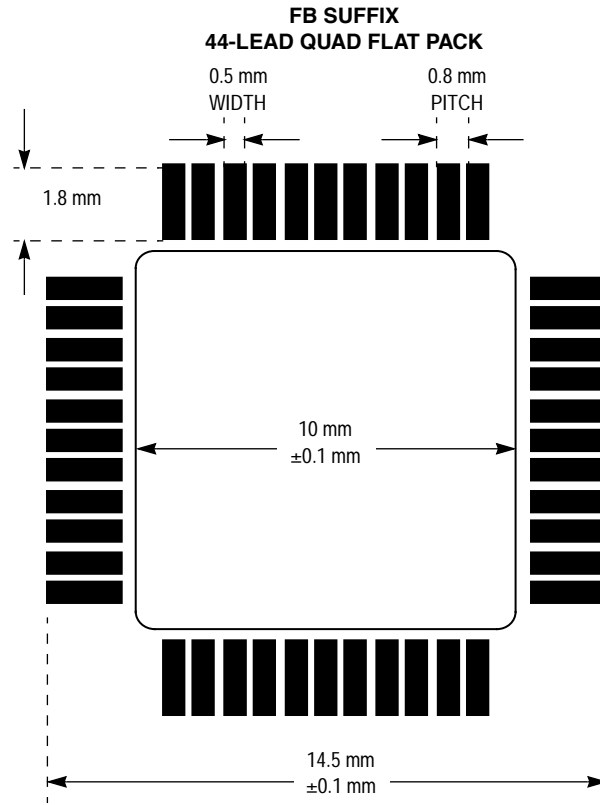
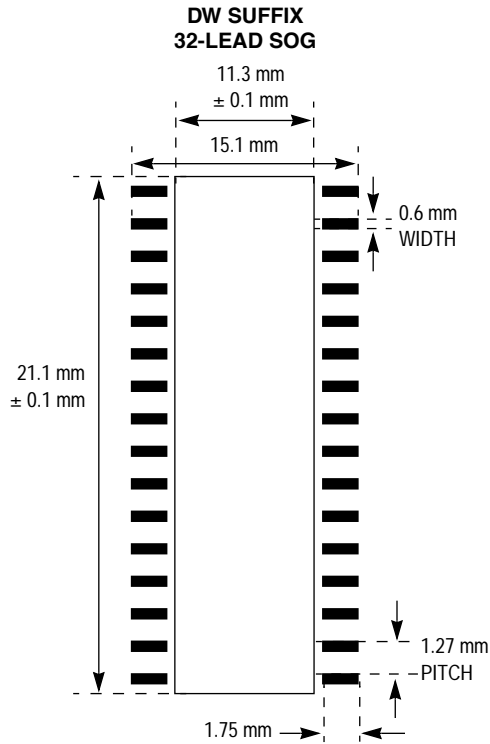


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -L-, -M- AND -N- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -T-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.530 (0.021).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.00	2.21	0.079	0.087
D	0.30	0.45	0.0118	0.0177
E	2.00	2.10	0.079	0.083
F	0.30	0.40	0.012	0.016
G	0.80	BSC	0.031	BSC
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
M	5°	10°	5°	10°
S	12.95	13.45	0.510	0.530
V	12.95	13.45	0.510	0.530
W	0.000	0.210	0.000	0.008
Y	5°	10°	5°	10°
A1	0.450	REF	0.018	REF
B1	0.130	0.170	0.005	0.007
C1	1.600	REF	0.063	REF
R1	0.130	0.300	0.005	0.012
R2	0.130	0.300	0.005	0.012
θ1	5°	10°	5°	10°
θ2	0°	7°	0°	7°

MC143120 PAD LAYOUTS




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