

TPS389xA-xP-EVM047 Evaluation Modules

This user's guide describes the characteristics and operational use of the TPS389XA-XP-EVM047 Evaluation Module (EVM) for engineering demonstration of the TPS3897A and TPS3896P supervisors (TPS3897A-6P-EVM047), the TPS3897P and TPS3896A supervisors (TPS3897P-6A-EVM047), the TPS3898A and TPS3895P supervisors (TPS3898A-5P-EVM047), or the TPS3898P and TPS3895A supervisors (TPS3898P-5A-EVM047). These EVMs are fully assembled and tested platforms for evaluating the performance of the TPS389xA-xP family of supervisory circuits. Any one EVM can be manually modified to easily accommodate alternative supervisor ICs of this same family. This TPS389XA-XP family are adjustable supervisors in an ultra small package, that can monitor voltages greater than the 500 mV sense voltage, whose accuracy is better than 1%. This user's guide includes setup instructions, schematic, bill of materials (BOM), layout, and test results for a typical SVS circuit on the EVM

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1 Introduction

The TPS389xA-xP-EVM047 helps designers evaluate the operation and performance of the TPS389xA-xP family of single channel supervisors (SVS) available in the ultra small μ Son package. Each EVM has two completely independent SVS circuits each preprogrammed by a resistor divider to monitor a 3.3 V SVS SENSE rail. Each SVS circuit issues the active Sense_out when the SVS SENSE voltage rises above the preprogrammed threshold, which in this case is set to 94.5% of the 3.3 V rail (nominally) by the divider resistors. The Sense_out is inactive when the SVS SENSE falls below the threshold minus hysteresis, or when the part is disabled. The SVS part itself is capable of monitoring voltage rails greater than 500 mV with its 1% accurate reference, is available with active high or low, push-pull or open-drain output drivers, and its Sense_out time delay is adjustable by an external capacitor. Each SVS circuit on the EVM use a 0.047 μ F capacitor to program the Sens_out time delays to 190 ms (nominally). The TPS389xA-xP family of supervisory circuits provides circuit initialization and timing for power good and reset to DSPs and microprocessor-based systems.

1.1 Features

- Low quiescent current: 6 μ A (typical)
- Power-on RESET generator with capacitor adjustable delay time
- Open-Drain/Push Pull output options
- External Enable Input
- Threshold accuracy of 1% over temperature

1.2 EVM Interface Information and Orderable Options (Dependent on Customer Demand and Availability)

The EVM contains two complete operational SVS circuits supporting two TPS389xA-xP ICs installed at U1 and U2 on the EVM. [Table 1](#) describes the input/output interface to each circuit per orderable EVM.

NOTE: SVS parts with the “A” designator employ the time delay capacitor to set both the Sense_out time delay and the Enable time delay. SVS parts designated with the “P” employ the time delay capacitor to set the SENSE_OUT time delay only.

Table 1. SVS Circuit Interface Information based on EVM Orderable

EVM Orderable	Part	Designator	ENABLE (EN)	OUTPUT (Sense_out)	INPUT DELAY (Sense_out relative to SVS SENSE)	ENABLE Delay (Sense_out relative to active EN)
TPS3897A-6P-EVM047	TPS3897A	U1	Active High	Active High, Open-Drain	Capacitor Adjustable	Capacitor Adjustable
	TPS3896P	U2	Active Low	Active Low, Push-Pull	Capacitor Adjustable	200ns
TPS3897P-6A-EVM047	TPS3897P	U1	Active High	Active High, Open-Drain	Capacitor Adjustable	200ns
	TPS3896A	U2	Active Low	Active Low, Push-Pull	Capacitor Adjustable	Capacitor Adjustable
TPS3898A-5P-EVM047	TPS3898A	U1	Active Low	Active Low, Open-Drain	Capacitor Adjustable	Capacitor Adjustable
	TPS3895P	U2	Active High	Active High, Push-Pull	Capacitor Adjustable	200ns
TPS3898P-5A-EVM047	TPS3898P	U1	Active Low	Active Low, Open-Drain	Capacitor Adjustable	200ns
	TPS3895A	U2	Active High	Active High, Push-Pull	Capacitor Adjustable	Capacitor Adjustable

2 Schematic

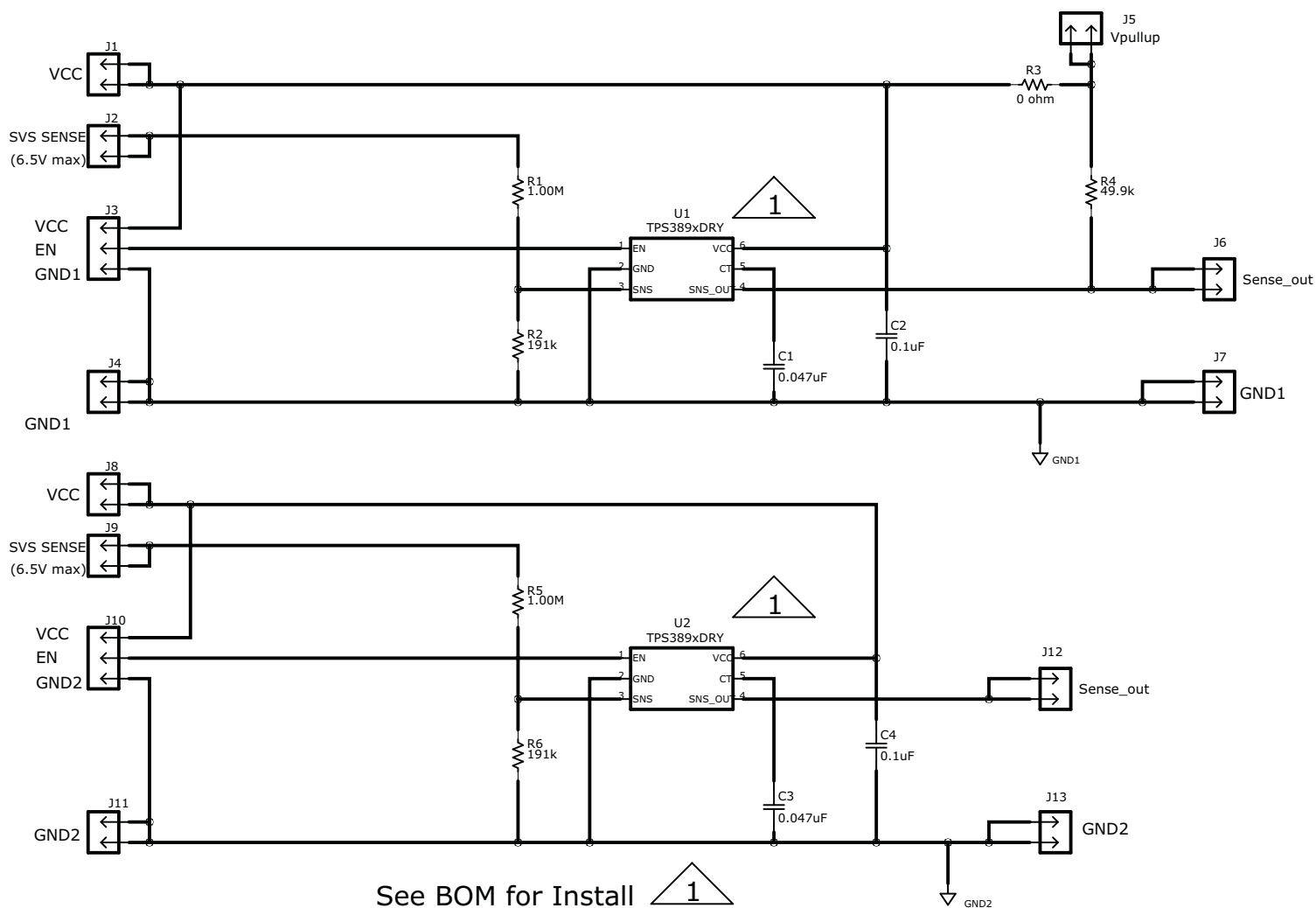


Figure 1. TPS389xA-xP-EVM-047 Schematic

3 I/O Description, Threshold and Delay Calculations, and Setup

3.1 EVM Input/Output Connectors and Test Jumpers

Table 2. EVM Input/Output Connectors and Jumpers

Connector	Label	Description
J1, J8	VCC	Input power supply connection to the U1 and U2 SVS circuits, respectively: 1.7 V to 6.5 V .
J2, J9	SVS SENSE	Monitored supervisor sense voltage input to the U1 and U2 SVS circuits, respectively. This monitored voltage is compared to the 0.5 V reference at the SENSE pin of the IC through the resistor divider, R1–R2 or R5–R6 respectively.
J4, J7	GND1	Ground return for the input power supply (VCC), the SVS SENSE and the Sense_out of the U1 SVS circuit.
J6, J12	Sense_out	Logically Active when the SVS SENSE is above threshold and the circuit is enabled. Logically inactive when the SVS is disabled and the SVS SENSE is less than the threshold minus the threshold hysteresis.
J11,J13	GND2	Ground return for the input power supply (VCC), the SVS SENSE and the Sense_out of the U2 SVS circuit.
J3, J10	EN	Enable for the U1 and U2 SVS circuits respectively. Jumpering J3 (J10) from EN (pin 2) to VCC (pin 1) enables those SVS circuits with active high enable (see Table 1). Jumpering J3 (J10) from EN (pin 2) to GND (pin 3) enables those SVS circuits with active low enable (see section Section 1.2)
J5	Vpull-up	External pull-up voltage input for the open-drain Sense_out. Normally this pull-up is accomplished through an on-board 0 Ω resistor (R3) to VCC. Remove R3 before applying a V pullup voltage (up to 20 V abs max).

3.2 CT and Output Delay Time

An external capacitor is connected between the CT pin and GND to program the adjustable delay time. Each EVM SVS circuit uses a 0.047 μF ceramic capacitor to gives a delay of 190 ms. If the CT pin is left open, there will be a delay of 40 μs. The adjustable time delay, can be calculated using the following equation (found in the data sheet):

$$t_{DL} = (C_{CT} \times 4 \times 10^6) + 40 \mu s \quad (1)$$

Where C_{CT} is the capacitance in farads and t_{DL} is the time delay in seconds. This equation sets the enable and input delays.

3.3 SVS SENSE Voltage Threshold: Programming the Threshold Voltage

The SVS SENSE voltage is monitored at the SENSE pin of the IC through an on board resistive voltage divider. This divider is designed to trigger the active Sense_out when the SVS SENSE voltage crosses the threshold set by the divider. Typically this threshold voltage, V_{thresh} , is set lower than the nominal rail voltage being monitored by a few percent depending on the application. This EVM has set the threshold voltage to be approximately 5.5% below monitored SVS SENSE voltage of 3.3 V. The nominal resistor values for a given threshold voltage can be calculated from [Equation 2](#):

$$V_{thresh} = (1 + R1/R2) \times 0.5 V \quad (2)$$

Where the R1 and R2 resistors are place values representing the R1-R2 resistors shown in the U1 SVS circuit or the R5-R6 resistors shown in the U2 SVS circuit of the EVM, respectively.

[Equation 2](#) does not account for the tolerances of the divider resistors, the accuracy of the SVS SENSE threshold voltage or the accuracy of the reference voltage. For the TPS389xA-xP, the reference voltage accuracy is 0.5 V±1%.

[Equation 3](#) calculates the nominal threshold voltage and its error as a function of the reference accuracy and the divider resistor tolerance.

$$V_{thresh} \pm Error = \underbrace{(1 + R1/R2)}_{V_{thresh}} \underbrace{\times 0.5 (1 \pm 0.01)}_{\text{Reference Accuracy}} \underbrace{\pm 2 \times R_{tol} (1 - V_{sense}/V_{thresh})}_{\text{Resistor Tolerance Error}} \quad (3)$$

Where R_{tol} is the tolerance of the divider resistors as a decimal.

Table 3 shows the SVS SENSE threshold accuracy based on the resistor tolerance and the reference accuracy values.

Table 3. SVS SENSE Threshold Accuracy and Resistor Divider Selection

Monitor SVS Voltage	Threshold Voltage (nominal)	R1(R5) Selection (0.1% Tol) Ω	R2 (R6) Calculation (0.1% Tol) Ω	Threshold Accuracy Min/Max Threshold Voltage
1.8 V	1.699 V (5.61% below SVS Voltage)	1M	422K	1.68V / 1.72V
3.3 V	3.118 V (5.52% below SVS Voltage)	1M	191K	3.08V / 3.15V
5.0 V	4.667 V (6.66% below SVS Voltage)	1M	120K	4.61V / 4.72V

3.4 SETUP: Connecting to the SVS Circuit of U1 (U2).

3.4.1 Connect the VCC power supply to power the circuit from J1 (J8) to ground, GND1 (GND2) at J4 (J11).

3.4.2 Observe the output between Sense_out, J6 (J12), and ground, J7 (J13), using a voltmeter and or an oscilloscope.

3.4.3 Enable the SVS circuit by correctly jumpering J3 (J10) in accord with the Table 2 description.

3.4.4 Connect the monitored voltage the SVS SENSE connector, J2 (J9), and ground, J4 (J11).

3.4.4.1 Vary the monitored voltage level, at SVS SENSE, as needed to see the various responses to the output at Sense_out.

4 Operation

4.1 Operation Description

After applying power to VCC, followed by the active Enable, the Sense_out will become active after the Enable delay, provided that the SVS SENSE voltage is above the programmed threshold voltage. When the SVS SENSE voltage falls below the threshold voltage minus the hysteresis voltage (V_{HYS}) - where $V_{HYS} = 5 \text{ mV} \times (1 + R1/R2)$ - the Sense_out becomes immediately inactive (within 16 μs typical). Assuming that VCC is within operational range and that the EN is active, the output will toggle when the input SVS SENSE voltage rises and falls above-below the threshold.

4.2 Test Results

Figure 2 shows the Sense_out voltage (red, C2) becoming active high approximately 192 ms (Input Delay) after the SVS SENSE voltage (gold, C1) rises above the threshold voltage. The Sense_out signal immediately falls when the SVS SENSE voltage falls below the threshold. The VCC voltage has been previously set to 3.3 V. The SVS circuit being demonstrated employs the TPS3895A supervisory IC.

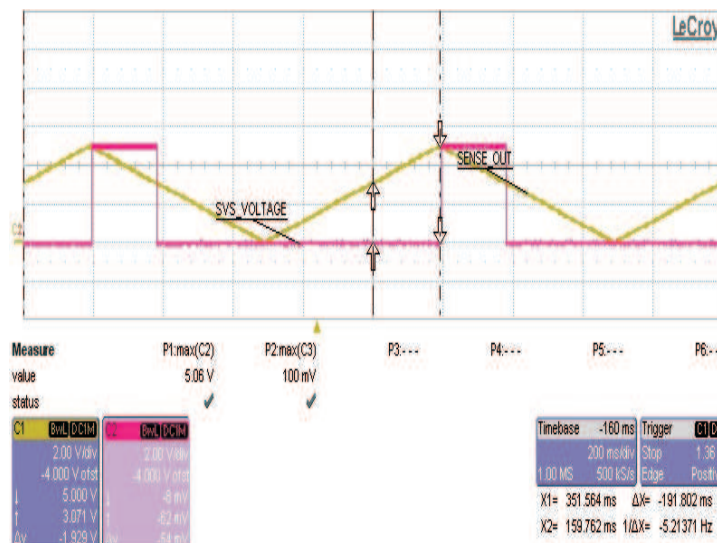


Figure 2. Sense_out response (active high) to rising/falling SVS SENSE (TPS3895A)

Figure 3 shows the Sense_out voltage (gold, C1) becoming active low approximately 160 ms (Input Delay) after the SVS SENSE voltage (blue, C2) rises above the threshold voltage. The Sense_out signal immediately falls when the SVS SENSE voltage falls below the threshold. The VCC voltage has been previously set to 3.3 V. The SVS circuit being demonstrated employs the TPS3895A supervisory IC

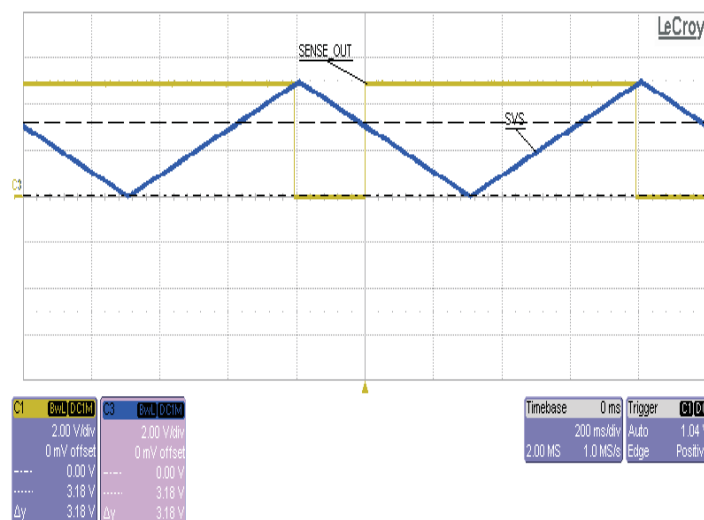


Figure 3. Sense_out response (active low) to rising/falling SVS SENSE (TPS3898A)

This section provides the TPS389XEVM board layout.

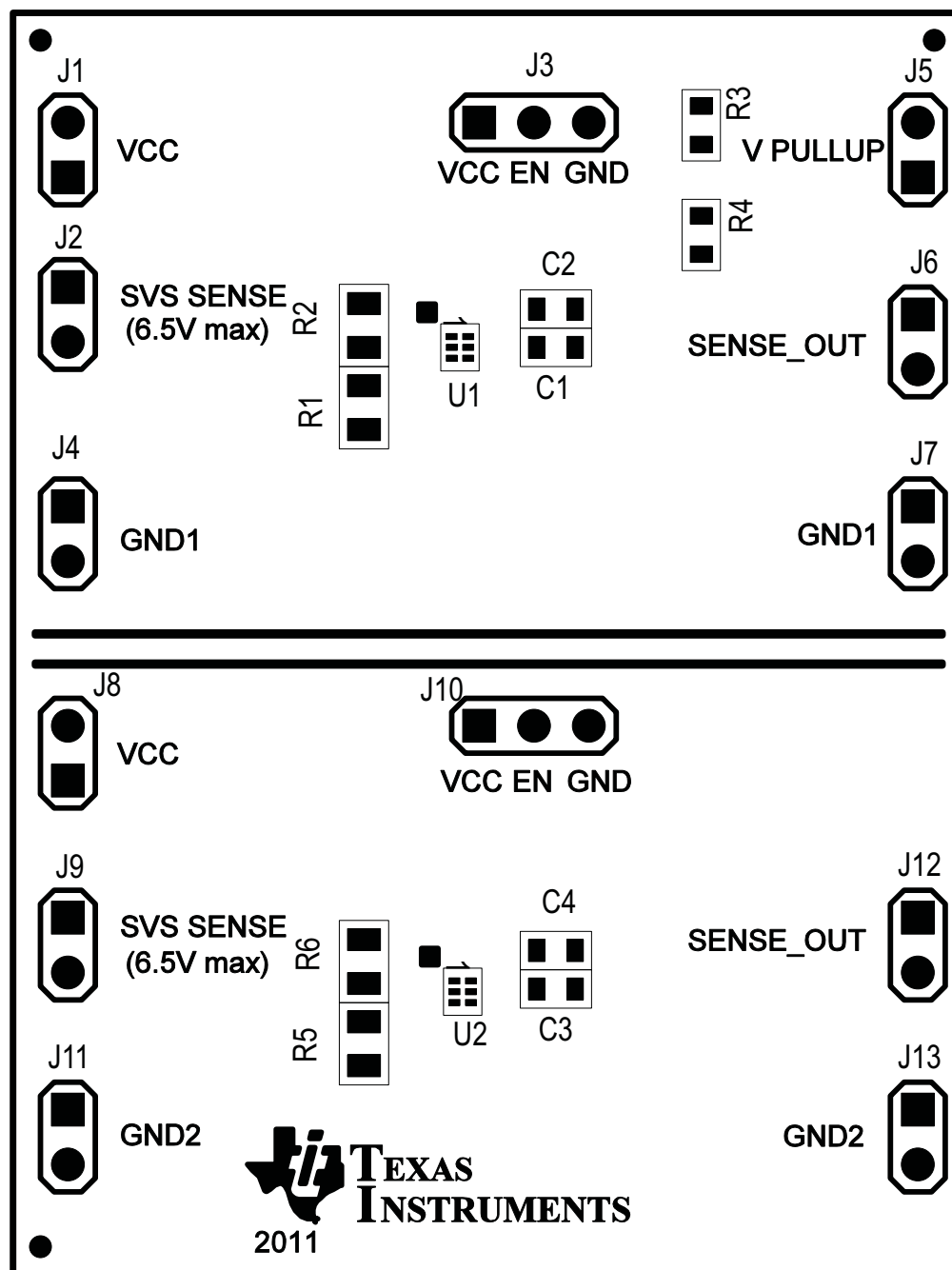


Figure 4. Assembly Layer (Top)

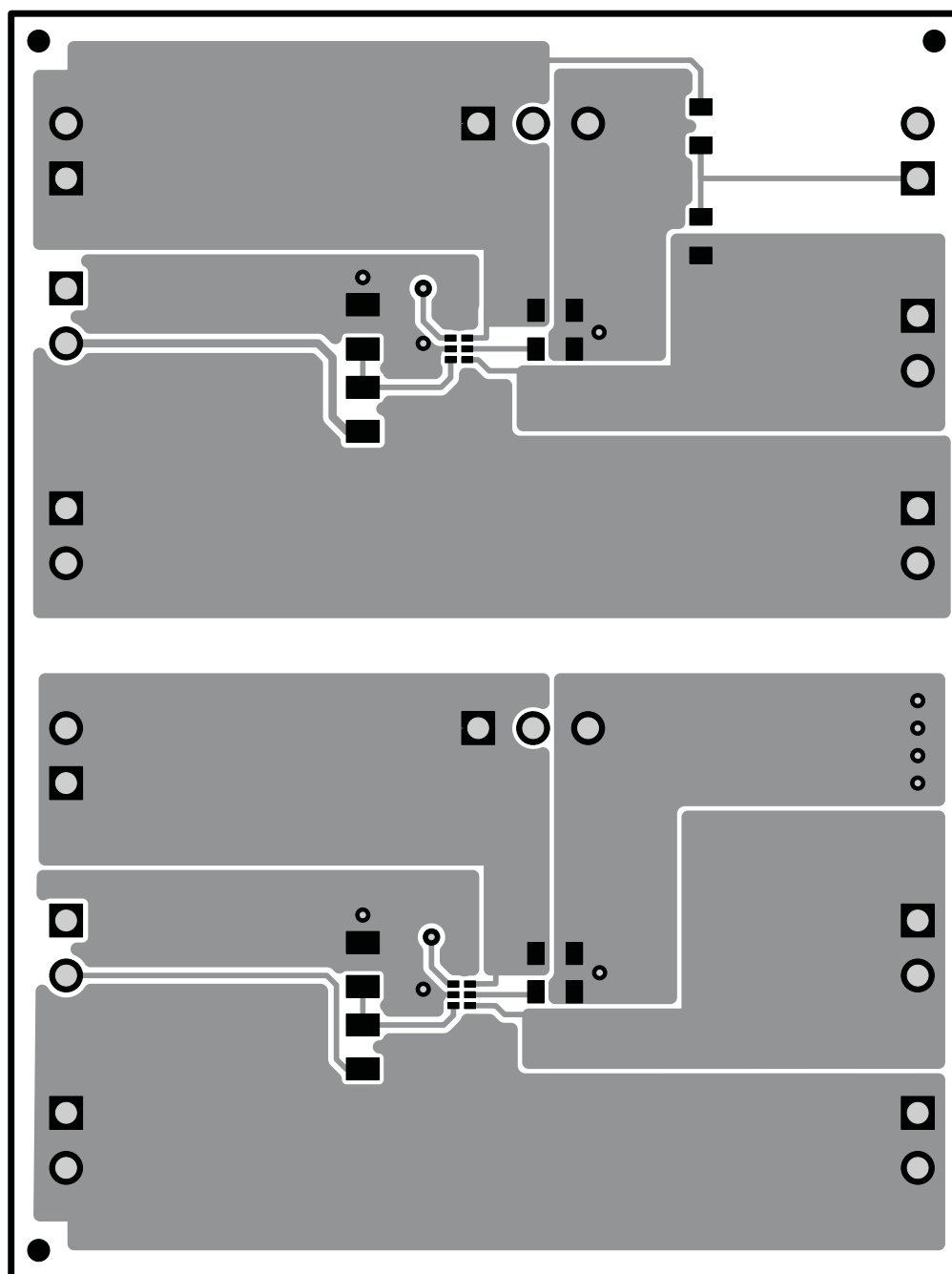


Figure 5. Top Layer Routing

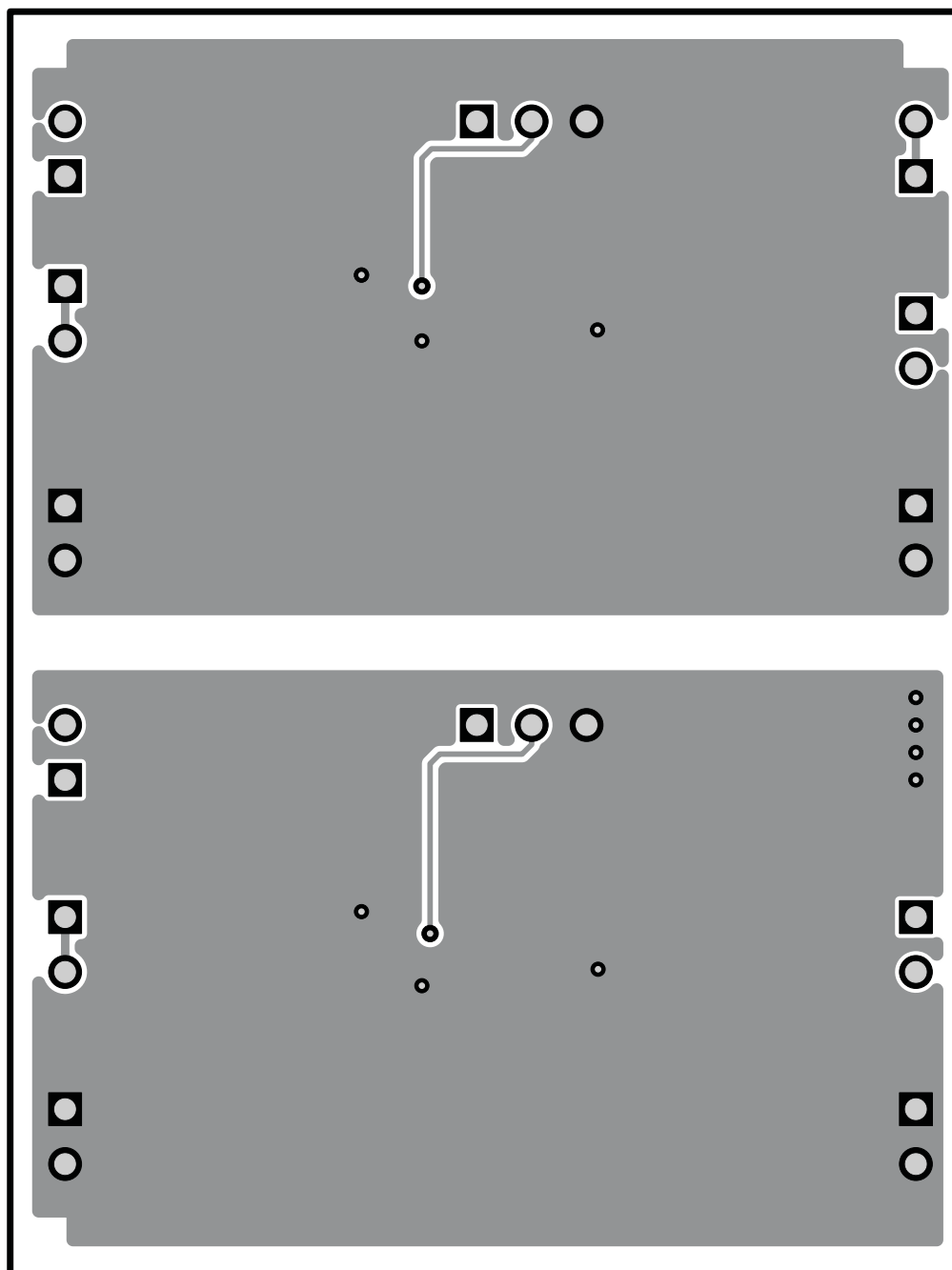


Figure 6. Bottom Layer Routing

6 Bill of Materials

Table 4. EVM Assembly Associated with EVM Orderable

PWR047-001	PWR047-002	PWR047-003	PWR047-004	RefDes	Value	Description	Size	Part Number
COUNT	COUNT	COUNT	COUNT	RefDes	Value	Description	Size	Part Number
2	2	2	2	C1 C3	0.047uF	Capacitor, Ceramic, X7R, 10V 10%	0603	STD
2	2	2	2	C2 C4	0.1uF	Capacitor, Ceramic, X7R, 50V 10%	0603	STD
11	11	11	11	J1-2 J4-9 J11-13	PEC02SAAN	Header, Male 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN
2	2	2	2	J3 J10	PEC03SAAN	Header, Male 3-pin, 100mil spacing	0.100 inch x 3	PEC03SAAN
2	2	2	2	R1 R5	1.00M	Resistor, 1/8W, 0.1%, ±25ppm/°C	0805	ERA-6AEB105V
2	2	2	2	R2 R6	191k	Resistor, 1/8W, 0.1%, ±25ppm/°C	0805	TNPW0805191KBEEA
1	1	1	1	R3	0 ohm	Resistor, Chip, 1/16W, 1%	0402	STD
1	1	1	1	R4	49.9k	Resistor, Chip, 1/16W, 1%	0402	STD
1	0	0	0	U1	TPS3897ADRY	IC, Single Chan Adjustable Supervisory	DSBGA	TPS3897ADRY
0	0	1	0	U1	TPS3898ADRY	IC, Single Chan Adjustable Supervisory	DSBGA	TPS3898ADRY
0	0	0	1	U2	TPS3895ADRY	IC, Single Chan Adjustable Supervisory	DSBGA	TPS3895ADRY
0	1	0	0	U2	TPS3896ADRY	IC, Single Chan Adjustable Supervisory	DSBGA	TPS3896ADRY
0	1	0	0	U1	TPS3897PDRY	IC, Single Chan Adjustable Supervisory	DSBGA	TPS3897PDRY
0	0	0	1	U1	TPS3898PDRY	IC, Single Chan Adjustable Supervisory	DSBGA	TPS3898PDRY
0	0	1	0	U2	TPS3895PDRY	IC, Single Chan Adjustable Supervisory	DSBGA	TPS3895PDRY
1	0	0	0	U2	TPS3896PDRY	IC, Single Chan Adjustable Supervisory	DSBGA	TPS3896PDRY
2	2	2	2	--	Shunt	Shunt, Black	100-mil	929950-00
1	1	1	1	--	Board	PCB, 2.300 In x 1.730 In x 0.062 In		PWR047
Notes:								
1. These assemblies are ESD sensitive, ESD precautions shall be observed.								
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.								
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.								
4. Ref designators marked with an asterisk (**) cannot be substituted. All other components can be substituted with equivalent MFG's components.								
5. Install label after final wash. Text shall be 8 pt font. Text shall be per Table 5 .								
6. Score the board per score line but do not separate them.								

Table 5.

Assembly Number	text
PWR047-001	TPS3897A-6P-EVM047
PWR047-002	TPS3897P-6A-EVM047
PWR047-003	TPS3898A-5P-EVM047
PWR047-004	TPS3898P-5A-EVM047

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 0 V to 7 V and the output voltage range of 0 V to 7 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85° C. The EVM is designed to operate properly with certain components above 85° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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