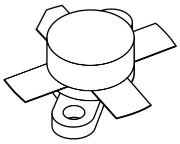


BLF177

HF/VHF power MOS transistor

Rev. 06 — 24 January 2007 **Product data sheet**

IMPORTANT NOTICE

Dear customer,

As from October 1st, 2006 Philips Semiconductors has a new trade name
- NXP Semiconductors, which will be used in future data sheets together with new contact details.
In data sheets where the previous Philips references remain, please use the new links as shown below.

http://www.philips.semiconductors.com use http://www.nxp.com

http://www.semiconductors.philips.com use http://www.nxp.com (Internet)

sales.addresses@www.semiconductors.philips.com use salesaddresses@nxp.com (email)

The copyright notice at the bottom of each page (or elsewhere in the document, depending on the version)
- © Koninklijke Philips Electronics N.V. (year). All rights reserved -
is replaced with:
- © NXP B.V. (year). All rights reserved. -

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or phone (details via salesaddresses@nxp.com). Thank you for your cooperation and understanding,

NXP Semiconductors

founded by Philips

HF/VHF power MOS transistor BLF177

FEATURES

- High power gain
- Low intermodulation distortion
- Easy power control
- Good thermal stability
- Withstands full load mismatch.

APPLICATIONS

- Designed for industrial and military applications in the HF/VHF frequency range.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor encapsulated in a 4-lead, SOT121B flanged package, with a ceramic cap. All leads are isolated from the flange.

A marking code, showing gate-source voltage (V_{GS}) information is provided for matched pair applications. Refer to the handbook 'General' section for further information.

PINNING

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

PIN CONFIGURATION

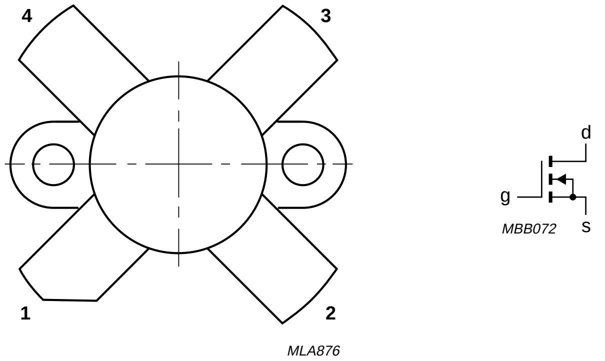


Fig.1 Simplified outline (SOT121B) and symbol.

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

WARNING

Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_3 (dB)	d_5 (dB)
SSB class-AB	28	50	150 (PEP)	>20	>35	<–30	<–30
CW class-B	108	50	150	typ. 19	typ. 70	–	–

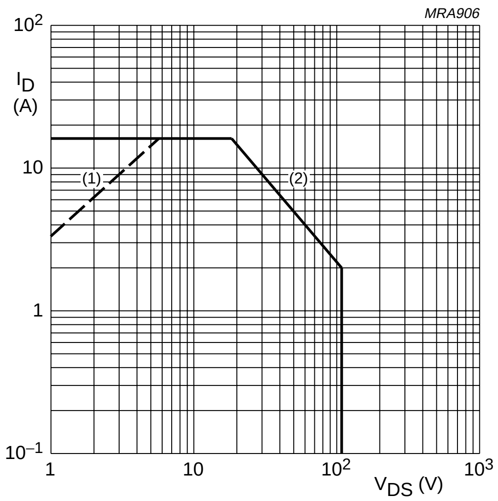
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	125	V
V_{GS}	gate-source voltage		–	±20	V
I_D	drain current (DC)		–	16	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C	–	220	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	200	°C

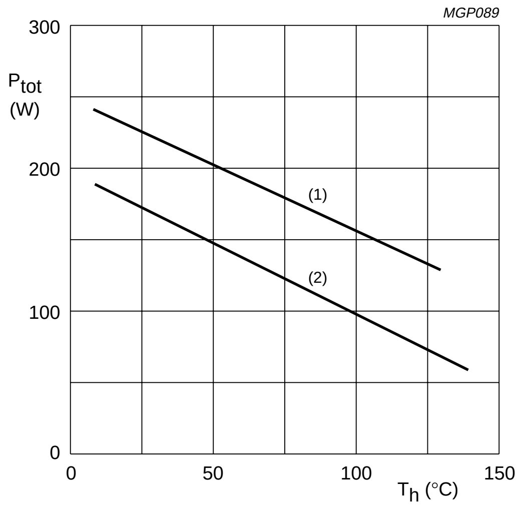
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	max. 0.8	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	max. 0.2	K/W



(1) Current in this area may be limited by R_{DSon}.
(2) $T_{mb} = 25$ °C.

Fig.2 DC SOAR.



(1) Short-time operation during mismatch.
(2) Continuous operation.

Fig.3 Power derating curves.

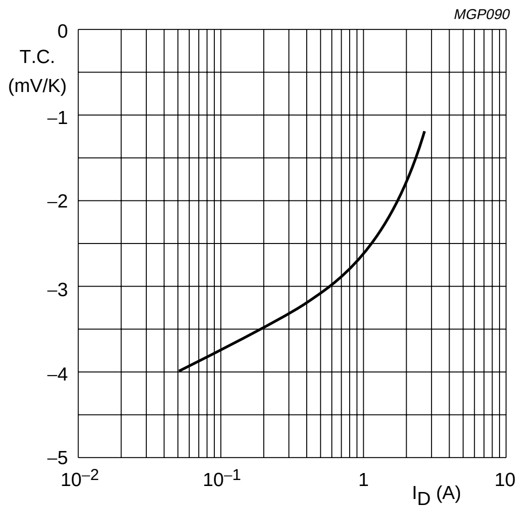
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 100 mA; V_{GS} = 0	125	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 50 V	–	–	2.5	mA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	1	μA
V_{GSth}	gate-source threshold voltage	I_D = 50 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched pairs	I_D = 50 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 5 A; V_{DS} = 10 V	4.5	6.2	–	S
R_{DSon}	drain-source on-state resistance	I_D = 5 A; V_{GS} = 10 V	–	0.2	0.3	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	25	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	480	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	190	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	14	–	pF

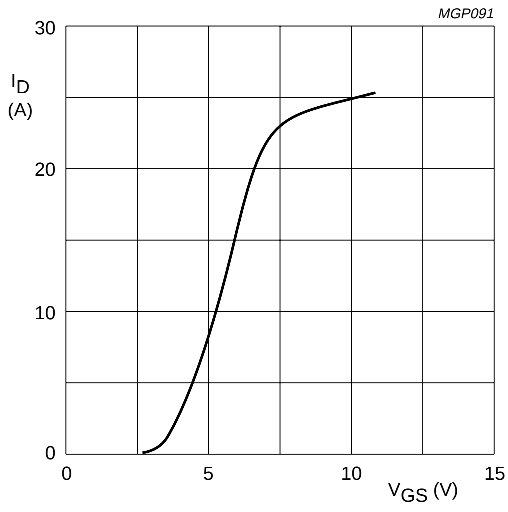
V_{GS} group indication

GROUP	LIMITS (V)		GROUP	LIMITS (V)	
	MIN.	MAX.		MIN.	MAX.
A	2.0	2.1	O	3.3	3.4
B	2.1	2.2	P	3.4	3.5
C	2.2	2.3	Q	3.5	3.6
D	2.3	2.4	R	3.6	3.7
E	2.4	2.5	S	3.7	3.8
F	2.5	2.6	T	3.8	3.9
G	2.6	2.7	U	3.9	4.0
H	2.7	2.8	V	4.0	4.1
J	2.8	2.9	W	4.1	4.2
K	2.9	3.0	X	4.2	4.3
L	3.0	3.1	Y	4.3	4.4
M	3.1	3.2	Z	4.4	4.5
N	3.2	3.3			



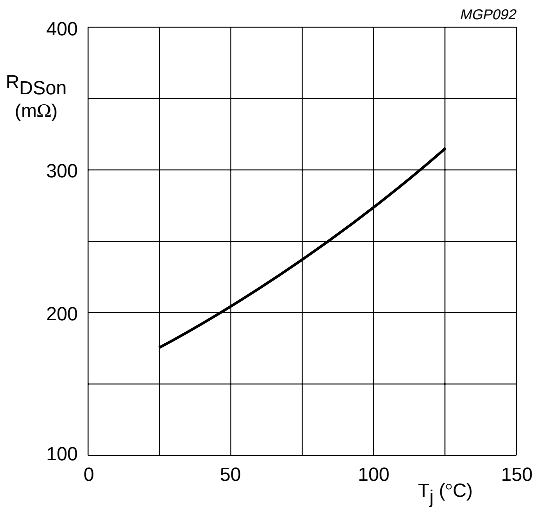
V_{DS} = 10 V; valid for T_h = 25 to 70 °C.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current; typical values.



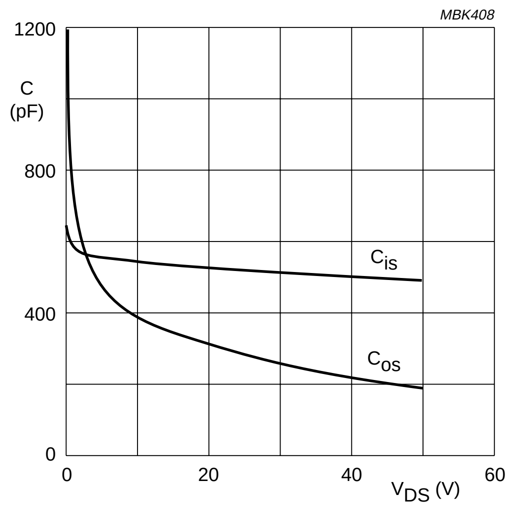
V_{DS} = 10 V.

Fig.5 Drain current as a function of gate-source voltage; typical values.



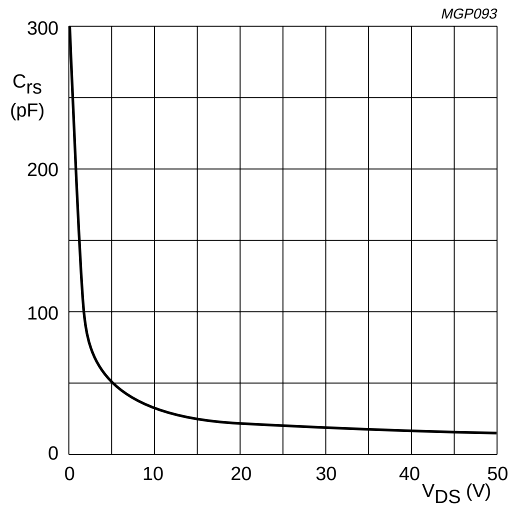
I_D = 5 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature; typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage; typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage; typical values.

APPLICATION INFORMATION FOR CLASS-AB OPERATION

RF performance in SSB operation in a common source class-AB test circuit (see Fig.13).
T_h = 25 °C; $R_{th\ mb-h}$ = 0.2 K/W; Z_L = 6.25 + j0 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz unless otherwise specified.

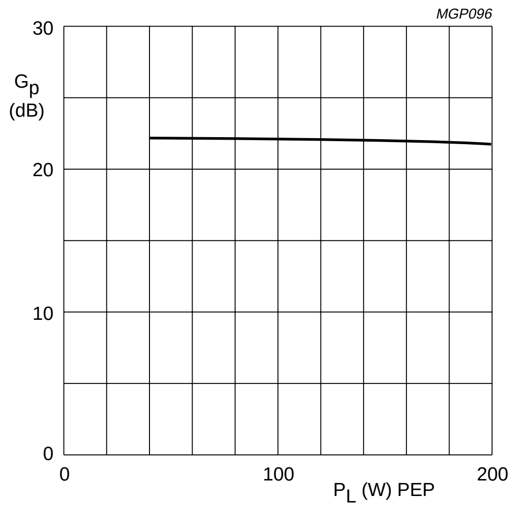
MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)	d_3 (dB) (note 1)	d_5 (dB) (note 1)
SSB, class-AB	28	50	0.7	20 to 150 (PEP)	>20 typ. 35	>35 typ. 40	<–30 typ. –35	<–30 typ. –38

Note

1. Maximum values at drive levels within the specified PEP values for either amplified tone. For the peak envelope power the values should be decreased by 6 dB.

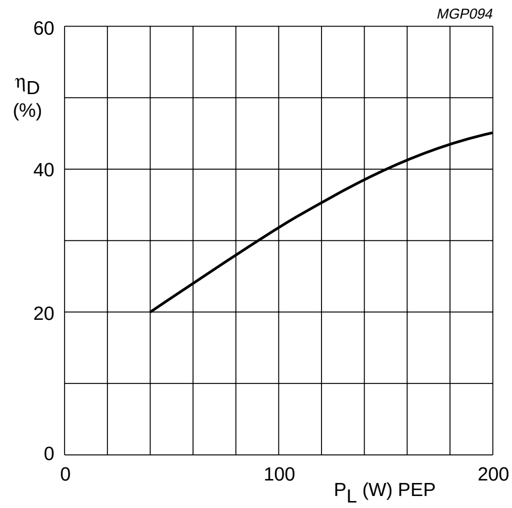
Ruggedness in class-AB operation

The BLF177 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases under the following conditions: f = 28 MHz; V_{DS} = 50 V at rated output power.



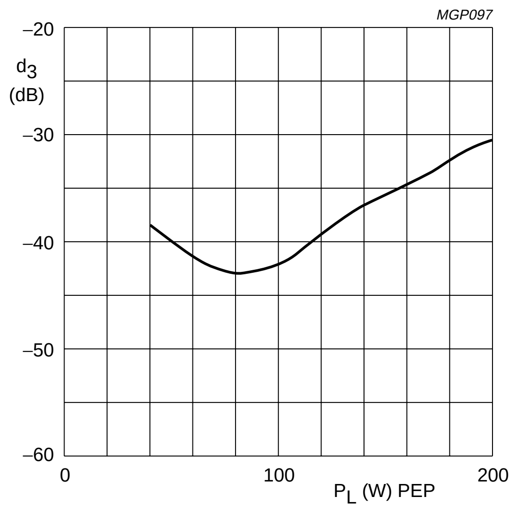
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.7 A;
R_{GS} = 5 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.9 Power gain as a function of load power; typical values.



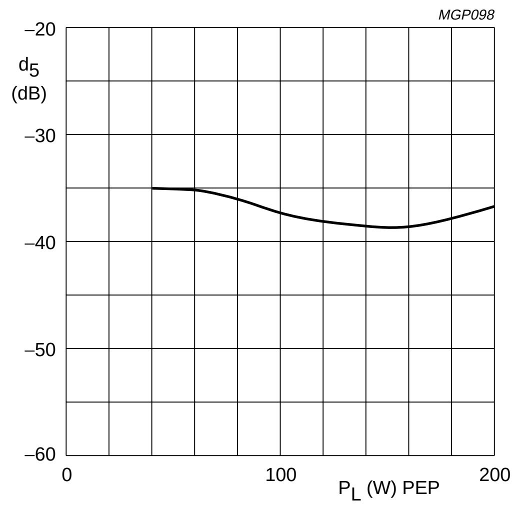
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.7 A;
R_{GS} = 5 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.10 Two tone efficiency as a function of load power; typical values.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.7 A;
R_{GS} = 5 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.11 Third order intermodulation distortion as a function of load power; typical values.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.7 A;
R_{GS} = 5 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.12 Fifth order intermodulation distortion as a function of load power; typical values.

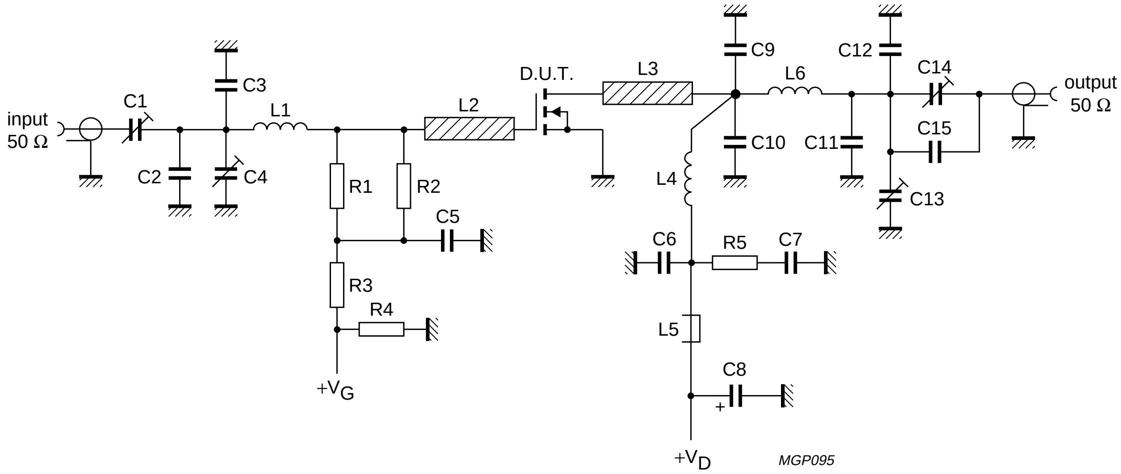


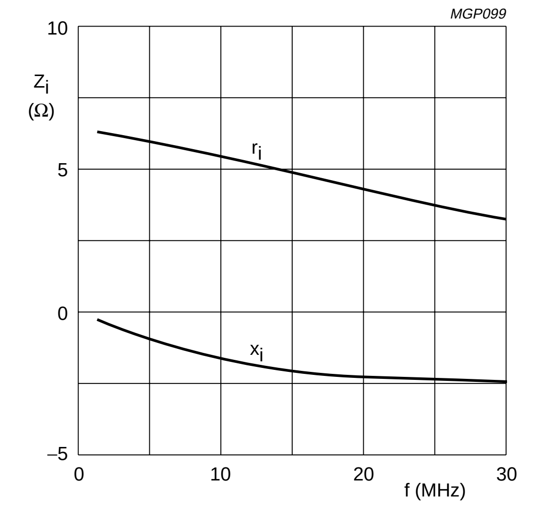
Fig.13 Test circuit for class-AB operation.

List of components class-AB test circuit (see Fig.13)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C4, C13, C14	film dielectric trimmer	7 to 100 pF		2222 809 07015
C2	multilayer ceramic chip capacitor (note 1)	56 pF		
C3, C11	multilayer ceramic chip capacitor (note 1)	62 pF		
C5, C6	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C7	multilayer ceramic chip capacitor	3 × 100 nF		2222 852 47104
C8	electrolytic capacitor	2.2 μF, 63 V		
C9, C10	multilayer ceramic chip capacitor (note 1)	20 pF		
C12	multilayer ceramic chip capacitor (note 1)	100 pF		
C15	multilayer ceramic chip capacitor (note 1)	150 pF		
L1	5 turns enamelled 0.7 mm copper wire	133 nH	length 4.5 mm; int. dia. 6 mm; leads 2 × 5 mm	
L2, L3	stripline (note 2)	41.1 Ω	length 13 × 6 mm	
L4	7 turns enamelled 1.5 mm copper wire	236 nH	length 12.5 mm; int. dia. 8 mm; leads 2 × 5 mm	
L5	grade 3B Ferroxcube wideband HF choke			4312 020 36642
L6	5 turns enamelled 2 mm copper wire	170 nH	length 11.5 mm; int. dia. 8 mm; leads 2 × 5 mm	
R1, R2	metal film resistor	10 Ω, 1 W		
R2	metal film resistor	10 kΩ, 0.4 W		
R3	metal film resistor	1 MΩ, 0.4 W		
R5	metal film resistor	10 kΩ, 1 W		

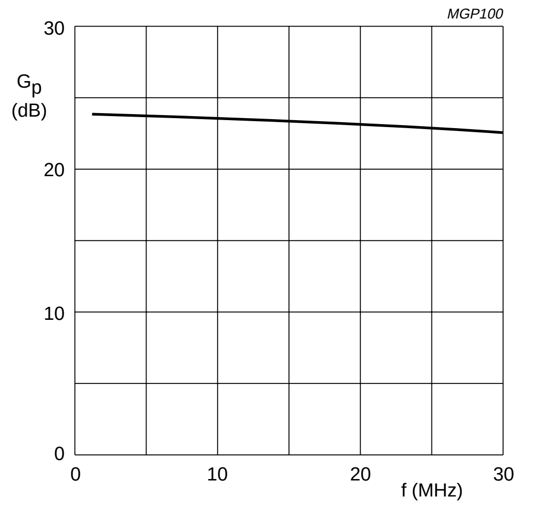
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric (ε_r = 2.2), thickness 1.6 mm (Rogers 5880).



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.7 A;
P_L = 150 W (PEP); R_{GS} = 6.25 Ω; R_L = 6.25 Ω.

Fig.14 Input impedance as a function of frequency (series components); typical values.



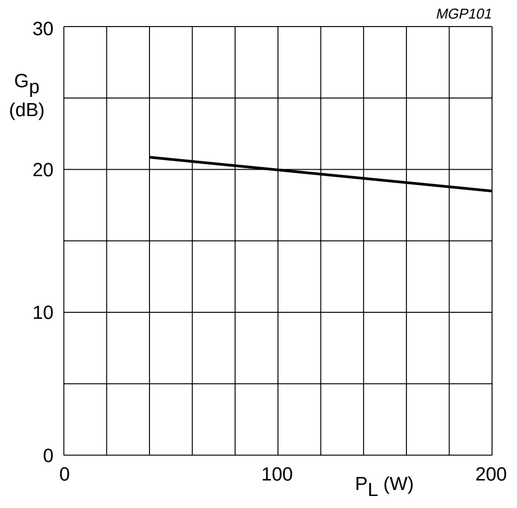
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.7 A;
P_L = 150 W (PEP); R_{GS} = 6.25 Ω; R_L = 6.25 Ω.

Fig.15 Power gain as a function of frequency; typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

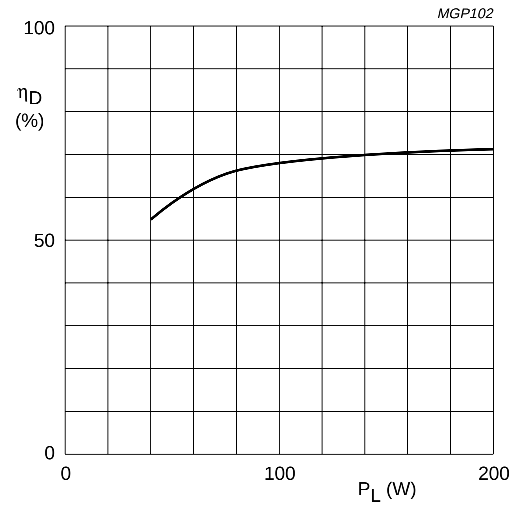
RF performance in CW operation in a common source class-B test circuit (see Fig.19).
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.2 K/W; R_{GS} = 15.8 Ω unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	108	50	0.1	150	typ. 19	typ. 70



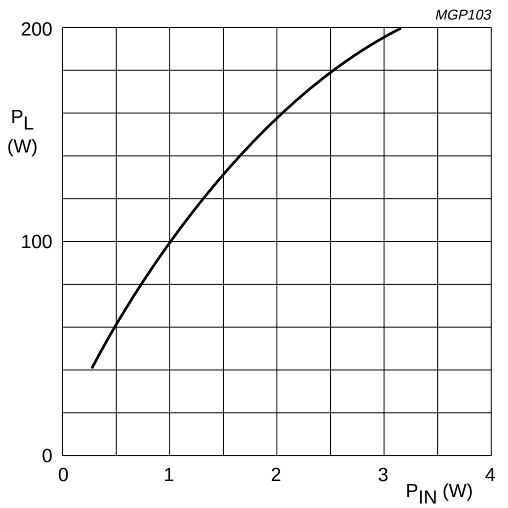
Class-B operation; V_{DS} = 50 V; I_{DQ} = 100 mA;
R_{GS} = 15.8 Ω; f = 108 MHz.

Fig.16 Power gain as a function of load power; typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 100 mA;
R_{GS} = 15.8 Ω; f = 108 MHz.

Fig.17 Two tone efficiency as a function of load power; typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 100 mA;
R_{GS} = 15.8 Ω; f = 108 MHz.

Fig.18 Load power as a function of input power; typical values.

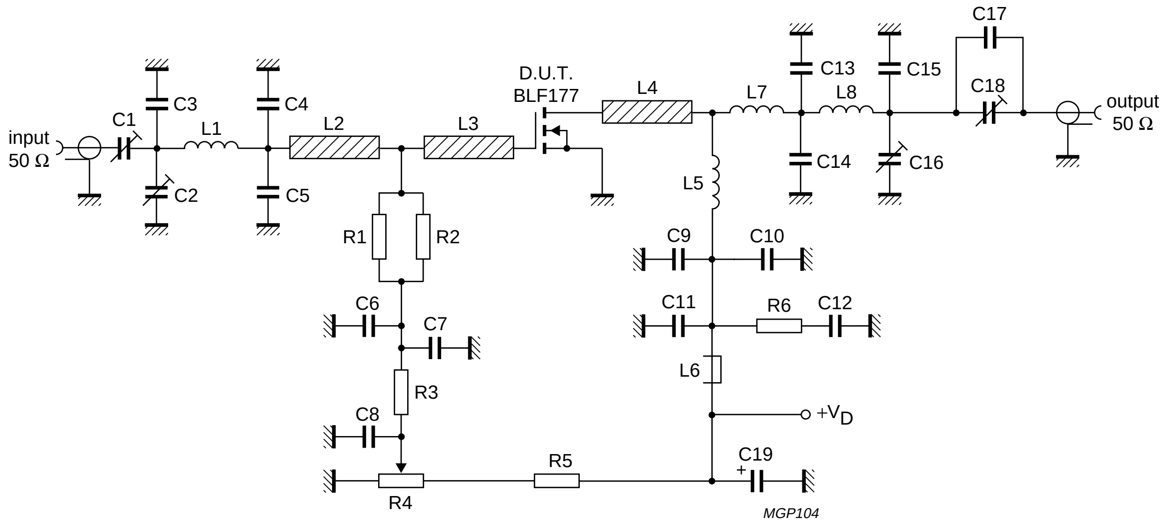


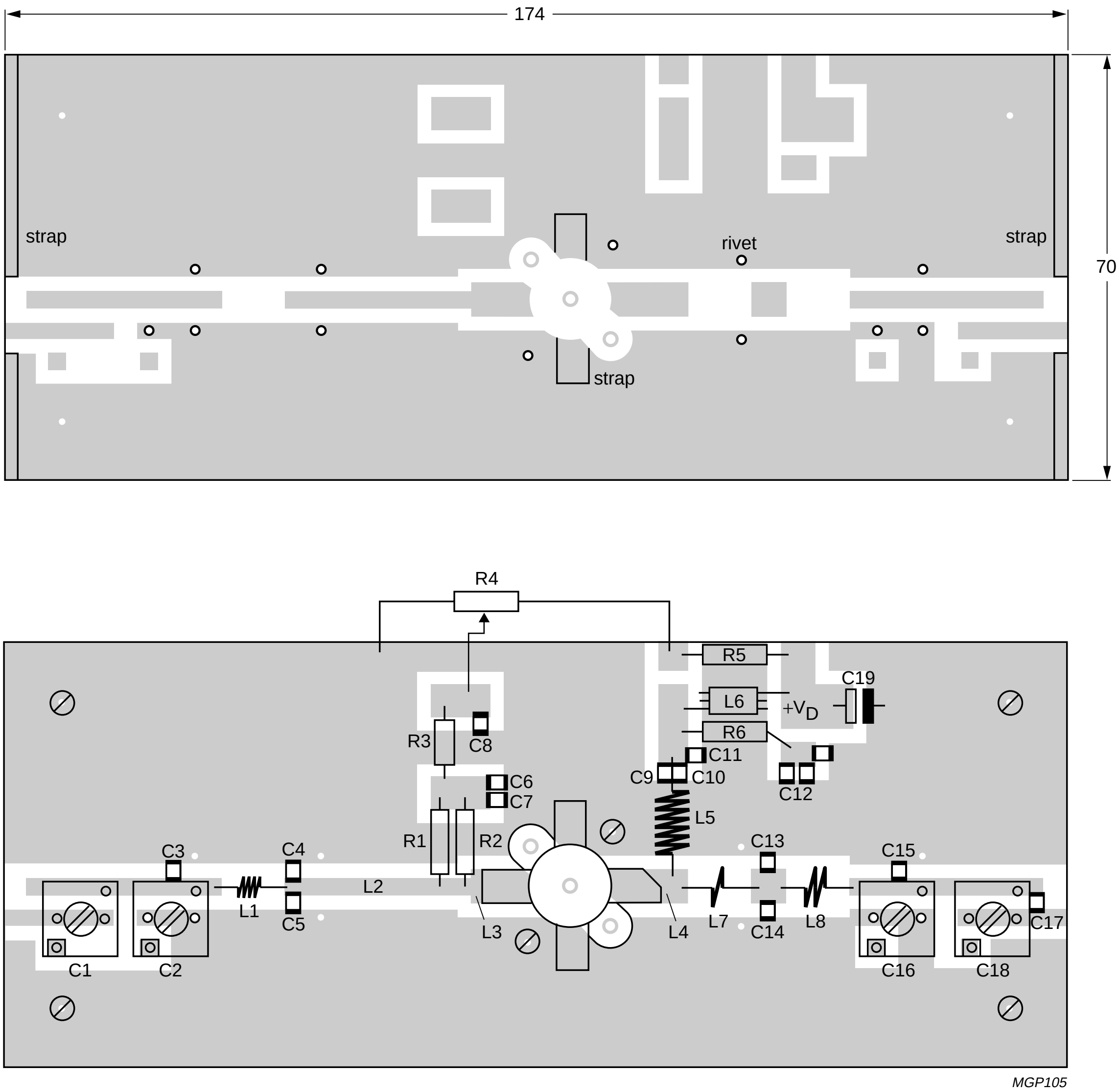
Fig.19 Test circuit for class-B operation at 108 MHz.

List of components class-B test circuit (see Fig.19)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2, C16, C18	film dielectric trimmer	2.5 to 20 pF		2222 809 07004
C3	multilayer ceramic chip capacitor (note 1)	20 pF		
C4, C5	multilayer ceramic chip capacitor (note 1)	62 pF		
C6, C7, C9, C10	multilayer ceramic chip capacitor (note 1)	1 nF		
C8	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C11	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C12	multilayer ceramic chip capacitor	3 × 100 nF		2222 852 47104
C13, C14	multilayer ceramic chip capacitor (note 1)	36 pF		
C15	multilayer ceramic chip capacitor (note 1)	12 pF		
C17	multilayer ceramic chip capacitor (note 1)	5.6 pF		
C19	electrolytic capacitor	4.4 μF, 63 V		2222 030 28478
L1	3 turns enamelled 0.8 mm copper wire	22 nH	length 5.5 mm; int. dia. 3 mm; leads 2 × 5 mm	
L2	stripline (note 2)	64.7 Ω	31 × 3 mm	
L3, L4	stripline (note 2)	41.1 Ω	10 × 6 mm	
L5	6 turns enamelled 1.6 mm copper wire	122 nH	length 13.8 mm; int. dia. 6 mm; leads 2 × 5 mm	
L6	grade 3B Ferroxcube wideband HF choke			4312 020 36642
L7	1 turn enamelled 1.6 mm copper wire	16.5 nH	int. dia. 9 mm; leads 2 × 5 mm	
L8	2 turns enamelled 1.6 mm copper wire	34.4 nH	length 3.9 mm; int. dia. 6 mm; leads 2 × 5 mm	
R1, R2	metal film resistor	31.6 Ω, 1 W		
R3	metal film resistor	1 kΩ, 0.4 W		
R4	cermet potentiometer	5 kΩ		
R5	metal film resistor	44.2 kΩ, 0.4 W		
R6	metal film resistor	10 Ω, 1 W		

Notes

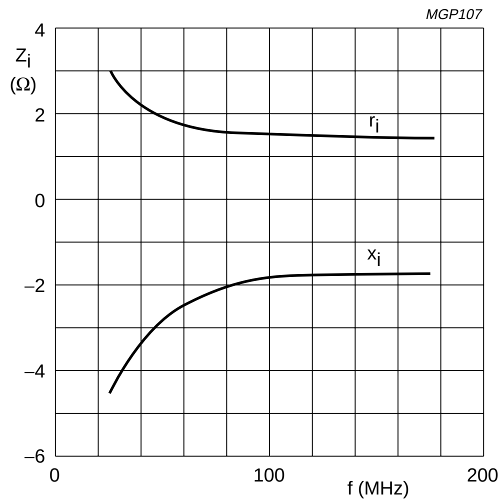
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric (ε_r = 2.2), thickness 1.6 mm (Rogers 5880).



Dimensions in mm.

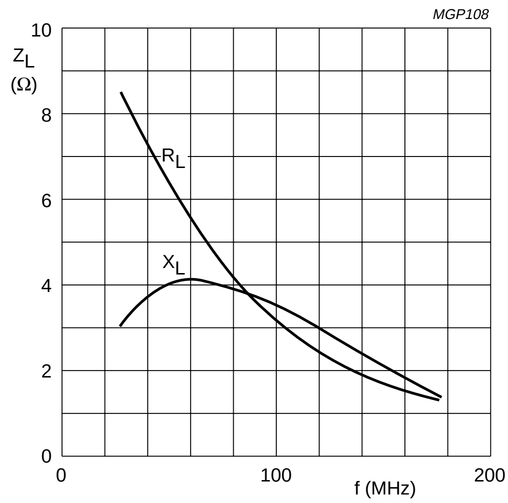
The circuit and components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized to serve as a ground. Earth connections are made by means of hollow rivets, whilst under the source leads and at the input and output copper straps are used for a direct contact between upper and lower sheets.

Fig.20 Component layout for 108 MHz class-B test circuit.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 0.1 A;
P_L = 150 W; R_{GS} = 15 Ω.

Fig.21 Input impedance as a function of frequency (series components); typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 0.1 A;
P_L = 150 W; R_{GS} = 15 Ω.

Fig.22 Load impedance as a function of frequency (series components); typical values.

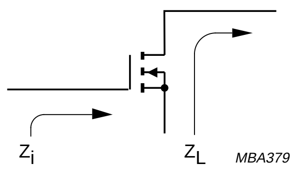
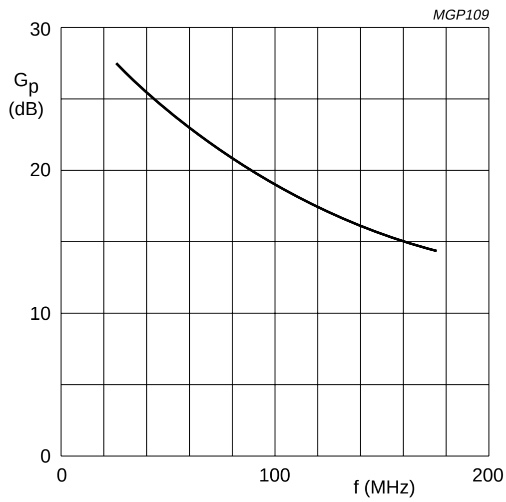


Fig.23 Definition of transistor impedance.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 0.1 A;
P_L = 150 W; R_{GS} = 15 Ω.

Fig.24 Power gain as a function of frequency; typical values.

BLF177 scattering parameters

V_{DS} = 50 V; I_D = 100 mA; note 1.

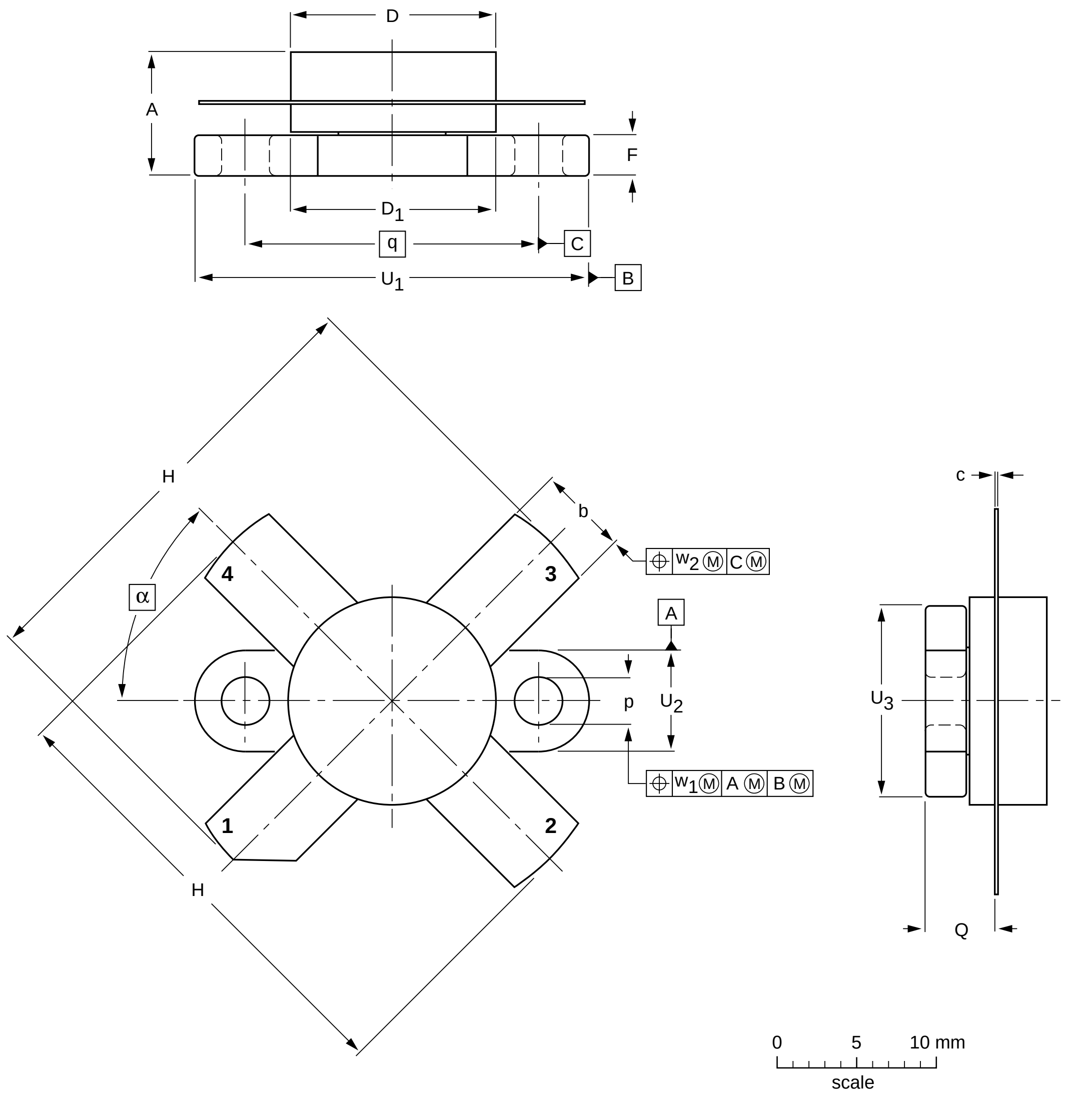
f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	$\|s_{11}\|$	∠ Φ	$\|s_{21}\|$	∠ Φ	$\|s_{12}\|$	∠ Φ	$\|s_{22}\|$	∠ Φ
5	0.86	–110.20	36.90	114.20	0.02	25.20	0.64	–84.90
10	0.83	–139.40	20.39	93.30	0.02	5.10	0.55	–112.00
20	0.85	–155.70	9.82	72.60	0.02	–13.40	0.60	–129.30
30	0.88	–161.50	5.96	59.30	0.02	–24.70	0.69	–138.00
40	0.90	–164.90	3.98	49.30	0.02	–31.70	0.76	–144.30
50	0.92	–167.10	2.83	41.90	0.01	–35.80	0.82	–149.30
60	0.94	–169.00	2.11	36.00	0.01	–36.80	0.86	–153.50
70	0.96	–170.70	1.63	31.20	0.01	–33.70	0.89	–157.00
80	0.96	–172.20	1.29	27.40	0.00	–23.00	0.91	–159.90
90	0.97	–173.40	1.04	24.20	0.00	3.30	0.92	–162.40
100	0.97	–174.30	0.86	21.70	0.00	42.50	0.94	–164.50
125	0.99	–176.50	0.57	16.40	0.01	81.60	0.95	–168.80
150	0.99	–178.10	0.40	13.40	0.01	88.70	0.97	–171.90
175	0.99	–179.80	0.30	11.60	0.02	90.70	0.98	–174.50
200	1.00	179.20	0.23	11.00	0.02	90.80	0.98	–176.70
250	1.00	177.00	0.15	11.70	0.03	90.50	0.99	179.80
300	1.00	175.10	0.11	16.70	0.03	89.60	0.99	176.90
350	0.99	173.30	0.08	24.10	0.04	88.30	0.99	174.30
400	1.00	171.80	0.07	33.10	0.05	88.00	0.99	171.90
450	0.99	170.10	0.07	42.70	0.05	87.80	0.99	169.60
500	0.99	168.50	0.07	51.90	0.06	86.50	0.99	167.40
600	0.99	165.40	0.07	64.20	0.07	84.90	0.99	163.10
700	0.99	162.30	0.09	70.60	0.09	83.10	0.98	158.90
800	0.99	158.90	0.10	73.80	0.10	82.20	0.98	154.80
900	0.99	155.30	0.12	74.90	0.12	80.70	0.97	150.60
1000	0.98	151.80	0.14	76.40	0.14	79.80	0.97	146.20

Note

1. For more extensive s-parameters see internet website: http://www.semiconductors.philips.com.markets/communications/wirelesscommunicationms/broadcast

PACKAGE OUTLINE

Flanged ceramic package; 2 mounting holes; 4 leads | **SOT121B**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	F	H	p	Q	q	U_1	U_2	U_3	w_1	w_2	α
mm	7.27 6.17	5.82 5.56	0.16 0.10	12.86 12.59	12.83 12.57	2.67 2.41	28.45 25.52	3.30 3.05	4.45 3.91	18.42	24.90 24.63	6.48 6.22	12.32 12.06	0.25	0.51	45°
inches	0.286 0.243	0.229 0.219	0.006 0.004	0.506 0.496	0.505 0.495	0.105 0.095	1.120 1.005	0.130 0.120	0.175 0.154	0.725	0.98 0.97	0.255 0.245	0.485 0.475	0.01	0.02	

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT121B						99-03-29

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contact information

For additional information, please visit: **http://www.nxp.com**

For sales office addresses, send an email to: **salesaddresses@nxp.com**

Revision history

Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF177_N_6	20070124	Product data sheet	-	BLF177_5
Modifications:	• correction made to figure title of Fig.13 • correction made to note 2 on page 9 • correction made to note 2 on page 13 • correction made to figure note of Fig.20			
BLF177_5 (9397 750 14416)	20041217	Product specification	-	BLF177_4
BLF177_4 (9397 750 11579)	20030721	Product specification	-	BLF177_3
BLF177_3 (9397 750 04059)	19980702	Product specification	-	BLF177_CNV_2
BLF177_CNV_2 (9397 750 xxxxx)	19971216	Product specification	-	-

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 24 January 2007
Document identifier: BLF177_N_6