

# 74AVC4T245-Q100

4-bit dual supply translating transceiver with configurable voltage translation; 3-state

Rev. 6 — 11 April 2024

Product data sheet

## 1. General description

The 74AVC4T245-Q100 is an 4-bit, dual supply transceiver that enables bidirectional level translation. The device can be used as two 2-bit transceivers or as a 4-bit transceiver. It features four 2-bit input-output ports (nAn and nBn), a direction control input (nDIR), an output enable input (nOE) and dual supply pins ( $V_{CC(A)}$  and  $V_{CC(B)}$ ). Both  $V_{CC(A)}$  and  $V_{CC(B)}$  can be supplied at any voltage between 0.8 V and 3.6 V making the device suitable for translating between any of the low voltage nodes (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V). Pins nAn, nOE and nDIR are referenced to  $V_{CC(A)}$  and pins nBn are referenced to  $V_{CC(B)}$ . A HIGH on nDIR allows transmission from nAn to nBn and a LOW on nDIR allows transmission from nBn to nAn. The output enable input (nOE) can be used to disable the outputs so the buses are effectively isolated. The device is fully specified for partial power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either  $V_{CC(A)}$  or  $V_{CC(B)}$  are at GND level, both nAn and nBn are in the high-impedance OFF-state.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range:  $V_{CC(A)}$ : 0.8 V to 3.6 V;  $V_{CC(B)}$ : 0.8 V to 3.6 V
- Complies with JEDEC standards:
  - JESD8-12 (0.8 V to 1.3 V)
  - JESD8-11 (0.9 V to 1.65 V)
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8-B (2.7 V to 3.6 V)
- Maximum data rates:
  - 380 Mbit/s ( $\geq$  1.8 V to 3.3 V translation)
  - 200 Mbit/s ( $\geq$  1.1 V to 3.3 V translation)
  - 200 Mbit/s ( $\geq$  1.1 V to 2.5 V translation)
  - 200 Mbit/s ( $\geq$  1.1 V to 1.8 V translation)
  - 150 Mbit/s ( $\geq$  1.1 V to 1.5 V translation)
  - 100 Mbit/s ( $\geq$  1.1 V to 1.2 V translation)
- Suspend mode
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 3B exceeds 8000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

### 3. Ordering information

Table 1. Ordering information

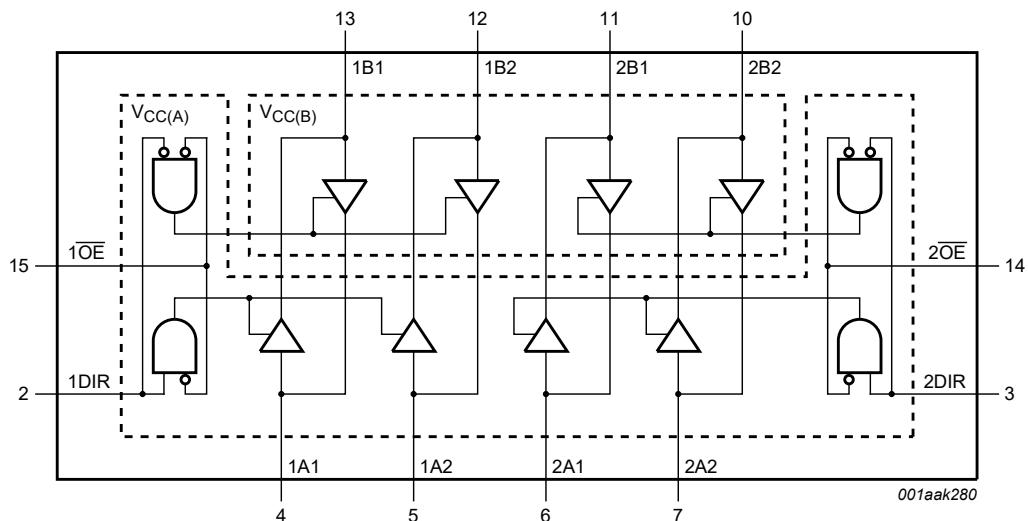
Type number	Package				Version
	Temperature range	Name	Description		
<a href="#">74AVC4T245D-Q100</a>	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm		<a href="#">SOT109-1</a>
<a href="#">74AVC4T245PW-Q100</a>	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm		<a href="#">SOT403-1</a>
<a href="#">74AVC4T245BQ-Q100</a>	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm		<a href="#">SOT763-1</a>
<a href="#">74AVC4T245GU-Q100</a>	-40 °C to +125 °C	XQFN16	plastic, extremely thin quad flat package; no leads; 16 terminals; body 1.80 × 2.60 × 0.50 mm		<a href="#">SOT1161-1</a>

### 4. Marking

Table 2. Marking codes

Type number	Marking code
74AVC4T245D-Q100	74AVC4T245D
74AVC4T245PW-Q100	VC4T245
74AVC4T245BQ-Q100	C4T245
74AVC4T245GU-Q100	BT5

### 5. Functional diagram



Pin numbers are shown for SO16, TSSOP16 and DHVQFN16 packages only.

Fig. 1. Logic symbol

4-bit dual supply translating transceiver with configurable voltage translation; 3-state

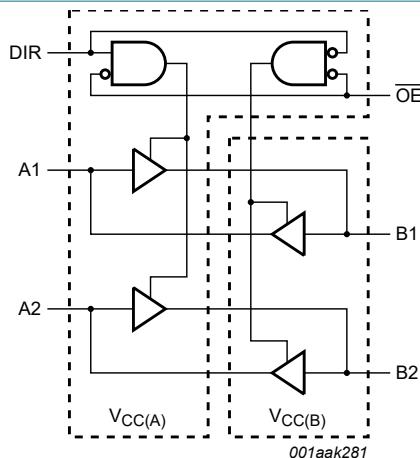


Fig. 2. Logic diagram (one 2-bit transceiver)

## 6. Pinning information

### 6.1. Pinning

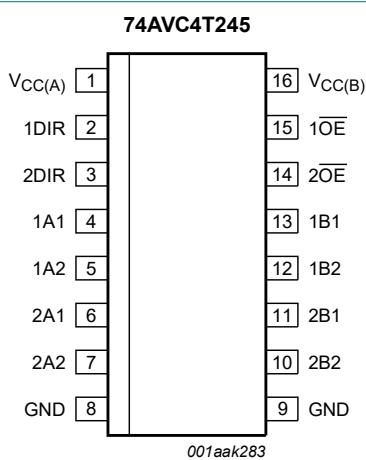


Fig. 3. Pin configuration SOT109-1 (SO16)

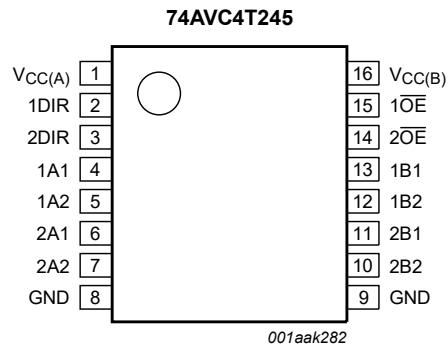
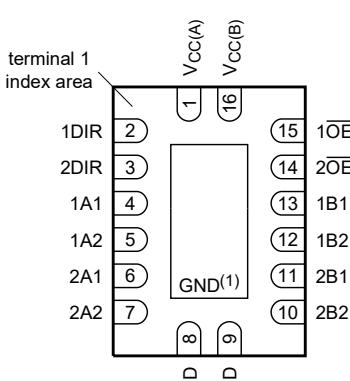
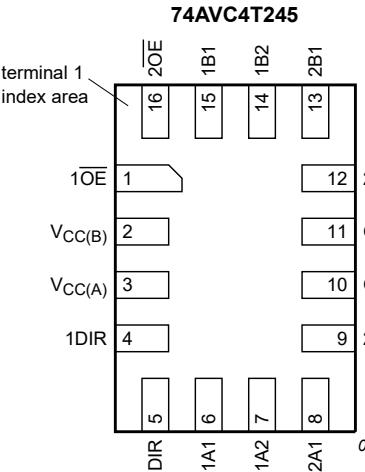


Fig. 4. Pin configuration SOT403-1 (TSSOP16)

74AVC4T245		74AVC4T245	
 Transparent top view	(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.	 Transparent top view	
Fig. 5. Pin configuration SOT763-1 (DHVQFN16)		Fig. 6. Pin configuration SOT1161-1 (XQFN16)	

## 6.2. Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT109-1, SOT403-1 and SOT763-1	SOT1161-1	
V <sub>CC(A)</sub>	1	3	supply voltage A (nAn, n $\overline{OE}$ and nDIR inputs are referenced to V <sub>CC(A)</sub> )
1DIR, 2DIR	2, 3	4, 5	direction control
1A1, 1A2	4, 5	6, 7	data input or output
2A1, 2A2	6, 7	8, 9	data input or output
GND[1]	8, 9	10, 11	ground (0 V)
2B2, 2B1	10, 11	12, 13	data input or output
1B2, 1B1	12, 13	14, 15	data input or output
2 $\overline{OE}$ , 1 $\overline{OE}$	14, 15	16, 1	output enable input (active LOW)
V <sub>CC(B)</sub>	16	2	supply voltage B (nBn inputs are referenced to V <sub>CC(B)</sub> )

[1] All GND pins must be connected to ground (0 V).

## 7. Functional description

**Table 4. Function table**

*H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.*

Supply voltage	Input	Input/output[1]	
$V_{CC(A)}, V_{CC(B)}$	$nOE$ [2]	$nDIR$ [2]	$nAn$ [2]
0.8 V to 3.6 V	L	L	$nAn = nBn$
0.8 V to 3.6 V	L	H	input
0.8 V to 3.6 V	H	X	Z
GND[1]	X	X	Z

[1] If at least one of  $V_{CC(A)}$  or  $V_{CC(B)}$  is at GND level, the device goes into suspend mode.

[2] The  $nAn$ ,  $nDIR$  and  $nOE$  input circuit is referenced to  $V_{CC(A)}$ ; The  $nBn$  input circuit is referenced to  $V_{CC(B)}$ .

## 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{CC(A)}$	supply voltage A		-0.5	+4.6	V	
$V_{CC(B)}$	supply voltage B		-0.5	+4.6	V	
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA	
$V_I$	input voltage		[1]	-0.5	+4.6	V
$I_{ok}$	output clamping current	$V_O < 0$ V	-50	-	mA	
$V_O$	output voltage	Active mode [1] [2] [3]	-0.5	$V_{CCO} + 0.5$	V	
		Suspend or 3-state mode [1]	-0.5	+4.6	V	
$I_O$	output current	$V_O = 0$ V to $V_{CCO}$ [2]	-	$\pm 50$	mA	
$I_{CC}$	supply current	per $V_{CC(A)}$ or $V_{CC(B)}$ pin	-	100	mA	
$I_{GND}$	ground current	per GND pin	-100	-	mA	
$T_{stg}$	storage temperature		-65	+150	°C	
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C				
		SOT109-1; SOT403-1; SOT763-1 [4]	-	500	mW	
		SOT1161-1	-	250	mW	

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2]  $V_{CCO}$  is the supply voltage associated with the output port.

[3]  $V_{CCO} + 0.5$  V should not exceed 4.6 V.

[4] For SOT109-1 (SO16) package:  $P_{tot}$  derates linearly with 12.4 mW/K above 110 °C.

For SOT403-1 (TSSOP16) package:  $P_{tot}$  derates linearly with 8.5 mW/K above 91 °C.

For SOT763-1 (DHVQFN16) package:  $P_{tot}$  derates linearly with 11.2 mW/K above 106 °C.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		0.8	3.6	V
$V_{CC(B)}$	supply voltage B		0.8	3.6	V
$V_I$	input voltage		0	3.6	V
$V_O$	output voltage	Active mode [1]	0	$V_{CCO}$	V
		Suspend or 3-state mode	0	3.6	V
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CCI} = 0.8 \text{ V to } 3.6 \text{ V}$	[2]	-	5 ns/V

[1]  $V_{CCO}$  is the supply voltage associated with the output port.

[2]  $V_{CCI}$  is the supply voltage associated with the input port.

## 10. Static characteristics

**Table 7. Typical static characteristics at  $T_{amb} = 25 \text{ °C}$**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V). [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -1.5 \text{ mA}; V_{CC(A)} = V_{CC(B)} = 0.8 \text{ V}$	-	0.69	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 1.5 \text{ mA}; V_{CC(A)} = V_{CC(B)} = 0.8 \text{ V}$	-	0.07	-	V
$I_I$	input leakage current	nDIR, nOE input; $V_I = 0 \text{ V or } 3.6 \text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 0.8 \text{ V to } 3.6 \text{ V}$	-	$\pm 0.025$	$\pm 0.25$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	A or B port; $V_O = 0 \text{ V or } V_{CCO}$ ; $V_{CC(A)} = V_{CC(B)} = 3.6 \text{ V}$	[2]	-	$\pm 0.5$	$\pm 2.5 \mu\text{A}$
		suspend mode A port; $V_O = 0 \text{ V or } V_{CCO}$ ; $V_{CC(A)} = 3.6 \text{ V}; V_{CC(B)} = 0 \text{ V}$	[2]	-	$\pm 0.5$	$\pm 2.5 \mu\text{A}$
		suspend mode B port; $V_O = 0 \text{ V or } V_{CCO}$ ; $V_{CC(A)} = 0 \text{ V}; V_{CC(B)} = 3.6 \text{ V}$	[2]	-	$\pm 0.5$	$\pm 2.5 \mu\text{A}$
$I_{OFF}$	power-off leakage current	A port; $V_I$ or $V_O = 0 \text{ V to } 3.6 \text{ V}$ ; $V_{CC(A)} = 0 \text{ V}$ ; $V_{CC(B)} = 0.8 \text{ V to } 3.6 \text{ V}$	-	$\pm 0.1$	$\pm 1$	$\mu\text{A}$
		B port; $V_I$ or $V_O = 0 \text{ V to } 3.6 \text{ V}$ ; $V_{CC(B)} = 0 \text{ V}$ ; $V_{CC(A)} = 0.8 \text{ V to } 3.6 \text{ V}$	-	$\pm 0.1$	$\pm 1$	$\mu\text{A}$
$C_I$	input capacitance	nDIR, nOE input; $V_I = 0 \text{ V or } 3.3 \text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 3.3 \text{ V}$	-	1.0	-	pF
$C_{I/O}$	input/output capacitance	A and B port; $V_O = 3.3 \text{ V or } 0 \text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 3.3 \text{ V}$	-	4.0	-	pF

[1]  $V_{CCO}$  is the supply voltage associated with the output port;  $V_{CCI}$  is the supply voltage associated with the data input port.

[2] For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

## 4-bit dual supply translating transceiver with configurable voltage translation; 3-state

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).<sup>[1]</sup>

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	data input					
		V <sub>CCI</sub> = 0.8 V	0.70V <sub>CCI</sub>	-	0.70V <sub>CCI</sub>	-	V
		V <sub>CCI</sub> = 1.1 V to 1.95 V	0.65V <sub>CCI</sub>	-	0.65V <sub>CCI</sub>	-	V
		V <sub>CCI</sub> = 2.3 V to 2.7 V	1.6	-	1.6	-	V
		V <sub>CCI</sub> = 3.0 V to 3.6 V	2	-	2	-	V
		nDIR, nOE input					
		V <sub>CC(A)</sub> = 0.8 V	0.70V <sub>CC(A)</sub>	-	0.70V <sub>CC(A)</sub>	-	V
		V <sub>CC(A)</sub> = 1.1 V to 1.95 V	0.65V <sub>CC(A)</sub>	-	0.65V <sub>CC(A)</sub>	-	V
		V <sub>CC(A)</sub> = 2.3 V to 2.7 V	1.6	-	1.6	-	V
		V <sub>CC(A)</sub> = 3.0 V to 3.6 V	2	-	2	-	V
V <sub>IL</sub>	LOW-level input voltage	data input					
		V <sub>CCI</sub> = 0.8 V	-	0.30V <sub>CCI</sub>	-	0.30V <sub>CCI</sub>	V
		V <sub>CCI</sub> = 1.1 V to 1.95 V	-	0.35V <sub>CCI</sub>	-	0.35V <sub>CCI</sub>	V
		V <sub>CCI</sub> = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		V <sub>CCI</sub> = 3.0 V to 3.6 V	-	0.8	-	0.8	V
		nDIR, nOE input					
		V <sub>CC(A)</sub> = 0.8 V	-	0.30V <sub>CC(A)</sub>	-	0.30V <sub>CC(A)</sub>	V
		V <sub>CC(A)</sub> = 1.1 V to 1.95 V	-	0.35V <sub>CC(A)</sub>	-	0.35V <sub>CC(A)</sub>	V
		V <sub>CC(A)</sub> = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		V <sub>CC(A)</sub> = 3.0 V to 3.6 V	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>O</sub> = -100 $\mu$ A; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	V <sub>CCO</sub> - 0.1	-	V <sub>CCO</sub> - 0.1	-	V
		I <sub>O</sub> = -3 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.1 V	0.85	-	0.85	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.4 V	1.05	-	1.05	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.65 V	1.2	-	1.2	-	V
		I <sub>O</sub> = -9 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.3 V	1.75	-	1.75	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.0 V	2.3	-	2.3	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>O</sub> = 100 $\mu$ A; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	0.1	-	0.1	V
		I <sub>O</sub> = 3 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.1 V	-	0.25	-	0.25	V
		I <sub>O</sub> = 6 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.4 V	-	0.35	-	0.35	V
		I <sub>O</sub> = 8 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.65 V	-	0.45	-	0.45	V
		I <sub>O</sub> = 9 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.3 V	-	0.55	-	0.55	V
		I <sub>O</sub> = 12 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.0 V	-	0.7	-	0.7	V
I <sub>I</sub>	input leakage current	nDIR, nOE input; V <sub>I</sub> = 0 V or 3.6 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	$\pm$ 1	-	$\pm$ 5	$\mu$ A

## 4-bit dual supply translating transceiver with configurable voltage translation; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I <sub>OZ</sub>	OFF-state output current	A or B port; V <sub>O</sub> = 0 V or V <sub>CC0</sub> ; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.6 V [2]	-	±5	-	±30	μA
		suspend mode A port; V <sub>O</sub> = 0 V or V <sub>CC0</sub> ; V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V [2]	-	±5	-	±30	μA
		suspend mode B port; V <sub>O</sub> = 0 V or V <sub>CC0</sub> ; V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V [2]	-	±5	-	±30	μA
I <sub>OFF</sub>	power-off leakage current	A port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	±5	-	±30	μA
		B port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC(B)</sub> = 0 V; V <sub>CC(A)</sub> = 0.8 V to 3.6 V	-	±5	-	±30	μA
I <sub>CC</sub>	supply current	A port; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; I <sub>O</sub> = 0 A					
		V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	10	-	55	μA
		V <sub>CC(A)</sub> = 1.1 V to 3.6 V; V <sub>CC(B)</sub> = 1.1 V to 3.6 V	-	8	-	50	μA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-	8	-	50	μA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V	-2	-	-12	-	μA
		B port; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; I <sub>O</sub> = 0 A					
		V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	10	-	55	μA
		V <sub>CC(A)</sub> = 1.1 V to 3.6 V; V <sub>CC(B)</sub> = 1.1 V to 3.6 V	-	8	-	50	μA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-2	-	-12	-	μA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V	-	8	-	50	μA
		A plus B port (I <sub>CC(A)</sub> + I <sub>CC(B)</sub> ); I <sub>O</sub> = 0 A; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	20	-	70	μA
		A plus B port (I <sub>CC(A)</sub> + I <sub>CC(B)</sub> ); I <sub>O</sub> = 0 A; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; V <sub>CC(A)</sub> = 1.1 V to 3.6 V; V <sub>CC(B)</sub> = 1.1 V to 3.6 V	-	16	-	65	μA

[1] V<sub>CC0</sub> is the supply voltage associated with the output port; V<sub>CCI</sub> is the supply voltage associated with the data input port.

[2] For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

Table 9. Typical total supply current (I<sub>CC(A)</sub> + I<sub>CC(B)</sub>)

V <sub>CC(A)</sub>	V <sub>CC(B)</sub>								Unit
		0 V	0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	0.1	0.1	0.1	0.1	0.1	0.1	0.1	μA
0.8 V	0.1	0.1	0.1	0.1	0.1	0.3	1.6	μA	
1.2 V	0.1	0.1	0.1	0.1	0.1	0.1	0.8	μA	
1.5 V	0.1	0.1	0.1	0.1	0.1	0.1	0.4	μA	
1.8 V	0.1	0.1	0.1	0.1	0.1	0.1	0.2	μA	
2.5 V	0.1	0.3	0.1	0.1	0.1	0.1	0.1	μA	
3.3 V	0.1	1.6	0.8	0.4	0.2	0.1	0.1	μA	

## 11. Dynamic characteristics

**Table 10. Typical power dissipation capacitance at  $V_{CC(A)} = V_{CC(B)}$  and  $T_{amb} = 25^\circ C$**

Voltages are referenced to GND (ground = 0 V). [1] [2]

Symbol	Parameter	Conditions	$V_{CC(A)} = V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$C_{PD}$	power dissipation capacitance	A port: (direction nAn to nBn); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction nAn to nBn); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction nBn to nAn); output enabled	9.5	9.7	9.8	9.9	10.7	11.9	pF
		A port: (direction nBn to nAn); output disabled	0.6	0.6	0.6	0.6	0.7	0.7	pF
		B port: (direction nAn to nBn); output enabled	9.5	9.7	9.8	9.9	10.7	11.9	pF
		B port: (direction nAn to nBn); output disabled	0.6	0.6	0.6	0.6	0.7	0.7	pF
		B port: (direction nBn to nAn); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		B port: (direction nBn to nAn); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF

[1]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

[2]  $f_i = 10$  MHz;  $V_i = \text{GND}$  to  $V_{CC}$ ;  $t_r = t_f = 1$  ns;  $C_L = 0$  pF;  $R_L = \infty \Omega$ .

## 4-bit dual supply translating transceiver with configurable voltage translation; 3-state

**Table 11. Typical dynamic characteristics at  $V_{CC(A)} = 0.8$  V and  $T_{amb} = 25$  °C**Voltages are referenced to GND (ground = 0 V); for test circuit see [Fig. 9](#); for waveforms see [Fig. 7](#) and [Fig. 8.\[1\]](#)

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$t_{pd}$	propagation delay	nAn to nBn	14.5	7.3	6.5	6.2	5.9	6.0	ns
		nBn to nAn	14.5	12.7	12.4	12.3	12.1	12.0	ns
$t_{dis}$	disable time	nOE to nAn	14.3	14.3	14.3	14.3	14.3	14.3	ns
		nOE to nBn	17.0	9.9	9.0	9.4	9.0	9.7	ns
$t_{en}$	enable time	nOE to nAn	18.2	18.2	18.2	18.2	18.2	18.2	ns
		nOE to nBn	19.2	10.7	9.8	9.6	9.7	10.2	ns

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .**Table 12. Typical dynamic characteristics at  $V_{CC(B)} = 0.8$  V and  $T_{amb} = 25$  °C**Voltages are referenced to GND (ground = 0 V); for test circuit see [Fig. 9](#); for waveforms see [Fig. 7](#) and [Fig. 8.\[1\]](#)

Symbol	Parameter	Conditions	$V_{CC(A)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$t_{pd}$	propagation delay	nAn to nBn	14.5	12.7	12.4	12.3	12.1	12.0	ns
		nBn to nAn	14.5	7.3	6.5	6.2	5.9	6.0	ns
$t_{dis}$	disable time	nOE to nAn	14.3	5.5	4.1	4.0	3.0	3.5	ns
		nOE to nBn	17.0	13.8	13.4	13.1	12.9	12.7	ns
$t_{en}$	enable time	nOE to nAn	18.2	5.6	4.0	3.2	2.4	2.2	ns
		nOE to nBn	19.2	14.6	14.1	13.9	13.7	13.6	ns

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

## 4-bit dual supply translating transceiver with configurable voltage translation; 3-state

Table 13. Dynamic characteristics for temperature range  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ 

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9; for waveforms see Fig. 7 and Fig. 8.[1]

Symbol	Parameter	Conditions	V <sub>CC(B)</sub>										Unit	
			1.2 V $\pm$ 0.1 V		1.5 V $\pm$ 0.1 V		1.8 V $\pm$ 0.15 V		2.5 V $\pm$ 0.2 V		3.3 V $\pm$ 0.3 V			
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
<b>V<sub>CC(A)</sub> = 1.1 V to 1.3 V</b>														
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	9.4	0.5	7.1	0.5	6.2	0.5	5.2	0.5	5.1	ns	
		nBn to nAn	0.5	9.4	0.5	8.9	0.5	8.7	0.5	8.4	0.5	8.2	ns	
t <sub>dis</sub>	disable time	nOE to nAn	1.8	10.9	1.8	10.9	1.8	10.9	1.8	10.9	1.8	10.9	ns	
		nOE to nBn	1.9	12.4	1.9	9.6	1.9	9.5	1.4	8.1	1.2	9.1	ns	
t <sub>en</sub>	enable time	nOE to nAn	1.4	12.8	1.4	12.8	1.4	12.8	1.4	12.8	1.4	12.8	ns	
		nOE to nBn	1.1	13.3	1.1	10.0	1.1	8.9	1.0	7.9	1.0	7.7	ns	
<b>V<sub>CC(A)</sub> = 1.4 V to 1.6 V</b>														
t <sub>pd</sub>	propagation delay	nAn to nBn	0.3	8.9	0.3	6.3	0.3	5.2	0.3	4.2	0.3	4.2	ns	
		nBn to nAn	0.7	7.1	0.7	6.3	0.5	6.0	0.4	5.7	0.3	5.6	ns	
t <sub>dis</sub>	disable time	nOE to nAn	1.8	10.2	1.8	10.2	1.5	10.2	1.3	10.2	1.6	10.2	ns	
		nOE to nBn	1.9	11.3	1.9	10.3	1.9	9.1	1.4	7.4	1.2	7.6	ns	
t <sub>en</sub>	enable time	nOE to nAn	1.1	9.4	1.4	9.4	1.1	9.4	0.7	9.4	0.4	9.4	ns	
		nOE to nBn	1.4	12.1	1.4	9.6	1.1	7.7	0.9	5.8	0.9	5.6	ns	
<b>V<sub>CC(A)</sub> = 1.65 V to 1.95 V</b>														
t <sub>pd</sub>	propagation delay	nAn to nBn	0.1	8.7	0.1	6.0	0.1	4.9	0.1	3.9	0.3	3.9	ns	
		nBn to nAn	0.6	6.2	0.6	5.3	0.5	4.9	0.3	4.6	0.3	4.5	ns	
t <sub>dis</sub>	disable time	nOE to nAn	1.8	8.6	1.6	8.6	1.8	8.6	1.3	8.6	1.6	8.6	ns	
		nOE to nBn	1.7	10.9	1.7	9.9	1.6	8.7	1.2	6.9	1.0	6.9	ns	
t <sub>en</sub>	enable time	nOE to nAn	1.0	7.2	1.0	7.2	1.0	7.2	0.6	7.2	0.4	7.2	ns	
		nOE to nBn	1.2	11.7	1.2	9.2	1.0	7.4	0.8	5.3	0.8	4.6	ns	
<b>V<sub>CC(A)</sub> = 2.3 V to 2.7 V</b>														
t <sub>pd</sub>	propagation delay	nAn to nBn	0.1	8.4	0.1	5.7	0.1	4.6	0.2	3.5	0.1	3.6	ns	
		nBn to nAn	0.6	5.2	0.6	4.2	0.4	3.9	0.2	3.4	0.2	3.3	ns	
t <sub>dis</sub>	disable time	nOE to nAn	1.0	6.2	1.0	6.2	1.0	6.2	1.0	6.2	1.0	6.2	ns	
		nOE to nBn	1.5	10.4	1.5	8.8	1.3	8.2	1.1	6.2	0.9	5.2	ns	
t <sub>en</sub>	enable time	nOE to nAn	0.7	4.8	0.7	4.8	0.7	4.8	0.6	4.8	0.4	4.8	ns	
		nOE to nBn	0.9	11.3	0.9	8.8	0.8	7.0	0.6	4.8	0.6	4.0	ns	
<b>V<sub>CC(A)</sub> = 3.0 V to 3.6 V</b>														
t <sub>pd</sub>	propagation delay	nAn to nBn	0.1	8.2	0.1	5.6	0.1	4.5	0.1	3.3	0.1	2.9	ns	
		nBn to nAn	0.6	5.1	0.6	4.2	0.4	3.4	0.2	3.0	0.1	2.8	ns	
t <sub>dis</sub>	disable time	nOE to nAn	0.7	5.6	0.7	5.6	0.7	5.6	0.7	5.6	0.7	5.6	ns	
		nOE to nBn	1.4	10.2	1.4	9.3	1.2	8.1	1.0	6.4	0.8	6.2	ns	
t <sub>en</sub>	enable time	nOE to nAn	0.6	3.8	0.6	3.8	0.6	3.8	0.6	3.8	0.4	3.8	ns	
		nOE to nBn	0.8	11.3	0.8	8.7	0.6	6.8	0.5	4.7	0.5	3.8	ns	

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.

## 4-bit dual supply translating transceiver with configurable voltage translation; 3-state

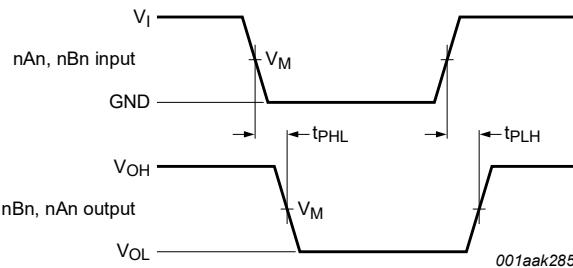
Table 14. Dynamic characteristics for temperature range  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ 

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9; for waveforms see Fig. 7 and Fig. 8.[1]

Symbol	Parameter	Conditions	V <sub>CC(B)</sub>										Unit	
			1.2 V $\pm$ 0.1 V		1.5 V $\pm$ 0.1 V		1.8 V $\pm$ 0.15 V		2.5 V $\pm$ 0.2 V		3.3 V $\pm$ 0.3 V			
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
<b>V<sub>CC(A)</sub> = 1.1 V to 1.3 V</b>														
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	10.4	0.5	7.9	0.5	6.9	0.5	5.8	0.5	5.7	ns	
		nBn to nAn	0.5	10.4	0.5	9.8	0.5	9.6	0.5	9.3	0.5	9.1	ns	
t <sub>dis</sub>	disable time	nOE to nAn	1.8	12.0	1.8	12.0	1.8	12.0	1.8	12.0	1.8	12.0	ns	
		nOE to nBn	1.9	13.7	1.9	10.6	1.9	10.5	1.4	9.0	1.2	10.1	ns	
t <sub>en</sub>	enable time	nOE to nAn	1.4	14.1	1.4	14.1	1.4	14.1	1.4	14.1	1.4	14.1	ns	
		nOE to nBn	1.1	14.7	1.1	11.0	1.1	9.8	1.0	8.7	1.0	8.5	ns	
<b>V<sub>CC(A)</sub> = 1.4 V to 1.6 V</b>														
t <sub>pd</sub>	propagation delay	nAn to nBn	0.3	9.8	0.3	7.0	0.3	5.8	0.3	4.7	0.3	4.7	ns	
		nBn to nAn	0.7	7.9	0.7	7.0	0.5	6.6	0.4	6.3	0.3	6.2	ns	
t <sub>dis</sub>	disable time	nOE to nAn	1.8	11.3	1.8	11.3	1.5	11.3	1.3	11.3	1.6	11.3	ns	
		nOE to nBn	1.9	12.5	1.9	11.4	1.9	10.1	1.4	8.2	1.2	8.4	ns	
t <sub>en</sub>	enable time	nOE to nAn	1.1	10.4	1.4	10.4	1.1	10.4	0.7	10.4	0.4	10.4	ns	
		nOE to nBn	1.4	13.3	1.4	10.6	1.1	8.5	0.9	6.4	0.9	6.2	ns	
<b>V<sub>CC(A)</sub> = 1.65 V to 1.95 V</b>														
t <sub>pd</sub>	propagation delay	nAn to nBn	0.1	9.6	0.1	6.6	0.1	5.4	0.1	4.3	0.3	4.3	ns	
		nBn to nAn	0.6	6.9	0.6	5.9	0.5	5.4	0.3	5.1	0.3	5.0	ns	
t <sub>dis</sub>	disable time	nOE to nAn	1.8	9.5	1.6	9.5	1.8	9.5	1.3	9.5	1.6	9.5	ns	
		nOE to nBn	1.7	12.0	1.7	10.9	1.6	9.6	1.2	7.6	1.0	7.6	ns	
t <sub>en</sub>	enable time	nOE to nAn	1.0	8.0	1.0	8.0	1.0	8.0	0.6	8.0	0.4	8.0	ns	
		nOE to nBn	1.2	12.9	1.2	10.2	1.0	8.2	0.8	5.9	0.8	5.1	ns	
<b>V<sub>CC(A)</sub> = 2.3 V to 2.7 V</b>														
t <sub>pd</sub>	propagation delay	nAn to nBn	0.1	9.3	0.1	6.3	0.1	5.1	0.2	4.0	0.1	4.0	ns	
		nBn to nAn	0.6	5.8	0.6	4.7	0.4	4.3	0.2	3.9	0.2	3.8	ns	
t <sub>dis</sub>	disable time	nOE to nAn	1.0	6.9	1.0	6.9	1.0	6.9	1.0	6.9	1.0	6.9	ns	
		nOE to nBn	1.5	11.5	1.5	10.4	1.3	9.1	1.1	6.9	0.9	5.8	ns	
t <sub>en</sub>	enable time	nOE to nAn	0.7	5.3	0.7	5.3	0.7	5.3	0.6	5.3	0.4	5.3	ns	
		nOE to nBn	0.9	12.4	0.9	9.7	0.8	7.7	0.6	5.3	0.6	4.4	ns	
<b>V<sub>CC(A)</sub> = 3.0 V to 3.6 V</b>														
t <sub>pd</sub>	propagation delay	nAn to nBn	0.1	9.1	0.1	6.2	0.1	5.0	0.1	3.8	0.1	3.3	ns	
		nBn to nAn	0.6	5.7	0.6	4.7	0.4	3.9	0.2	3.4	0.1	3.3	ns	
t <sub>dis</sub>	disable time	nOE to nAn	0.7	6.2	0.7	6.2	0.7	6.2	0.7	6.2	0.7	6.2	ns	
		nOE to nBn	1.4	11.3	1.4	10.3	1.2	9.0	1.0	7.1	0.8	6.9	ns	
t <sub>en</sub>	enable time	nOE to nAn	0.6	4.2	0.6	4.2	0.6	4.2	0.6	4.2	0.4	4.2	ns	
		nOE to nBn	0.8	12.4	0.8	9.6	0.6	7.5	0.5	5.2	0.5	4.2	ns	

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.

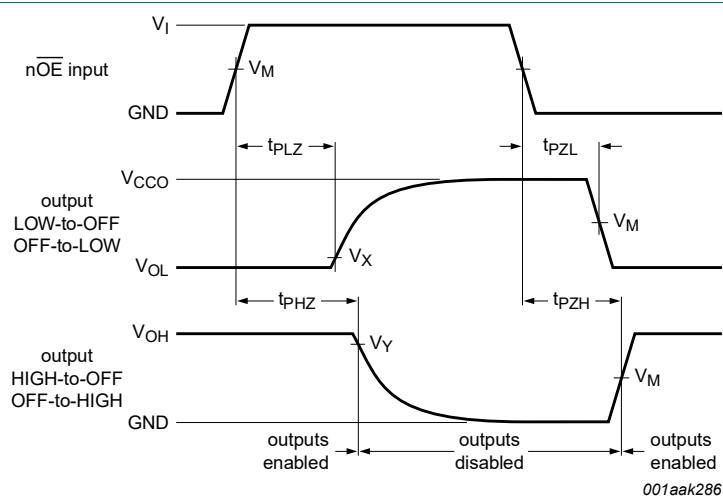
### 11.1. Waveforms and test circuit



Measurement points are given in [Table 15](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 7. The data input (nAn, nBn) to output (nBn, nAn) propagation delay times**



Measurement points are given in [Table 15](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 8. Enable and disable times**

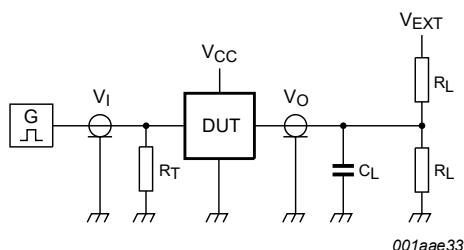
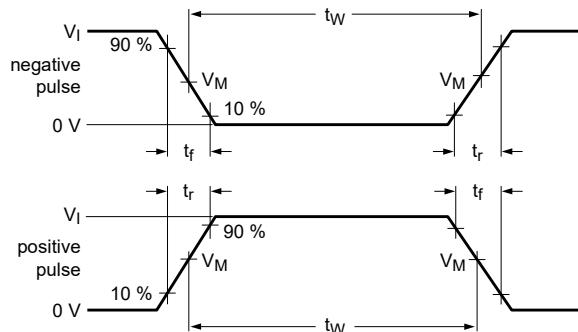
**Table 15. Measurement points**

Supply voltage	Input[1]	Output[2]		
$V_{CC(A)}, V_{CC(B)}$	$V_M$	$V_M$	$V_X$	$V_Y$
0.8 V to 1.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.1$ V	$V_{OH} - 0.1$ V
1.65 V to 2.7 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15$ V	$V_{OH} - 0.15$ V
3.0 V to 3.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V

[1]  $V_{CCI}$  is the supply voltage associated with the data input port.

[2]  $V_{CCO}$  is the supply voltage associated with the output port.

## 4-bit dual supply translating transceiver with configurable voltage translation; 3-state



001aae331

Test data is given in [Table 16](#).

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig. 9. Test circuit for measuring switching times**

**Table 16. Test data**

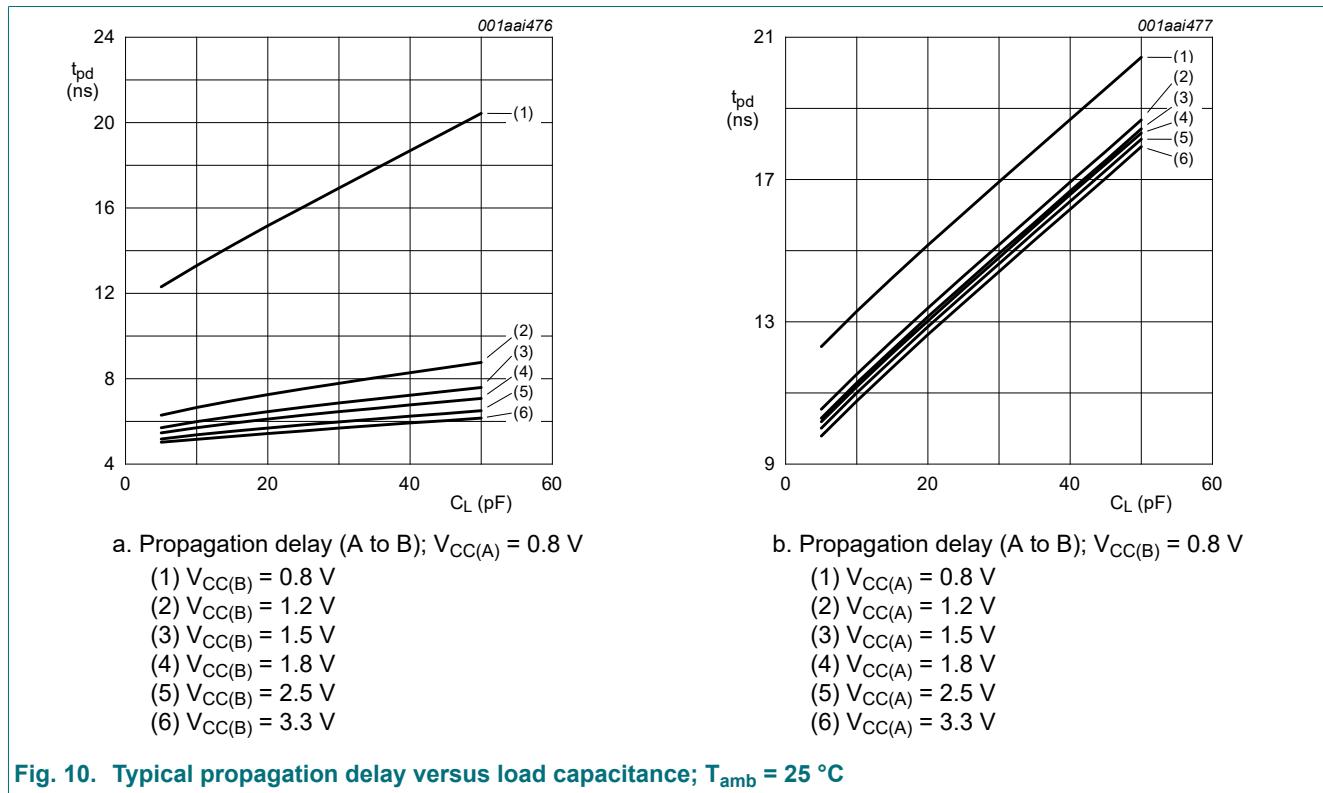
Supply voltage	Input		Load		$V_{EXT}$		
$V_{CC(A)}$ , $V_{CC(B)}$	$V_I$ [1]	$\Delta t/\Delta V$ [2]	$C_L$	$R_L$	$t_{PLH}$ , $t_{PHL}$	$t_{PZH}$ , $t_{PHZ}$	$t_{PZL}$ , $t_{PLZ}$ [3]
0.8 V to 1.6 V	$V_{CCI}$	$\leq 1.0 \text{ ns/V}$	15 pF	2 k $\Omega$	open	GND	2 $V_{CCO}$
1.65 V to 2.7 V	$V_{CCI}$	$\leq 1.0 \text{ ns/V}$	15 pF	2 k $\Omega$	open	GND	2 $V_{CCO}$
3.0 V to 3.6 V	$V_{CCI}$	$\leq 1.0 \text{ ns/V}$	15 pF	2 k $\Omega$	open	GND	2 $V_{CCO}$

[1]  $V_{CCI}$  is the supply voltage associated with the data input port.

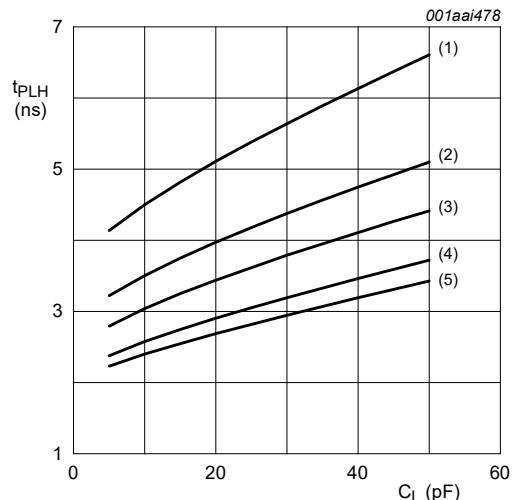
[2]  $dV/dt \geq 1.0 \text{ V/ns}$

[3]  $V_{CCO}$  is the supply voltage associated with the output port.

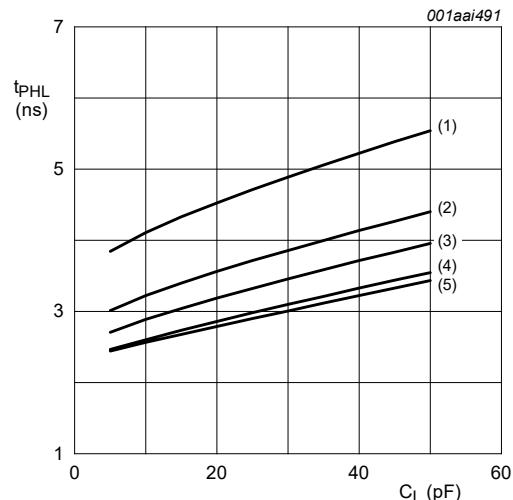
## 12. Typical propagation delay characteristics



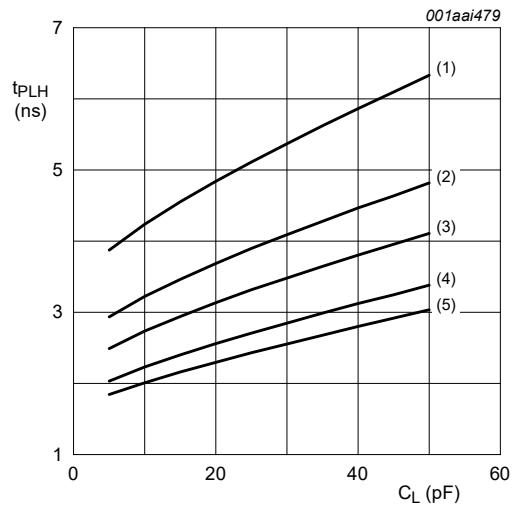
## 4-bit dual supply translating transceiver with configurable voltage translation; 3-state



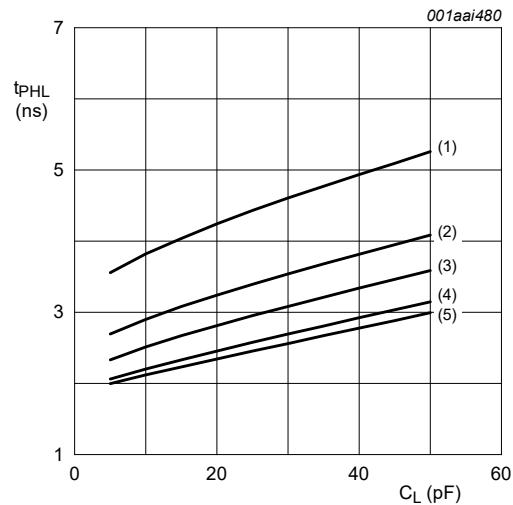
a. LOW to HIGH propagation delay (A to B);  
 $V_{CC(A)} = 1.2 \text{ V}$



b. HIGH to LOW propagation delay (A to B);  
 $V_{CC(A)} = 1.2 \text{ V}$



c. LOW to HIGH propagation delay (A to B);  
 $V_{CC(A)} = 1.5 \text{ V}$

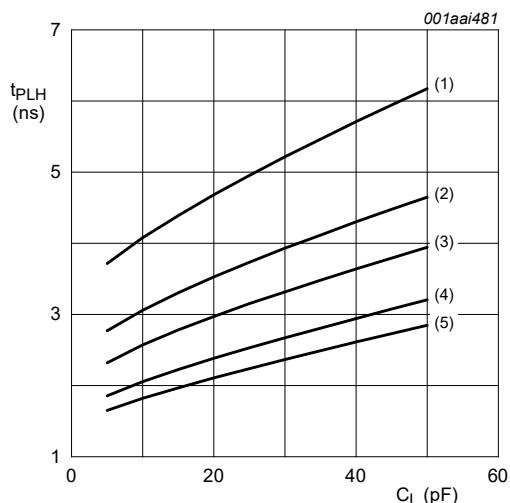


d. HIGH to LOW propagation delay (A to B);  
 $V_{CC(A)} = 1.5 \text{ V}$

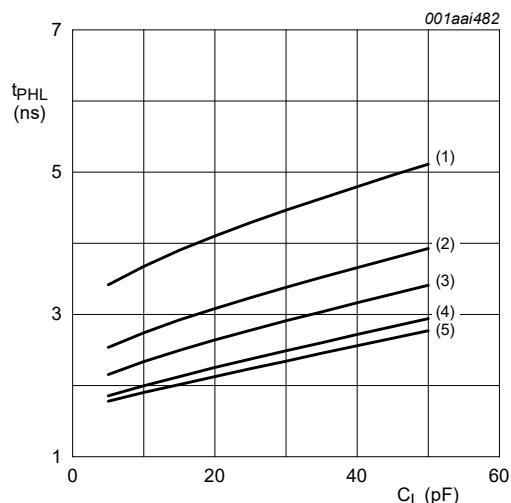
- (1)  $V_{CC(B)} = 1.2 \text{ V}$
- (2)  $V_{CC(B)} = 1.5 \text{ V}$
- (3)  $V_{CC(B)} = 1.8 \text{ V}$
- (4)  $V_{CC(B)} = 2.5 \text{ V}$
- (5)  $V_{CC(B)} = 3.3 \text{ V}$

Fig. 11. Typical propagation delay versus load capacitance;  $T_{amb} = 25 \text{ }^{\circ}\text{C}$

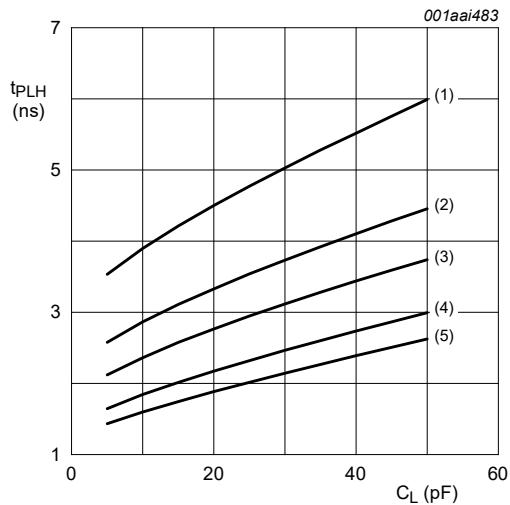
## 4-bit dual supply translating transceiver with configurable voltage translation; 3-state



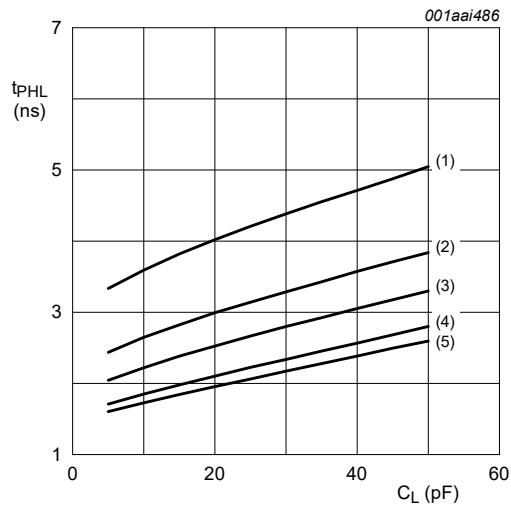
a. LOW to HIGH propagation delay (A to B);  
 $V_{CC(A)} = 1.8$  V



b. HIGH to LOW propagation delay (A to B);  
 $V_{CC(A)} = 1.8$  V



c. LOW to HIGH propagation delay (A to B);  
 $V_{CC(A)} = 2.5$  V

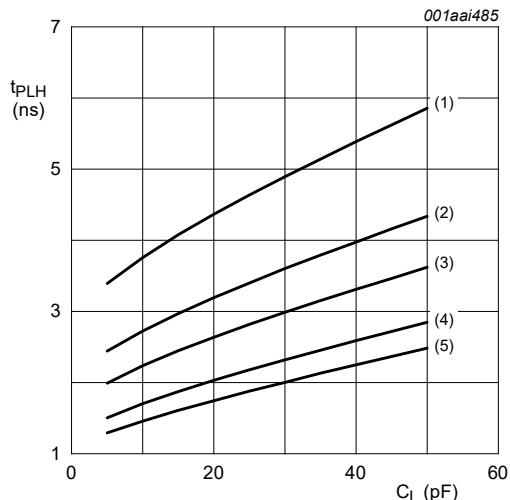


d. HIGH to LOW propagation delay (A to B);  
 $V_{CC(A)} = 2.5$  V

- (1)  $V_{CC(B)} = 1.2$  V
- (2)  $V_{CC(B)} = 1.5$  V
- (3)  $V_{CC(B)} = 1.8$  V
- (4)  $V_{CC(B)} = 2.5$  V
- (5)  $V_{CC(B)} = 3.3$  V

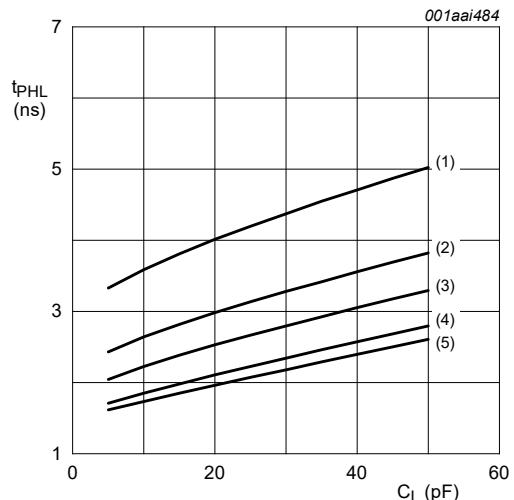
Fig. 12. Typical propagation delay versus load capacitance;  $T_{amb} = 25$  °C

## 4-bit dual supply translating transceiver with configurable voltage translation; 3-state



a. LOW to HIGH propagation delay (A to B);  
 $V_{CC(A)} = 3.3$  V

- (1)  $V_{CC(B)} = 1.2$  V
- (2)  $V_{CC(B)} = 1.5$  V
- (3)  $V_{CC(B)} = 1.8$  V
- (4)  $V_{CC(B)} = 2.5$  V
- (5)  $V_{CC(B)} = 3.3$  V



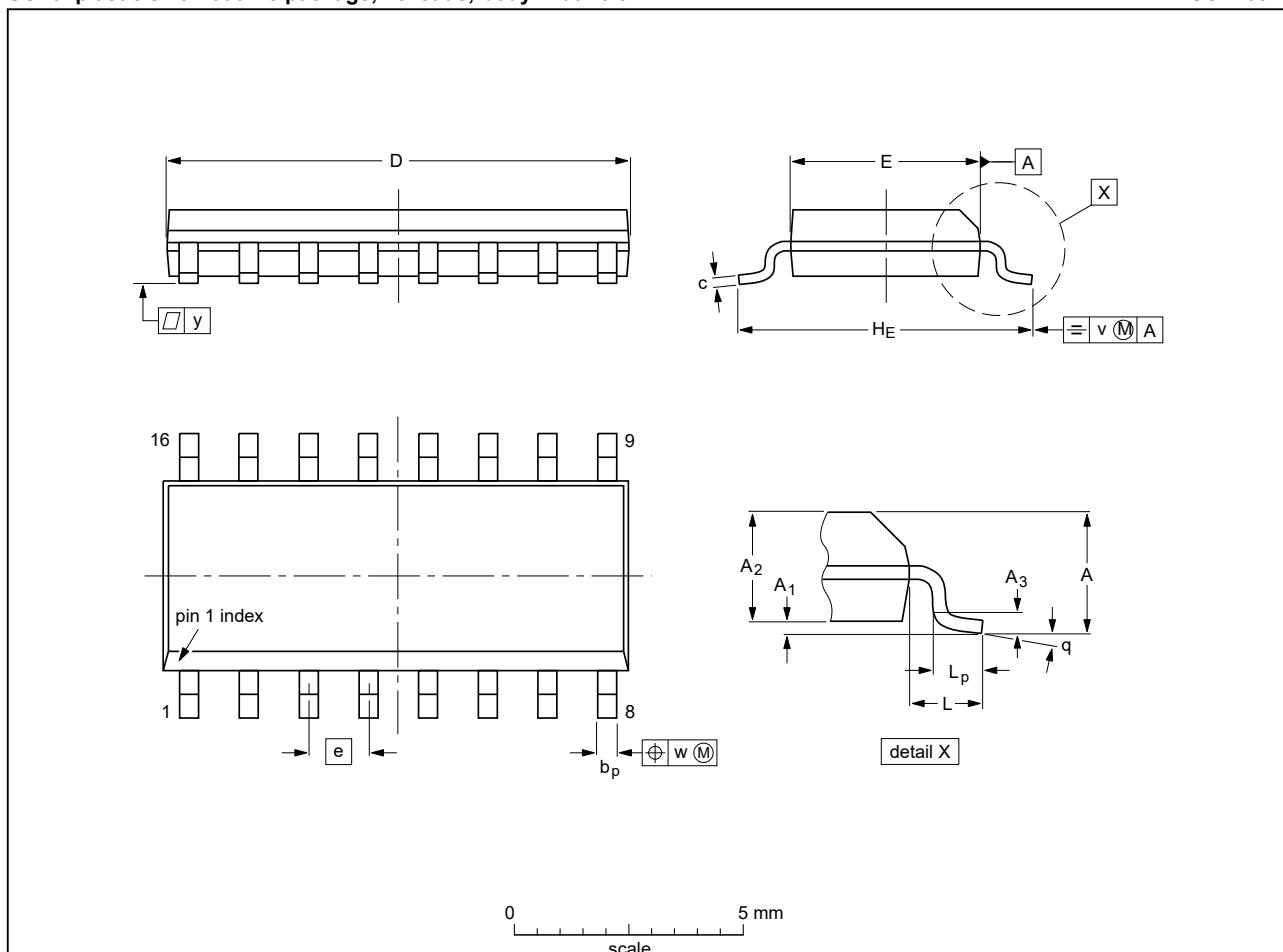
b. HIGH to LOW propagation delay (A to B);  
 $V_{CC(A)} = 3.3$  V

Fig. 13. Typical propagation delay versus load capacitance;  $T_{amb} = 25$  °C

## 13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit	A	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	θ	
mm	max 1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27	0.2	0.25	0.1	8°	
mm	nom			0.25					1.27		1.05					0°	
mm	min 0.10		1.25		0.31	0.10	9.8	3.8		5.8		0.4					
inches	max 0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°	
inches	nom			0.01					0.05		0.041			0.008	0.01	0.004	0°
inches	min 0.004	0.049			0.012	0.004	0.386	0.15		0.228		0.016					

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot109-1\_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				03-02-19 23-10-27

Fig. 14. Package outline SOT109-1 (SO16)

## 4-bit dual supply translating transceiver with configurable voltage translation; 3-state

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

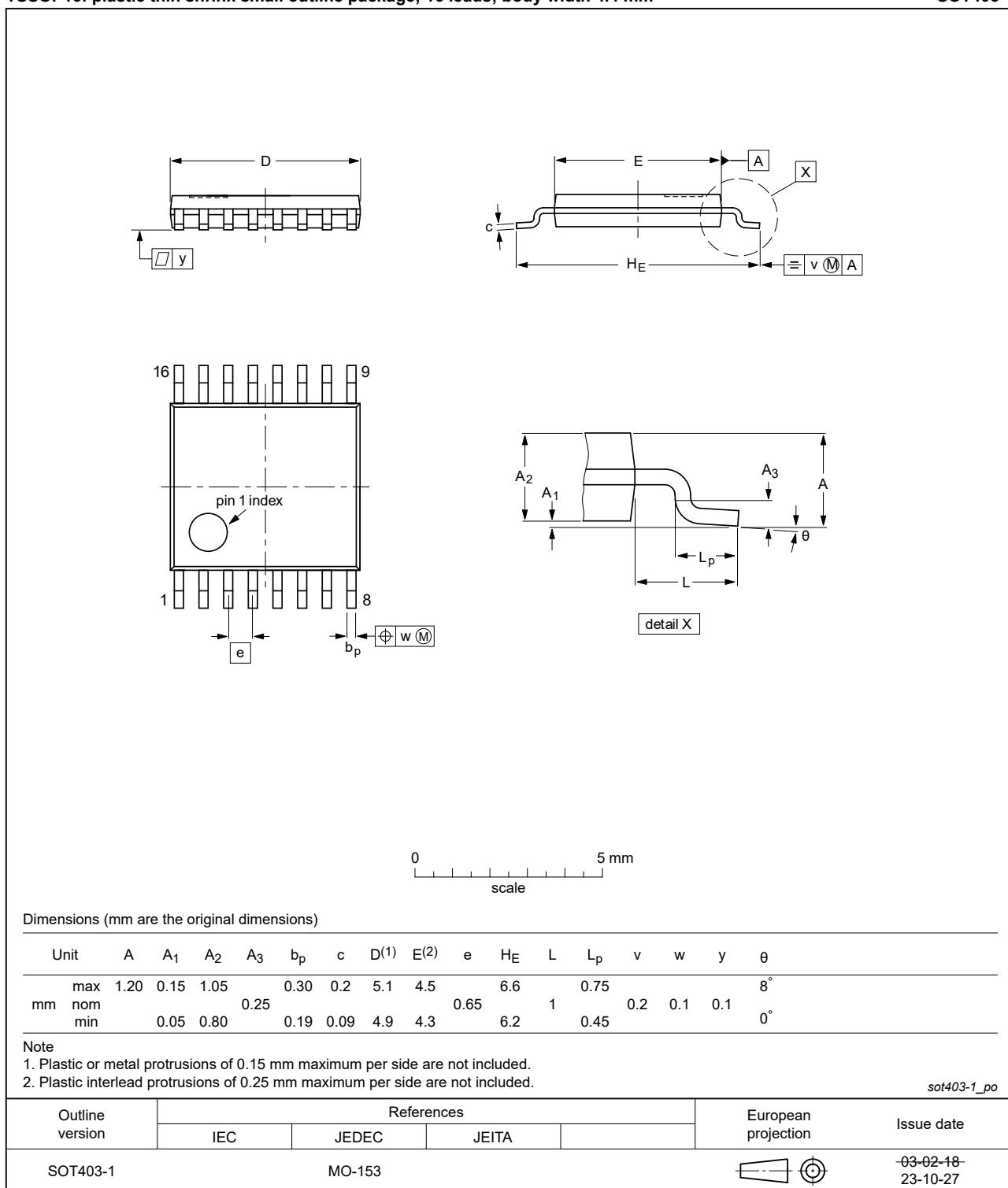


Fig. 15. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;  
16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

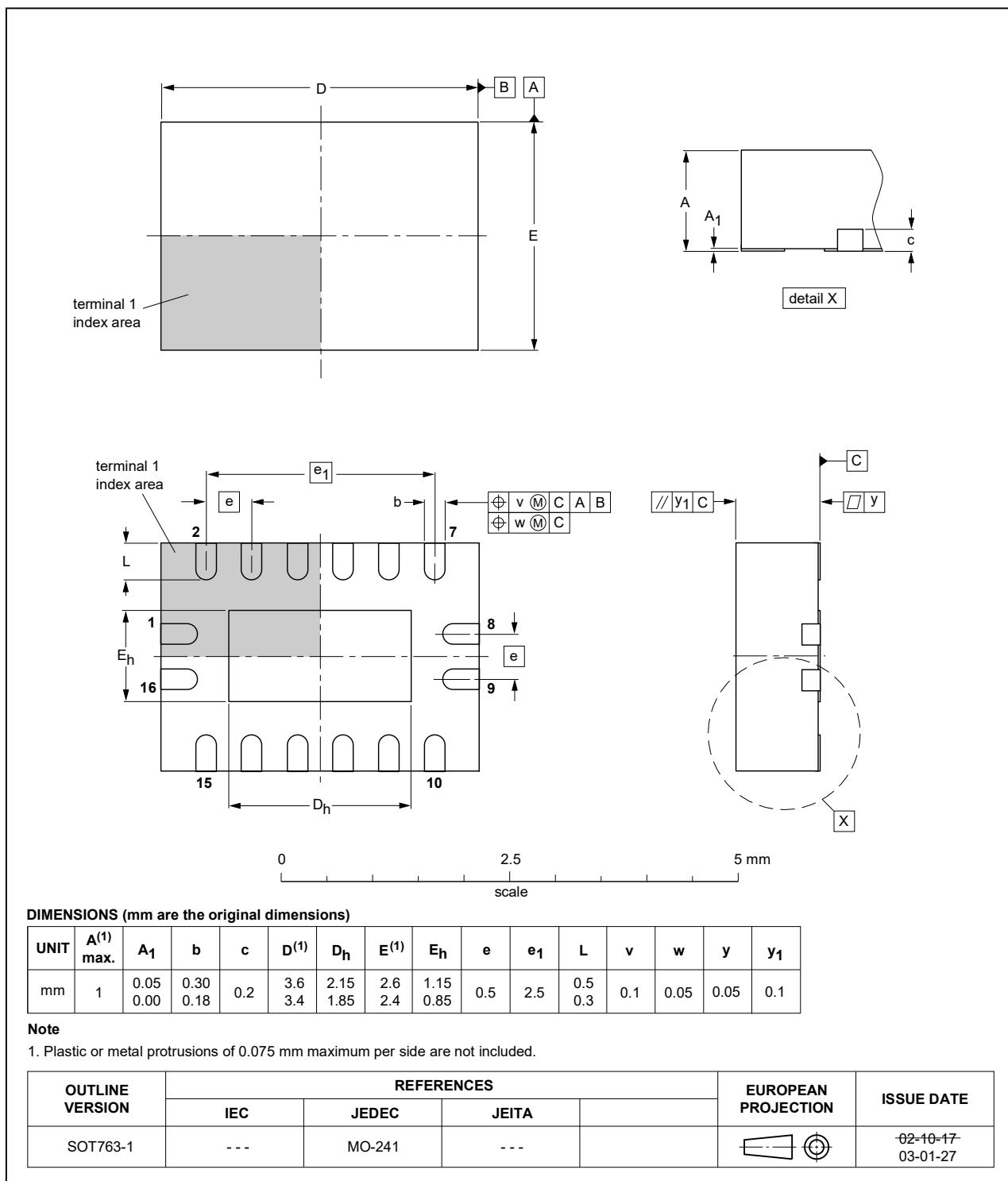


Fig. 16. Package outline SOT763-1 (DHVQFN16)

## 4-bit dual supply translating transceiver with configurable voltage translation; 3-state

XQFN16: plastic, extremely thin quad flat package; no leads;  
16 terminals; body 1.80 x 2.60 x 0.50 mm

SOT1161-1

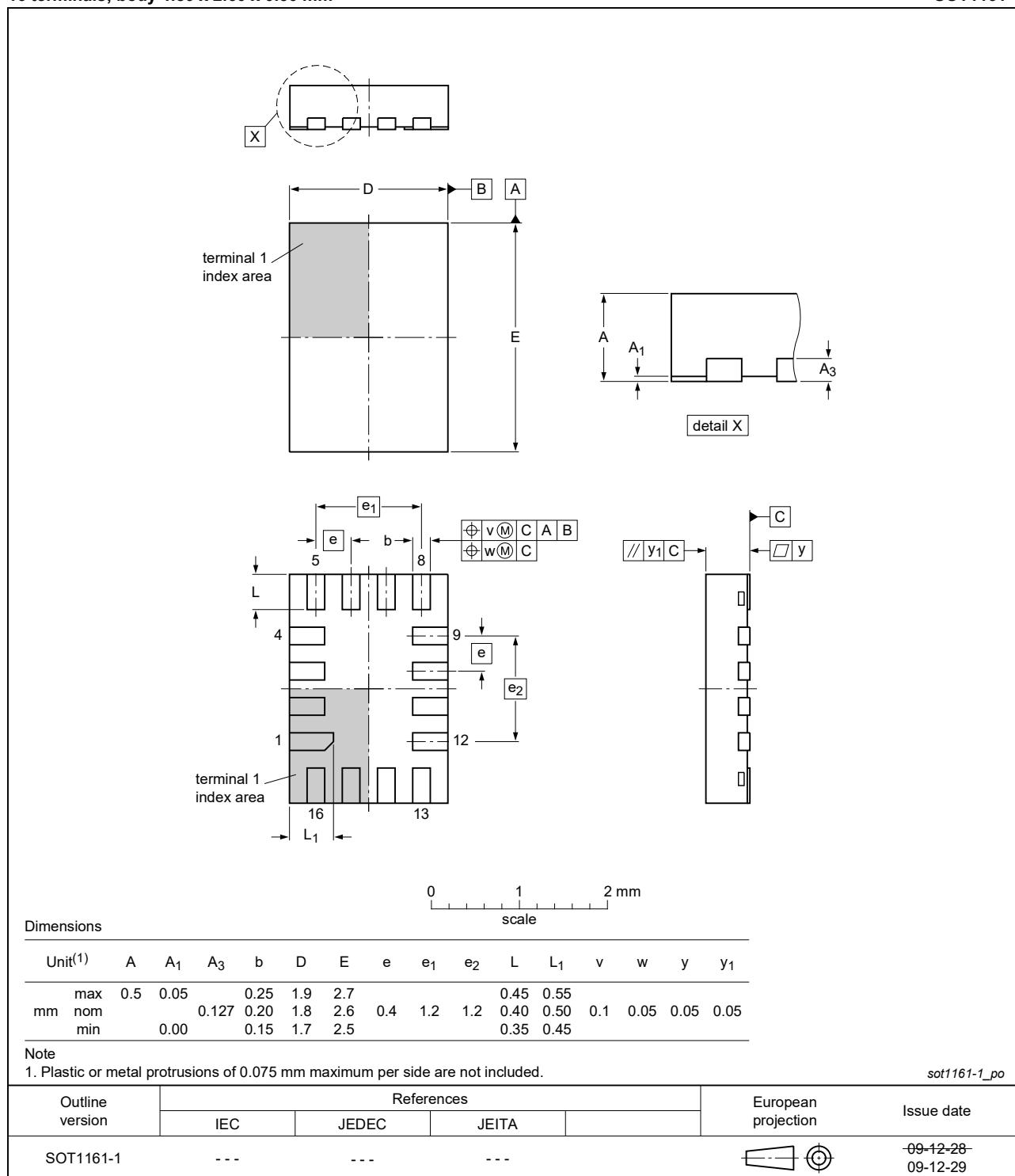


Fig. 17. Package outline SOT1161-1 (XQFN16)

## 14. Abbreviations

**Table 17. Abbreviations**

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

## 15. Revision history

**Table 18. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AVC4T245_Q100 v.6	20240411	Product data sheet	-	74AVC4T245_Q100 v.5
Modifications:			<ul style="list-style-type: none"> <li><a href="#">Fig. 14</a>, <a href="#">Fig. 15</a>: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.</li> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> </ul>	
74AVC4T245_Q100 v.5	20200317	Product data sheet	-	74AVC4T245_Q100 v.4
Modifications:			<ul style="list-style-type: none"> <li><a href="#">Section 2</a> updated.</li> </ul>	
74AVC4T245_Q100 v.4	20190613	Product data sheet	-	74AVC4T245_Q100 v.3
Modifications:			<ul style="list-style-type: none"> <li>Type number 74AVC4T245GU-Q100 (SOT1161-1/XQFN16) added.</li> <li><a href="#">Table 5</a>: Derating values for total power dissipation (<math>P_{tot}</math>) have changed.</li> </ul>	
74AVC4T245_Q100 v.3	20190320	Product data sheet	-	74AVC4T245_Q100 v.2
Modifications:			<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>	
74AVC4T245_Q100 v.2	20151207	Product data sheet	-	74AVC4T245_Q100 v.1
Modifications:			<ul style="list-style-type: none"> <li><a href="#">Table 5</a>: conditions <math>I_{CC}</math> and <math>I_{GND}</math> changed (errata).</li> </ul>	
74AVC4T245_Q100 v.1	20130402	Product data sheet	-	-

## 16. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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