

# FCH47N60F

## N-Channel SuperFET® FRFET® MOSFET

600 V, 47 A, 73 mΩ

### Features

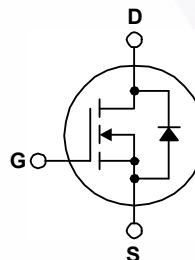
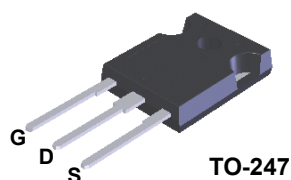
- 650 V @  $T_J = 150^\circ\text{C}$
- Typ.  $R_{DS(on)} = 58\text{ m}\Omega$
- Ultra Low Gate Charge (Typ.  $Q_g = 210\text{ nC}$ )
- Low Effective Output Capacitance (Typ.  $C_{oss\text{eff.}} = 420\text{ pF}$ )
- 100% Avalanche Tested
- RoHS Compliant

### Applications

- Solar Inverter
- AC-DC Power Supply

### Description

SuperFET® MOSFET is Fairchild Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server / telecom power, FPD TV power, ATX power and industrial power applications. SuperFET FRFET® MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FCH47N60F_F133	Unit
$V_{DSS}$	Drain-Source Voltage	600	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	47 29.7	A A
$I_{DM}$	Drain Current - Pulsed (Note 1)	141	A
$V_{GSS}$	Gate-Source voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	1800	mJ
$I_{AR}$	Avalanche Current (Note 1)	47	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	41.7	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	50	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	417 3.33	W W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FCH47N60F_F133	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.3	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	41.7	$^\circ\text{C/W}$

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCH47N60F	FCH47N60F_F133	TO-247	-	-	30

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA, T <sub>J</sub> = 25°C	600	--	--	V
		V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA, T <sub>J</sub> = 150°C	--	650	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, Referenced to 25°C	--	0.6	--	V/°C
BV <sub>DS</sub>	Drain-Source Avalanche Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 47A	--	700	--	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600V, V <sub>GS</sub> = 0V	--	--	10	μA
		V <sub>DS</sub> = 480V, T <sub>C</sub> = 125°C	--	--	100	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30V, V <sub>DS</sub> = 0V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30V, V <sub>DS</sub> = 0V	--	--	-100	nA
On Characteristics						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	3.0	--	5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 23.5A	--	0.062	0.073	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40V, I <sub>D</sub> = 23.5A	--	40	--	S
Dynamic Characteristics						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1.0MHz	--	5900	8000	pF
C <sub>oss</sub>	Output Capacitance		--	3200	4200	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	250	--	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 480V, V <sub>GS</sub> = 0V, f = 1.0MHz	--	160	--	pF
C <sub>oss eff.</sub>	Effective Output Capacitance	V <sub>DS</sub> = 0V to 400V, V <sub>GS</sub> = 0V	--	420	--	pF
Switching Characteristics						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 300V, I <sub>D</sub> = 47A R <sub>G</sub> = 25Ω  (Note 4)	--	185	430	ns
t <sub>r</sub>	Turn-On Rise Time		--	210	450	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	520	1100	ns
t <sub>f</sub>	Turn-Off Fall Time		--	75	160	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 480V, I <sub>D</sub> = 47A V <sub>GS</sub> = 10V  (Note 4)	--	210	270	nC
Q <sub>gs</sub>	Gate-Source Charge		--	38	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	110	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	47	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	141	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = 47A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>S</sub> = 47A	--	240	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>F</sub> /dt =100A/μs	--	2.04	--	μC

### NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. I<sub>AS</sub> = 18A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25Ω, Starting T<sub>J</sub> = 25°C
3. I<sub>SD</sub> ≤ 47A, di<sub>F</sub>/dt ≤ 1200A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25°C
4. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

Figure 1. On-Region Characteristics

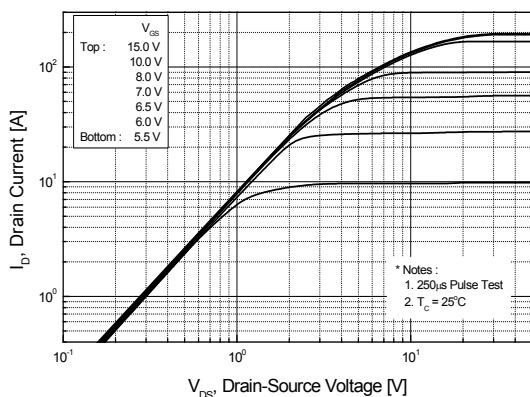


Figure 2. Transfer Characteristics

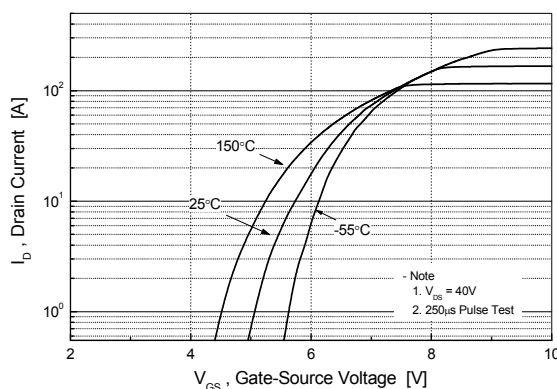


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

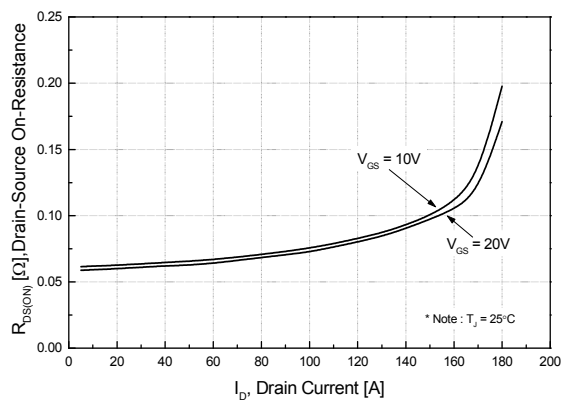


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

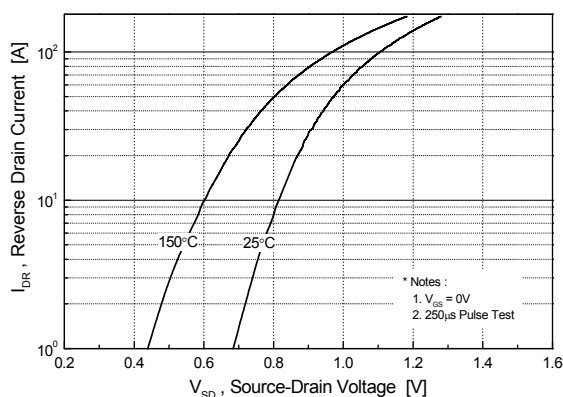


Figure 5. Capacitance Characteristics

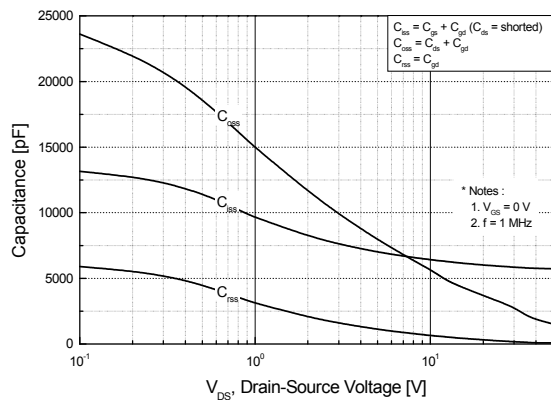
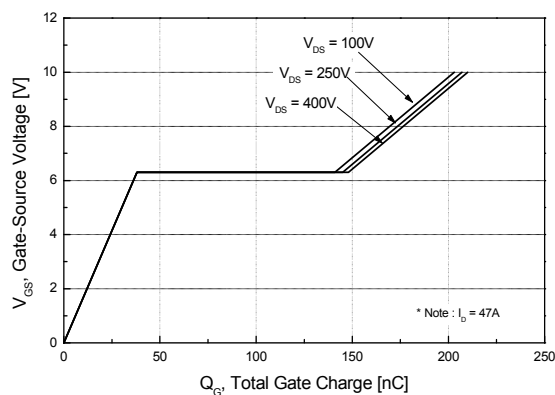
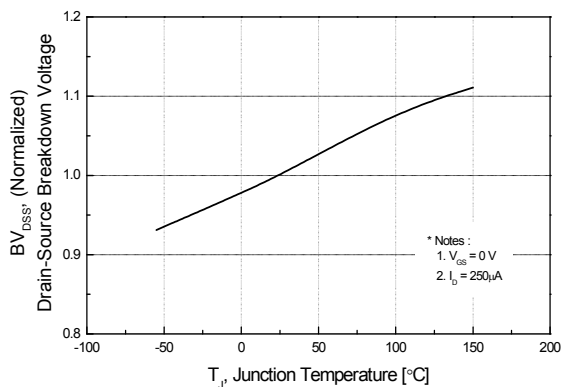


Figure 6. Gate Charge Characteristics

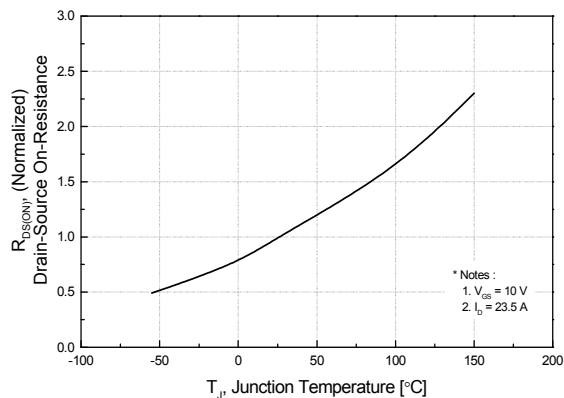


## Typical Performance Characteristics (Continued)

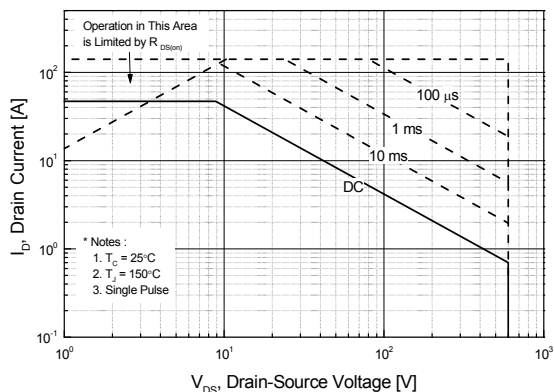
**Figure 7. Breakdown Voltage Variation vs. Temperature**



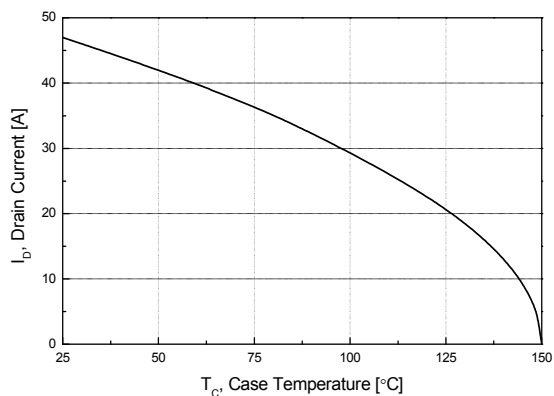
**Figure 8. On-Resistance Variation vs. Temperature**



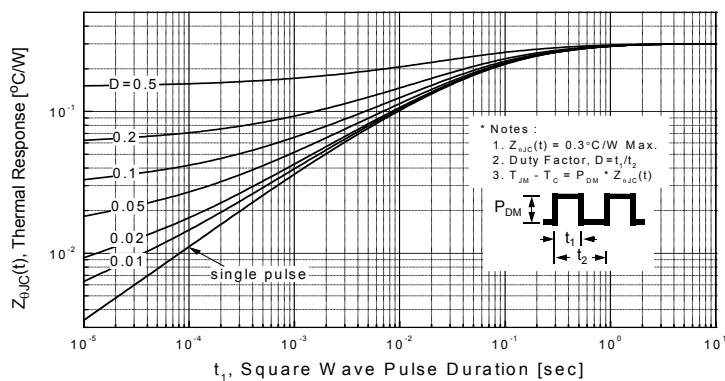
**Figure 9. Safe Operating Area**



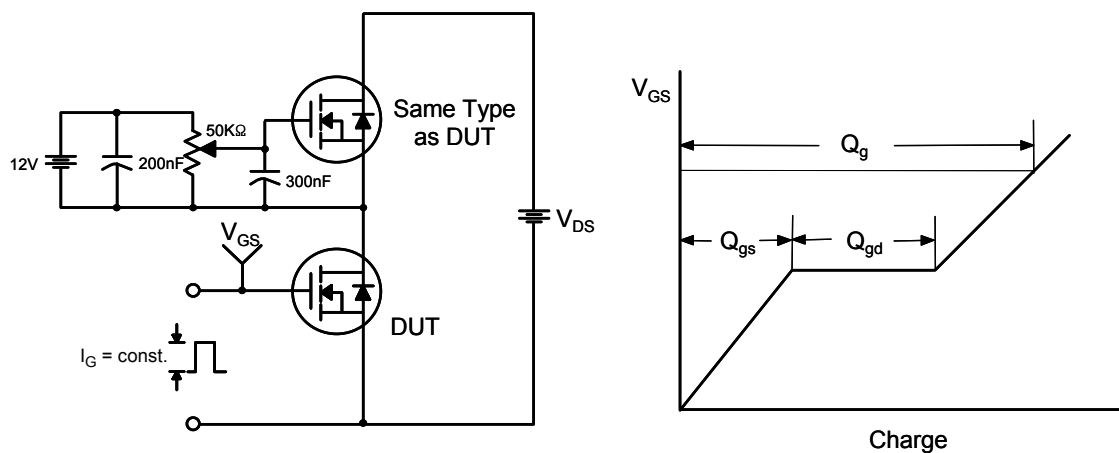
**Figure 10. Maximum Drain Current vs. Case Temperature**



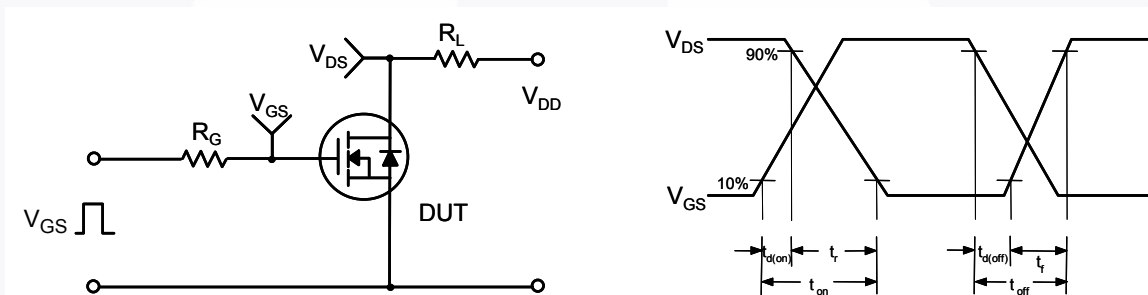
**Figure 11. Transient Thermal Response Curve**



**Figure 12. Gate Charge Test Circuit & Waveform**



**Figure 13. Resistive Switching Test Circuit & Waveforms**



**Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms**

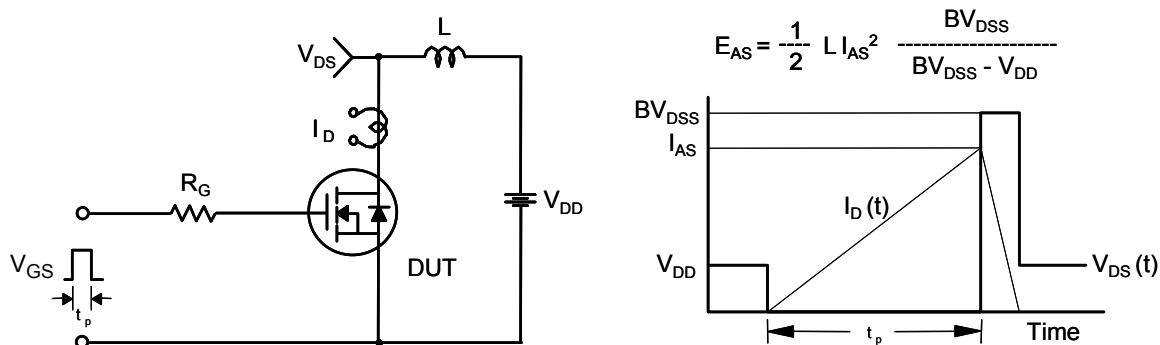
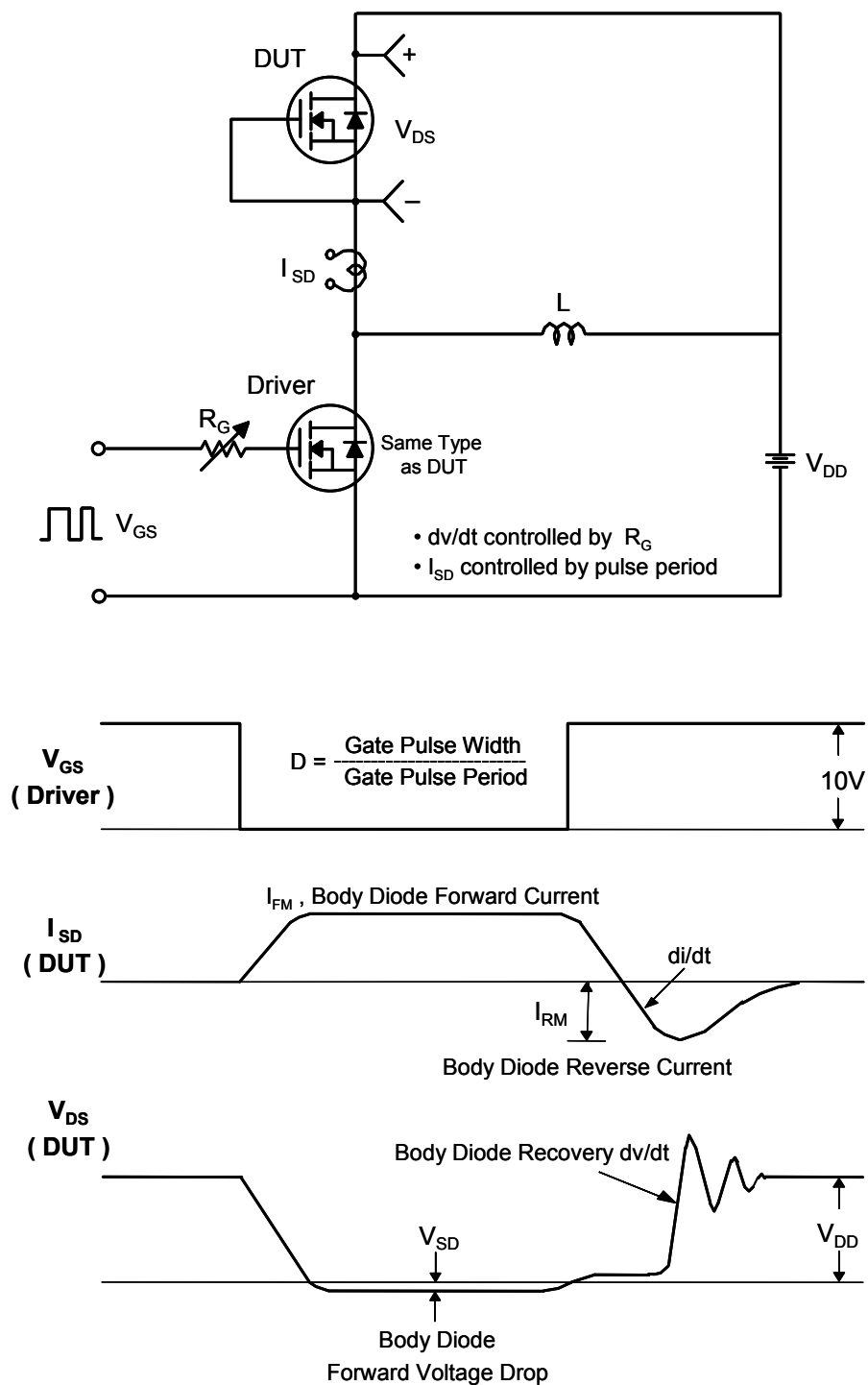
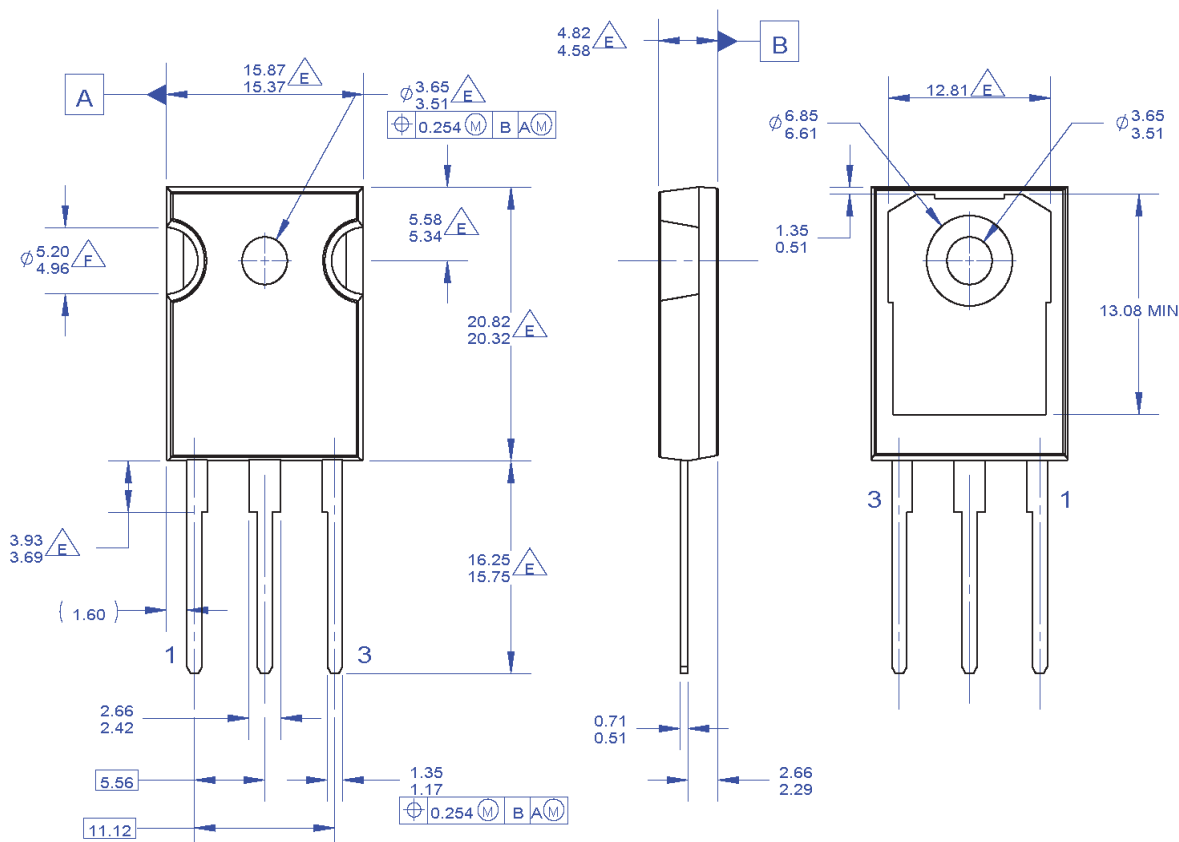


Figure 15. Peak Diode Recovery dv/dt Test Circuit &amp; Waveforms



## Mechanical Dimensions

## TO-247 3L



NOTES: UNLESS OTHERWISE SPECIFIED.

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- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DRAWING CONFORMS TO ASME Y14.5 - 1994

$\triangle E$  DOES NOT COMPLY JEDEC STANDARD VALUE

$\triangle F$  NOTCH MAY BE SQUARE

G. DRAWING FILENAME: MKT-TO247A03\_REV03

**Figure 16. TO-247, Molded, 3 Lead, Jedec Variation AB**

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Dimension in Millimeters



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Rev. I66