FEATURES

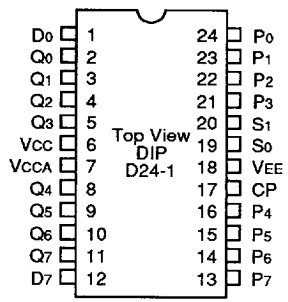
- **Max. shift frequency of 600MHz**
- **Max. Clock to Q delay of 1200ps**
- **IEE min. of –150mA**
- **ESD protection of 2000V**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option:**
  — **VEE = –4.2V to –5.46V**
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **70% faster than National 300K at lower power**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

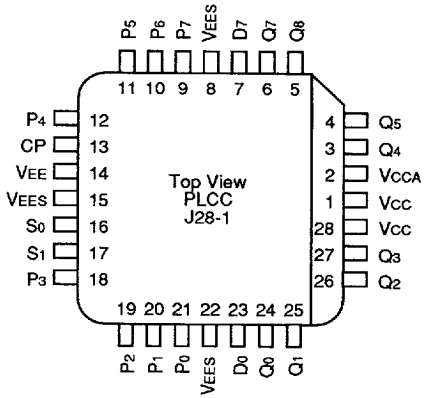
DESCRIPTION

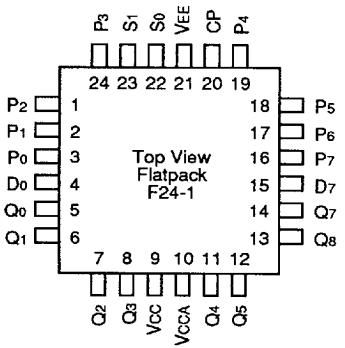
The SY100S341 offer eight D-type, edge-triggered flip-flops with both individual inputs for parallel operation as well as serial inputs for bidirectional shifting, and are designed for use in high-performance ECL systems. Data is clocked into the flip-flops on the rising edge of the clock.

The mode of operation is selected by two Select inputs (S_0, S_1) which determine if the device performs a shift, hold or parallel entry function, as described in the Truth Table. The inputs on these devices have 75KΩ pull-down resistors.

PIN CONFIGURATIONS





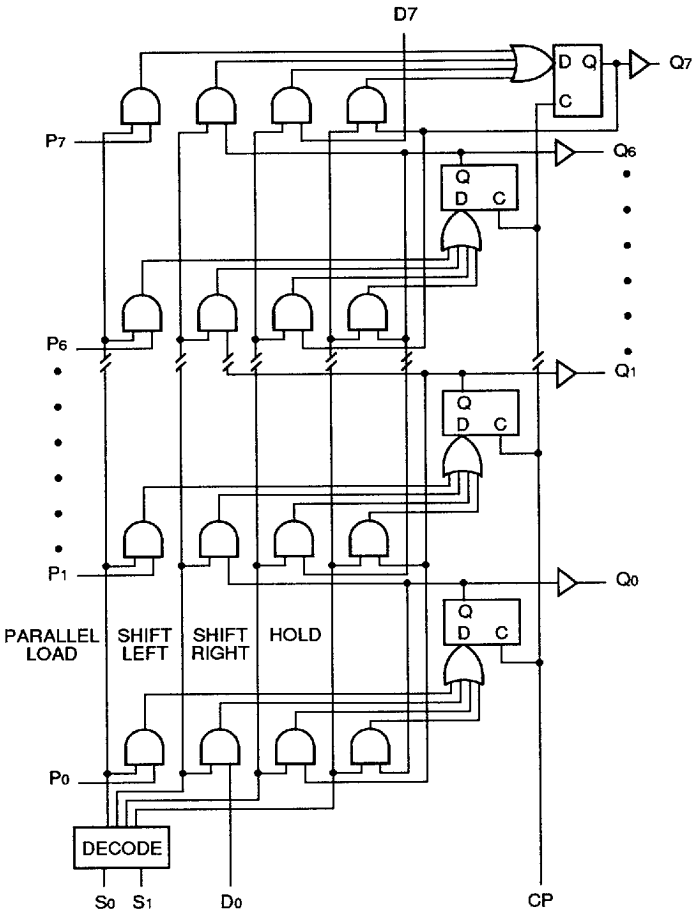


PIN NAMES

Label	Function
CP	Clock Pulse Input
S_0 — S_1	Select Inputs
D_0 — D_7	Serial Inputs
P_0 — P_7	Parallel Inputs
Q_0 — Q_7	Data Outputs

Rev: B Amendment: /0
Issue Date: February, 1994

BLOCK DIAGRAM



TRUTH TABLE

Function	Inputs					Outputs							
	D_7	D_0	S_1	S_0	CP	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
Load Register	X	X	L	L	↗	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
Shift Left	X	L	L	H	↗	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	L
Shift Left	X	H	L	H	↗	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	H
Shift Right	L	X	H	L	↗	L	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Shift Right	H	X	H	L	↗	H	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Hold	X	X	H	H	X	No Change							
Hold	X	X	X	X	H								
Hold	X	X	X	X	L								

NOTE:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↗ = LOW-to-HIGH Transition

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current, All Inputs	—	—	200	µA	V_{IN} = V_{IH} (Max.)
I_{EE}	Power Supply Current	–150	–102	–71	mA	Inputs Open

6

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{shift}	Shift Frequency	600	—	600	—	600	—	MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Output	450	1200	450	1200	450	1200	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps
t_s	Set-up Time D_n, P_n S_n	 300 600	 — —	 300 600	 — —	 300 600	 — —	ps
t_h	Hold Time D_n, P_n S_n	 300 0	 — —	 300 0	 — —	 300 0	 — —	ps
t_{pw} (H)	Pulse Width HIGH, CP	—	600	—	600	—	600	ps

AC ELECTRICAL CHARACTERISTICS (CONT'D.)

CERPACK

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

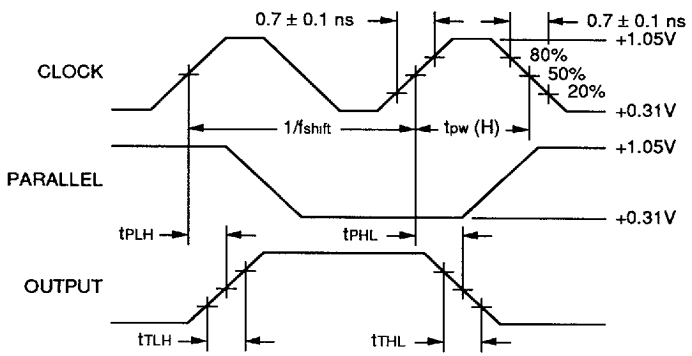
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{shift}	Shift Frequency	600	—	600	—	600	—	MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Output	450	1100	450	1100	450	1100	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps
t_s	Set-up Time D_n, P_n S_n	 300 600	 — —	 300 600	 — —	 300 600	 — —	ps
t_h	Hold Time D_n, P_n S_n	 300 0	 — —	 300 0	 — —	 300 0	 — —	ps
t_{pw} (H)	Pulse Width HIGH, CP	—	600	—	600	—	600	ps

PLCC

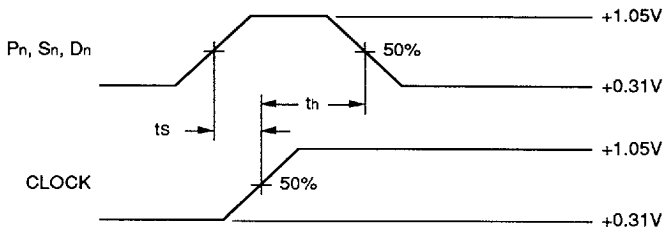
V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{shift}	Shift Frequency	600	—	600	—	600	—	MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Output	450	1000	450	1000	450	1000	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps
t_s	Set-up Time D_n, P_n S_n	 300 600	 — —	 300 600	 — —	 300 600	 — —	ps
t_h	Hold Time D_n, P_n S_n	 300 0	 — —	 300 0	 — —	 300 0	 — —	ps
t_{pw} (H)	Pulse Width HIGH, CP	—	600	—	600	—	600	ps

TIMING DIAGRAMS



Propagation Delay and Transition Times



Set-up and Hold Times

NOTES:
ts is the minimum time before the transition of the clock that information must be present at the data input
th is the minimum time after the transition of the clock that information must remain unchanged at the data input.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S341DC	D24-1	Commercial
SY100S341FC	F24-1	Commercial
SY100S341JC	J28-1	Commercial