


SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

LV5990M — Bi-CMOS IC Low power consumption and high efficiency Step-down Switching Regulator

Overview

LV5990M is 1ch DC-DC converter with built-in power Pch MOS transistor. The recommended operating range is 4.5V to 18V. The maximum current is 3A. The operating current is about 90 μ A, and low power consumption is achieved.

Functions

- 1ch SBD rectification DC-DC converter IC with built-in power Pch MOS transistor
- Maximum value of light load mode current is 90 μ A.
- Built-in OCP circuit with P-by-P method
- When P-by-P is generated continuously, it shifts to the HICCUP operation.
- If connect C-HICCUP to GND pin, then latch-off when over current.
- The oscillatory frequency is 360kHz.
- UVLO and built-in TSD

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Input voltage	V _{IN} -max		22	V
Allowable pin voltage	SW		30	V
	EN, PG		V _{IN}	V
	PDR		V _{IN} -6	V
	REF		6	V
	SS,FB,COMP		REF	V
	C-HICCUP			
Allowable power dissipation	Pd max	specified substrate *	1.05	W
Operating temperature	Topr		-40 to 85	°C
Storage temperature	Tstg		-55 to 150	°C

* Specified board: 40.0mm × 30.0mm × 1.6mm, glass epoxy.

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LV5990M

Recommended Operating Conditions at Ta = 25°C

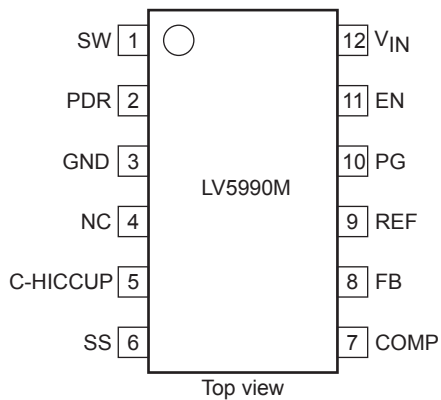
Parameter	Symbol	Conditions	Ratings	Unit
Input voltage range	V _{IN}		4.5 to 18	V

Electrical Characteristics at Ta = 25°C, V_{IN} = 15V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Reference voltage						
Internal reference voltage	VREF		1.235	1.260	1.285	V
Pch drive voltage	VPDR	I _{OUT} =0 to -5mA	V _{CC} -5.5	V _{CC} -5.0	V _{CC} -4.5	V
Saw wave oscillator						
Oscillatory frequency	F _{OSC}		300	360	420	kHz
ON/OFF circuit						
IC startup voltage (EN pin)	V _{CNT_ON}		1.5		V _{IN}	V
Disable voltage (EN pin)	V _{CNT_OFF}				0.3	V
Soft start circuit						
Soft start source current	I _{SS_SC}	EN>1.5V	1.3	2	3	μA
Soft start sink current	I _{SS_SK}	EN<0.3V, SS=0.4V	120	150	180	μA
UVLO circuit						
UVLO release voltage	V _{UVLO_N}	FB=COMP	3.0	3.4	3.8	V
UVLO lock voltage	V _{UVLO_F}	FB=COMP	2.5	2.9	3.3	V
Error amplifier						
Input bias current	I _{EA_IN}		-100	-50	100	nA
Error amplifier gain	G _{EA}		100	250	400	μA/V
Output sink current	I _{EA_OSK}	FB=1.75V	-40	-20	-10	μA
Output source current	I _{EA_OSC}	FB=0.75V	10	20	40	μA
Over current limit circuit						
Current limit peak	I _{CL}		3.2	4.7	6.2	A
HICCUP timer start-up cycle	N _{LCYCLES}			15		cycle
HICCUP comparator threshold voltage	V _{thIC}		1.20	1.26	1.32	V
HICCUP timer charge current	I _{HIC}		1	2	3	μA
PWM comparator						
Maximum on-duty	D _{MAX}		95			%
Logic output						
Power good "L" sink current	I _{pwrgd_L}	PG=5V	4	5	6	mA
Power good "H" leakage current	I _{pwrgd_H}	PG=5V			1	μA
Power good threshold FB voltage	V _{tPG}		1.0	1.1	1.2	V
Power good hysteresis	V _{PG_H}		40	50	60	mV
Power good impedance	R _{PG}			1		kΩ
Output						
Output on-resistance	R _{ON}	I _O =1A		150		mΩ
The entire device						
Standby current	I _{CCS}	EN<0.3V			1	μA
Light load mode consumption current	I _{sleep1}	EN>1.5V, I _{LOAD} =0, No oscillatory -20°C≤T _a ≤70°C *	50	70	90	μA
Thermal shutdown	TSD	*		170		°C

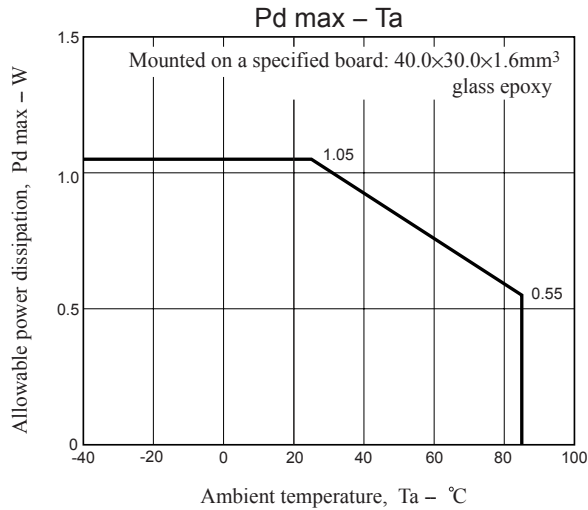
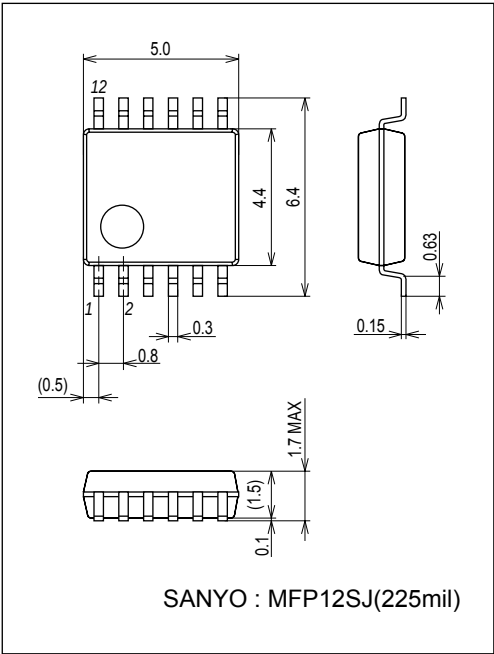
*: Design certification

Pin Assignment

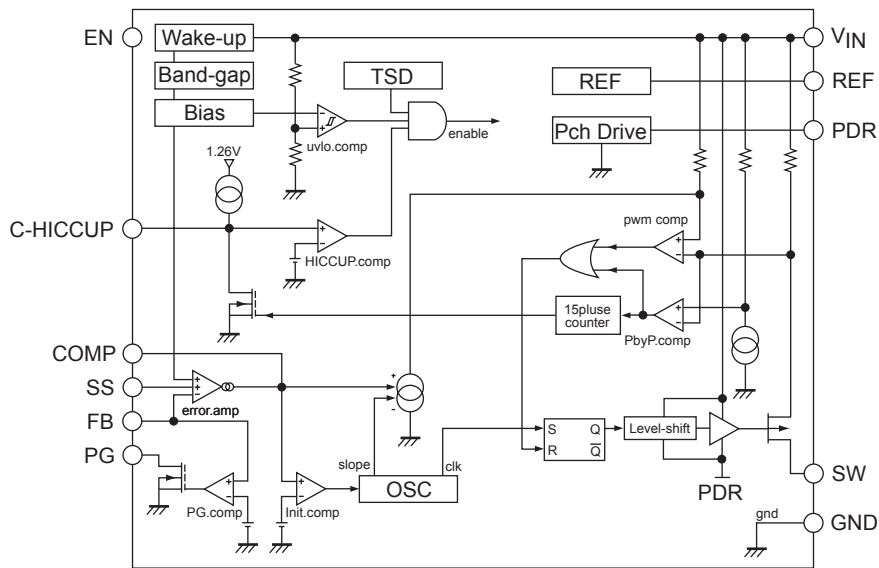


Package Dimensions

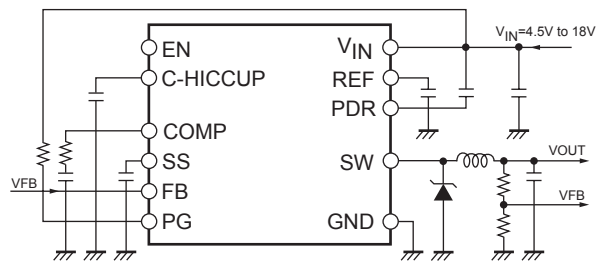
unit : mm (typ)
3403



Block Diagram



Application Circuit



Pin Function

Pin No.	Pin name	Function	Equivalent circuit
1	SW	High-side Pch MOSFET drain pin	
2	PDR	Pch MOSFET gate drive voltage The bypass capacitor is necessarily connected between this pin and V_{IN} .	
3	GND	Ground pin. Ground pin voltage is reference voltage.	
12	V_{IN}	Supply voltage pin. It is observed by the UVLO function. When its voltage becomes 3.4V or more, ICs startup in soft start.	
5	C-HICCUP	It is capacitor connection pin for setting re-startup cycle in HICCUP mode. If connect it to GND pin, then latch-off when over current.	
6	SS	Capacitor connection pin for soft start. About 2μA current charges the soft start capacitor.	
7	COMP	Error amplifier output pin. The phase compensation network is connected between GND pin and COMP pin.	
8	FB	Error amplifier reverse input pin. ICs make its voltage keep 1.26V. Output voltage is divided by external resistances and it across FB.	

Continued on next page.

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Pin No.	Pin name	Function	Equivalent circuit
9	REF	Reference voltage	
10	PG	Power good pin. Connect to open drain of MOS-FET in ICs inside. Setting output voltage to "L", when FB voltage is 1.05V or less.	
11	EN	ON/OFF pin.	

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