

(TLP2601)

ISOLATED LINE RECEIVER

SIMPLEX/MULTIPLEX DATA TRANSMISSION

COMPUTER-PERIPHERAL INTERFACE

MICROPROCESSOR SYSTEM INTERFACE

DIGITAL ISOLATION FOR A/D, D/A CONVERSION

DIRECT REPLACEMENT FOR HCPL-2601

The TOSHIBA TLP2601 a photocoupler which combines a GaAlAs IRED as the emitter and an integrated high gain, high speed photodetector.

The output of the detector circuit is an open collector, Schottky clamped transistor.

A Faraday shield integrated on the photodetector chip reduces the effects of capacitive coupling between the input LED emitter and the high gain stages of the detector. This provides an effective common mode transient immunity of $1000\text{V}/\mu\text{s}$.

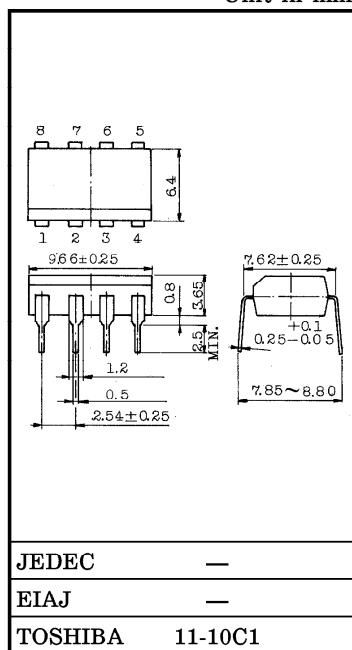
- Input Current Thresholds : $I_F=5\text{mA}$ Max.
- Isolation Voltage : 2500Vrms Min.
- Switching Speed : 10MBd
- Common Mode Transient Immunity : $1000\text{V} / \mu\text{s}$ Min.
- Guaranteed Performance Over Temp. : $0^\circ\text{C}\sim 70^\circ\text{C}$
- UL Recognized : UL1577, File No. E67349

TRUTH TABLE
(Positive Logic)

INPUT	ENABLE	OUTPUT
H	H	L
L	H	H
H	L	H
L	L	H

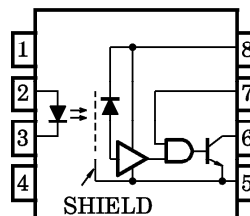
A 0.01 to 0.1 μ F bypass capacitor must be connected between pins 8 and 5 (See Note 1).

Unit in mm

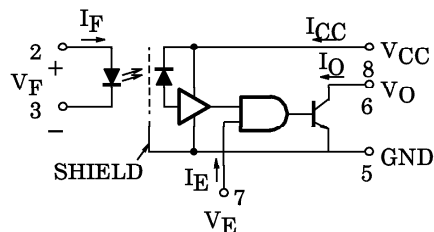


Weight : 0.54g

PIN CONFIGURATION (TOP VIEW)



SCHEMATIC



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RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input Current, Low Level	I _{FL}	0	—	250	μA
Input Current, High Level	I _{FH}	6.3 *	—	20	mA
Supply Voltage, Output	V _{CC}	4.5	—	5.5	V
High Level Enable Voltage	V _{EH}	2.0	—	V _{CC}	V
Low Level Enable Voltage	V _{EL}	0	—	0.8	V
Fan Out (TTL Load)	N	—	—	8	—
Operating Temperature	T _{opr}	0	—	70	°C

* 6.3mA is a guard banded value which allows for at least 20% CTR degradation.
 Initial input current threshold value is 5.0mA or less.

MAXIMUM RATINGS (No derating Required)

CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current	I _F	20	mA
	Reverse Voltage	V _R	5	V
DETECTOR	Output Current	I _O	25	mA
	Output Voltage	V _O	7	V
	Supply Voltage (1 Minute Maximum)	V _{CC}	7	V
	Enable Input Voltage (Not to exceed V _{CC} by more than 500mV)	V _E	5.5	V
	Output Collector Power Dissipation	P _O	40	mW
	Operating Temperature Range	T _{opr}	0~70	°C
Storage Temperature Range		T _{stg}	−55~125	°C
Lead Solder Temperature (10 sec.)**		T _{sold}	260	°C
Isolation Voltage (R. H. ≤ 60%, AC / 1min., Note 10)		BV _S	2500	V _{rms}
			3540	V _{dc}

** 1.6mm below seating plane.

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ELECTRICAL CHARACTERISTICS (Ta = 0°C~70°C Unless Otherwise Noted)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
High Level Output Current	I _{OH}	V _{CC} =5.5V, V _O =5.5V I _F =250μA, V _E =2.0V	—	1	250	μA
Low Level Output Voltage	V _{OL}	V _{CC} =5.5V, I _F =5mA V _E =2.0V, I _{OL} (Sinking) = 13mA	—	0.4	0.6	V
High Level Supply Current	I _{CCH}	V _{CC} =5.5V, I _F =0, V _E =0.5V	—	7	15	mA
Low Level Supply Current	I _{CCL}	V _{CC} =5.5V, I _F =10mA V _E =0.5V	—	12	19	mA
Low Level Enable Current	I _{EL}	V _{CC} =5.5V, V _E =0.5V	—	−1.6	−2.0	mA
High Level Enable Current	I _{EH}	V _{CC} =5.5V, V _E =2.0V	—	−1	—	mA
High Level Enable Voltage	V _{EH}	Note 11	2.0	—	—	V
Low Level Enable Voltage	V _{EL}	—	—	—	0.8	
Input Forward Voltage	V _F	I _F =10mA, Ta=25°C	—	1.65	1.75	V
Input Reverse Breakdown Voltage	BV _R	I _R =10μA, Ta=25°C	5	—	—	V
Input Capacitance	C _{IN}	V _F =0, f=1MHz	—	45	—	pF
Input Diode Temperature Coefficient	ΔV _F /ΔT _A	I _F =10mA	—	−2.0	—	mV/°C
Input-Output Insulation Leakage Current	I _{I-O}	Relative Humidity=45% Ta=25°C, t=5 second V _{I-O} =3000Vdc, Note 10	—	—	1	μA
Resistance (Input-Output)	R _{I-O}	V _{I-O} =500V, R. H. ≤ 60% Note 10	5×10 ¹⁰	10 ¹⁴	—	Ω
Capacitance (Input-Output)	C _{I-O}	f=1MHz, Note 10	—	0.6	—	pF

** All typical values are at V_{CC}=5V, Ta=25°C.

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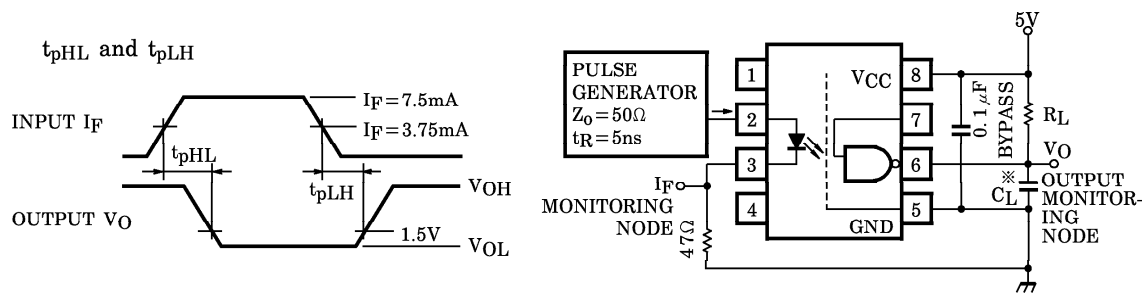
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SWITCHING CHARACTERISTICS ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time to High Output Level	t_{pLH}	1	$R_L = 350\Omega$, $C_L = 15\text{pF}$ $I_F = 7.5\text{mA}$ Note 2, 3, 4 & 5	—	60	75	ns
Propagation Delay Time to Low Output Level	t_{pHL}			—	60	75	ns
Output Rise Time (10-90%)	t_r			—	30	—	ns
Output Fall Time (90-10%)	t_f			—	30	—	ns
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}	2	$R_L = 350\Omega$, $C_L = 15\text{pF}$ $I_F = 7.5\text{mA}$ $V_{EH} = 3.0\text{V}$ $V_{EL} = 0.5\text{V}$ Note 6 & 7	—	25	—	ns
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}			—	25	—	ns
Common Mode Transient Immunity at High Output Level	CM_H	3	$V_{CM} = 400\text{V}$ $R_L = 350\Omega$ $V_O(\text{min.}) = 2\text{V}$ $I_F = 0\text{mA}$, Note 9	1000	10000	—	$\text{V} / \mu\text{s}$
Common Mode Transient Immunity at Low Output Level	CM_L		$V_{CM} = 400\text{V}$ $R_L = 350\Omega$ $V_O(\text{max.}) = 0.8\text{V}$ $I_F = 7.5\text{mA}$ Note 8	−1000	−10000	—	$\text{V} / \mu\text{s}$

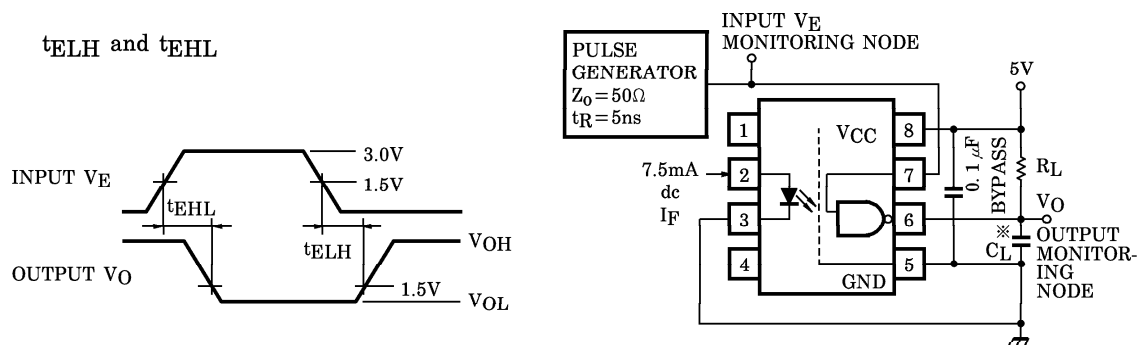
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TEST CIRCUIT 1.



※ C_L is approximately 15pF which includes probe and stray wiring capacitance.

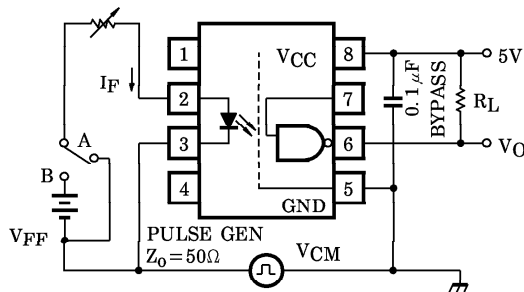
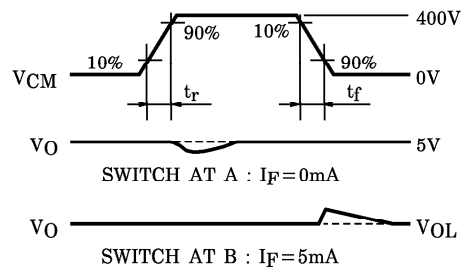
TEST CIRCUIT 2.



※ C_L is approximately 15pF which includes probe and stray wiring capacitance.

TEST CIRCUIT 3.

Transient Immunity and Typical Waveforms.

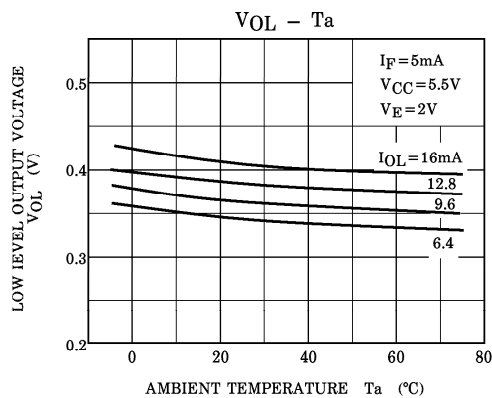
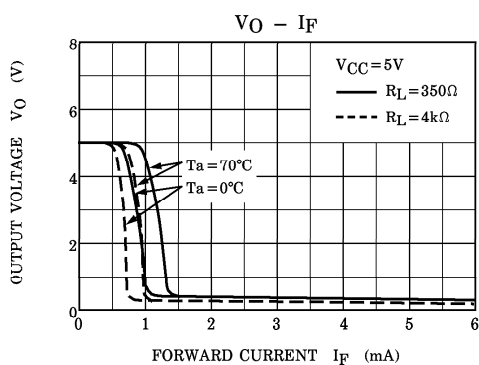
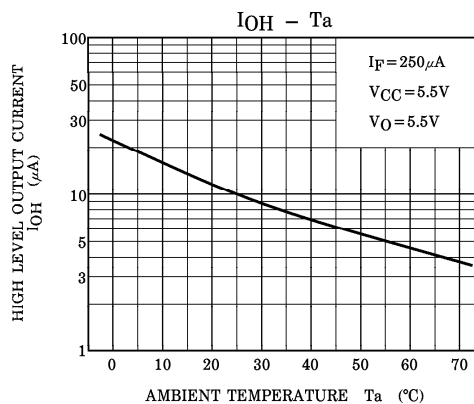
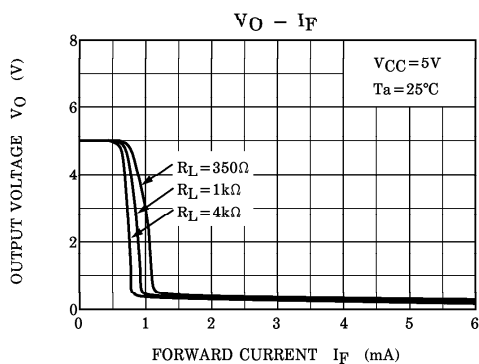
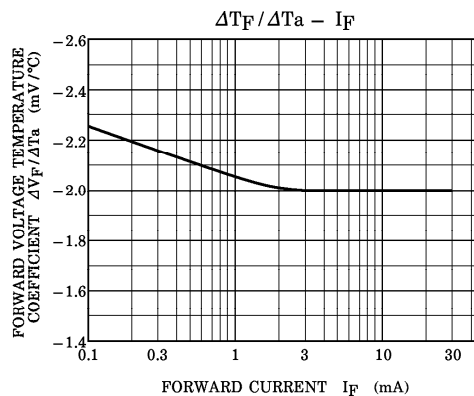
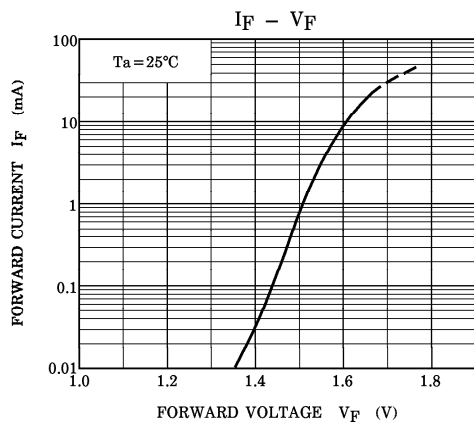


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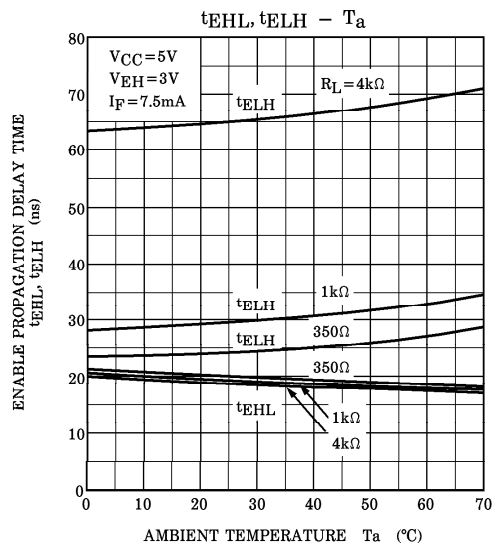
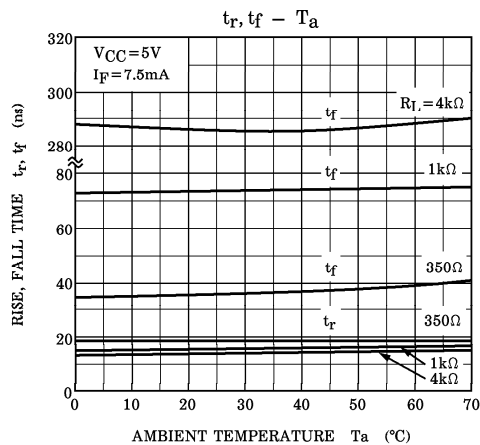
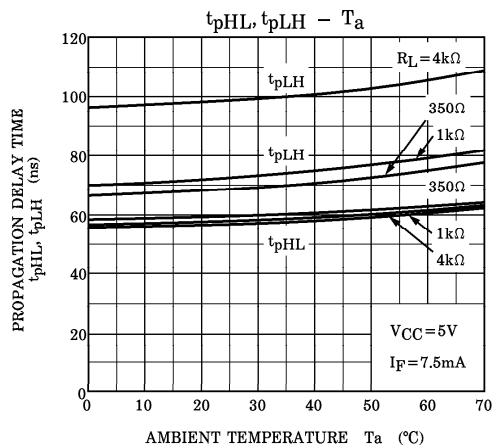
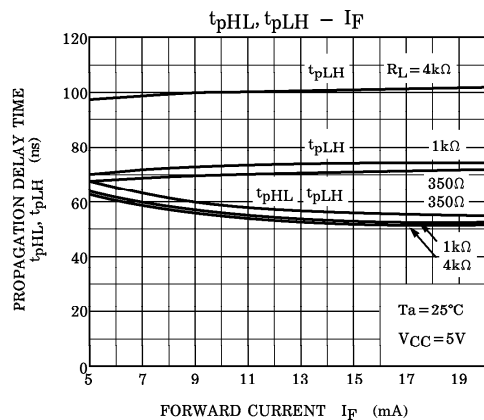


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NOTES

1. The V_{CC} supply voltage to each TLP2601 isolator must be bypassed by a $0.1\mu\text{F}$ capacitor of larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and GND pins of each device.
2. t_{pHL} • Propagation delay is measured from the 3.75mA level on the LOW to HIGH transition of the input current pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.
3. t_{pLH} • Propagation delay is measured from the 3.75mA level on the HIGH to LOW transition of the input current pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.
4. t_f • Fall time is measured from the 10% to the 90% levels of the HIGH to LOW transition on the output pulse.
5. t_r • Rise time is measured from the 90% to 10% levels of the LOW to HIGH transition on the output pulse.
6. t_{EHL} • Enable input propagation delay is measured from the 1.5V level on the LOW to HIGH transition of the input voltage pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.
7. t_{ELH} • Enable input propagation delay is measured from the 1.5V level on the HIGH to LOW transition of the input voltage pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.
8. CM_L • The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the low output state (i.e., $V_{OUT} < 0.8V$).
Measured in volts per microsecond ($V / \mu s$).
9. CM_H • The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the high state (i.e., $V_{OUT} > 2.0V$).
Measured in volts per microsecond ($V / \mu s$).
Volts/microsecond can be translated to sinusoidal voltages :

$$V / \mu s = \frac{(dV_{CM})}{dt} \text{ Max.} = f_{CM} V_{CM} \text{ (p.p.)}$$

Example :
 $V_{CM} = 318V_{pp}$ when $f_{CM} = 1\text{MHz}$ using CM_L and $CM_H = 1000V / \mu s$ data sheet specified minimum.
10. • Device considered a two-terminal device : Pins 1, 2, 3 and 4 shorted together, and Pins 5, 6, 7 and 8 shorted together.
11. Enable Input • No pull up resistor required as the device has an internal pull up resistor.

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