

EV34C6A5A1-17.664M TR

Lead Free  COMPLIANT	EU RoHS 2011/65 + 2015/863 COMPLIANT	ChinaRoHS  COMPLIANT	REACH SVHC 163 Jun 15, 2015 COMPLIANT
---	--	--	---



ITEM DESCRIPTION


Voltage Controlled Quartz Crystal Clock Oscillators VCXO LVCMOS (CMOS) 2.5Vdc 6 Pad 5.0mm x 7.0mm Ceramic Surface Mount (SMD) 17.664MHz ± 50 ppm Maximum 0°C to +70°C ± 100 ppm Minimum 10% Typical, 20% Maximum

ELECTRICAL SPECIFICATIONS

Nominal Frequency	17.664MHz
Frequency Tolerance/Stability	± 50 ppm Maximum (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, Shock, and Vibration.)
Aging at 25°C	± 2 ppm/First Year Typical, ± 10 ppm/10 Years Maximum
Operating Temperature Range	0°C to +70°C
Supply Voltage	2.5Vdc $\pm 5\%$
Input Current	15mA Maximum
Output Voltage Logic High (Voh)	90% of Vdd Minimum (IOH = -4mA)
Output Voltage Logic Low (Vol)	10% of Vdd Maximum (IOL = +4mA)
Rise/Fall Time	5nSec Maximum (Measured at 20% to 80% of Waveform)
Duty Cycle	50 ± 10 (%) (Measured at 50% of Waveform)
Load Drive Capability	15pF Maximum
Output Logic Type	CMOS
Absolute Pull Range	± 100 ppm Minimum (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, Shock, Vibration, and Aging over the Control Voltage (Vc).)
Control Voltage	0.2Vdc to 2.3Vdc (Test Condition for APR)
Control Voltage Range	0.0Vdc to Vdd
Linearity	10% Typical, 20% Maximum
Transfer Function	Positive Transfer Characteristic
Modulation Bandwidth	10kHz Minimum (Measured at -3dB, Vc = 1.25Vdc)
Input Impedance	50kOhms Minimum
Input Leakage Current	10 μ A Maximum
Phase Noise	All Values are Typical -65dBc/Hz at offset of 10Hz -95dBc/Hz at offset of 100Hz -120dBc/Hz at offset of 1kHz -142dBc/Hz at offset of 10kHz -152dBc/Hz at offset of 100kHz -154dBc/Hz at offset of 1MHz
Tri-State Input Voltage (Vih and Vil)	90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance)
RMS Phase Jitter	1pSec Maximum (Fj = 12kHz to 20MHz; Random)
Start Up Time	10mSec Maximum
Storage Temperature Range	-55°C to +125°C

ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

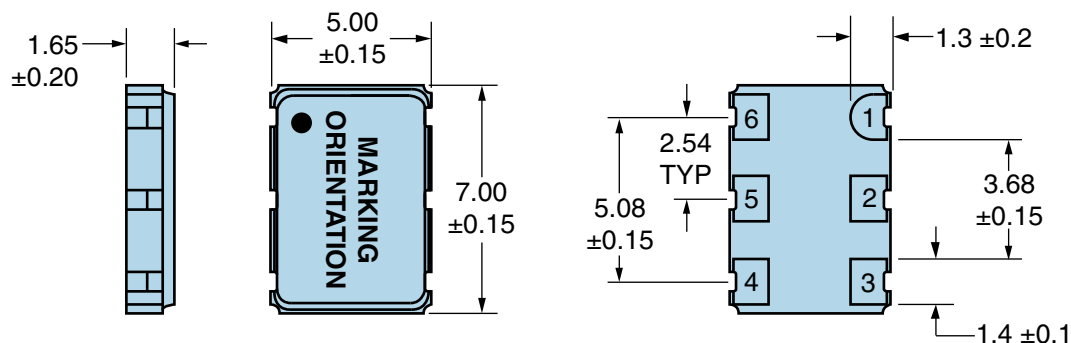
ESD Susceptibility	MIL-STD-883, Method 3015, Class 1, HBM: 1500V
Fine Leak Test	MIL-STD-883, Method 1014, Condition A
Flammability	UL94-V0
Gross Leak Test	MIL-STD-883, Method 1014, Condition C
Mechanical Shock	MIL-STD-883, Method 2002, Condition B
Moisture Resistance	MIL-STD-883, Method 1004

EV34C6A5A1-17.664M TR **ENVIRONMENTAL & MECHANICAL SPECIFICATIONS CONTINUED**

Moisture Sensitivity	J-STD-020, MSL 1
Resistance to Soldering Heat	MIL-STD-202, Method 210, Condition K
Resistance to Solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-883, Method 2003
Temperature Cycling	MIL-STD-883, Method 1010, Condition B
Vibration	MIL-STD-883, Method 2007, Condition A

EV34C6A5A1-17.664M TR

MECHANICAL DIMENSIONS (all dimensions in millimeters)

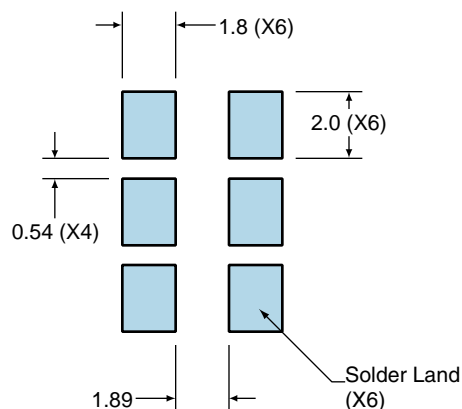


PIN	CONNECTION
1	Control Voltage
2	Tri-State
3	Case/Ground
4	Output
5	No Connect
6	Supply Voltage

LINE	MARKING
1	ECLIPTEK
2	17.664M
3	XXXXX XXXXX=Ecliptek Manufacturing Identifier

Suggested Solder Pad Layout

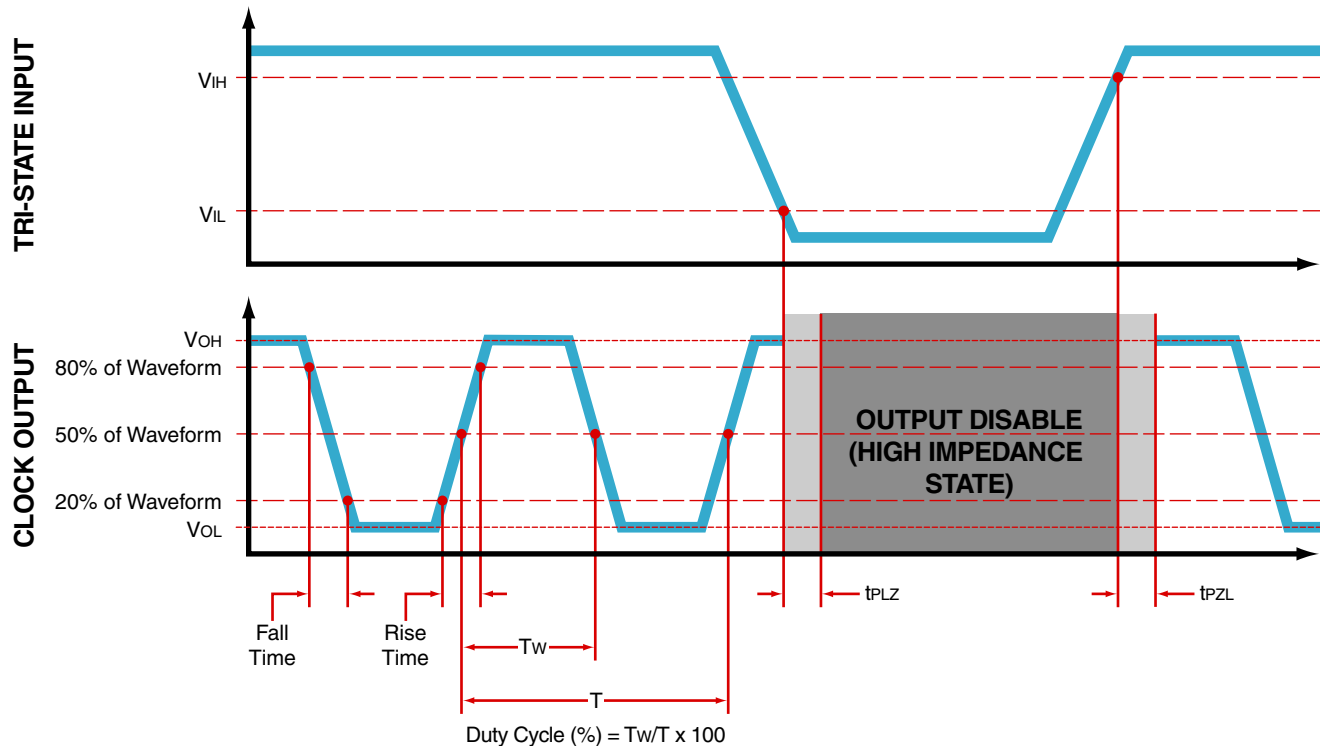
All Dimensions in Millimeters



All Tolerances are ±0.1

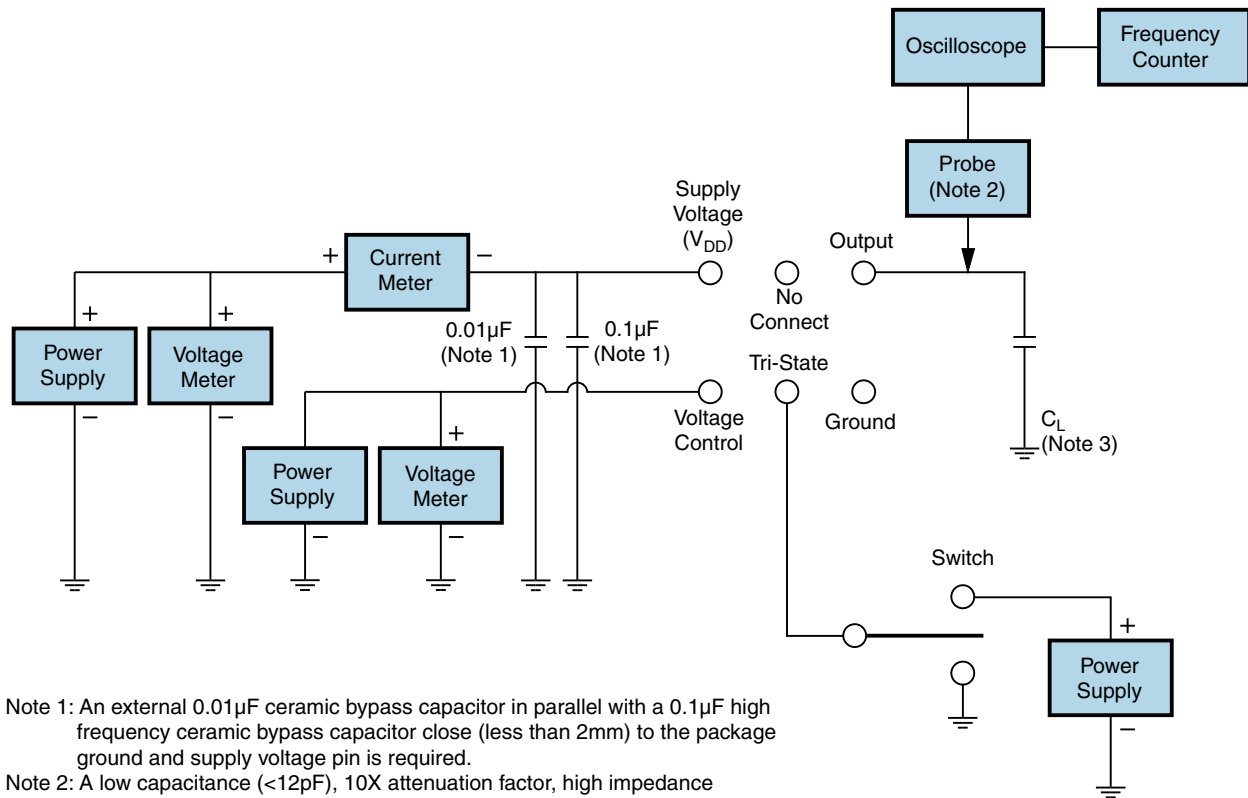
EV34C6A5A1-17.664M TR

OUTPUT WAVEFORM & TIMING DIAGRAM



EV34C6A5A1-17.664M TR

Test Circuit for CMOS Output



Note 1: An external $0.01\mu\text{F}$ ceramic bypass capacitor in parallel with a $0.1\mu\text{F}$ high frequency ceramic bypass capacitor close (less than 2mm) to the package ground and supply voltage pin is required.

Note 2: A low capacitance ($<12\text{pF}$), 10X attenuation factor, high impedance ($>10\text{Mohms}$), and high bandwidth ($>300\text{MHz}$) passive probe is recommended.

Note 3: Capacitance value C_L includes sum of all probe and fixture capacitance.

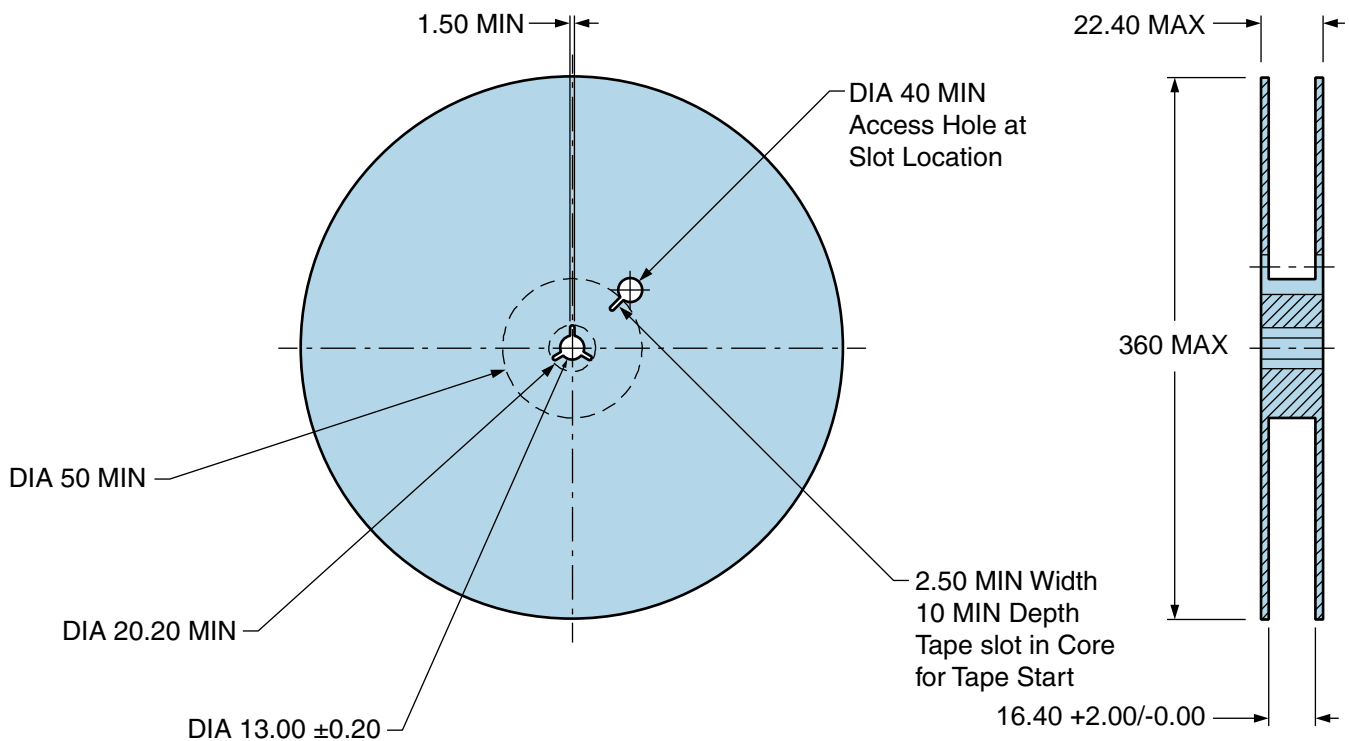
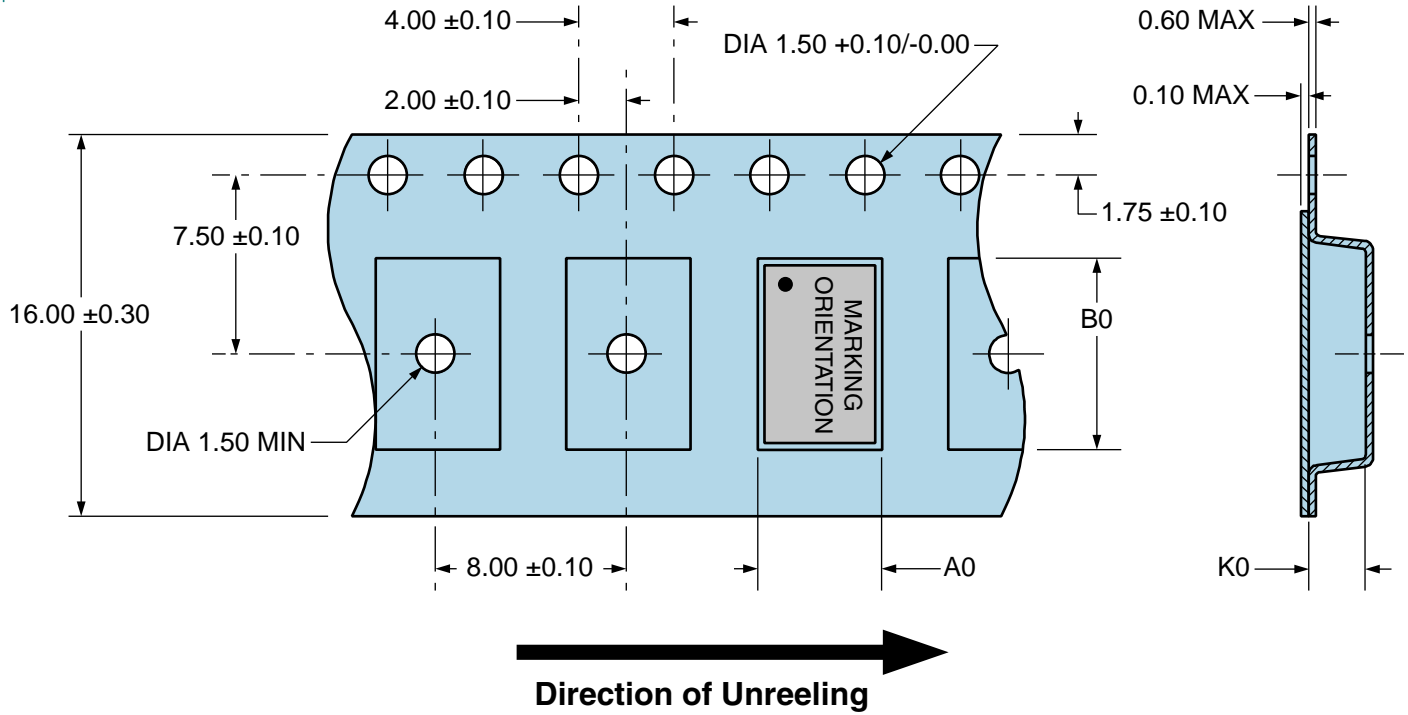
EV34C6A5A1-17.664M TR

Tape & Reel Dimensions

Quantity Per Reel: 1,000 units

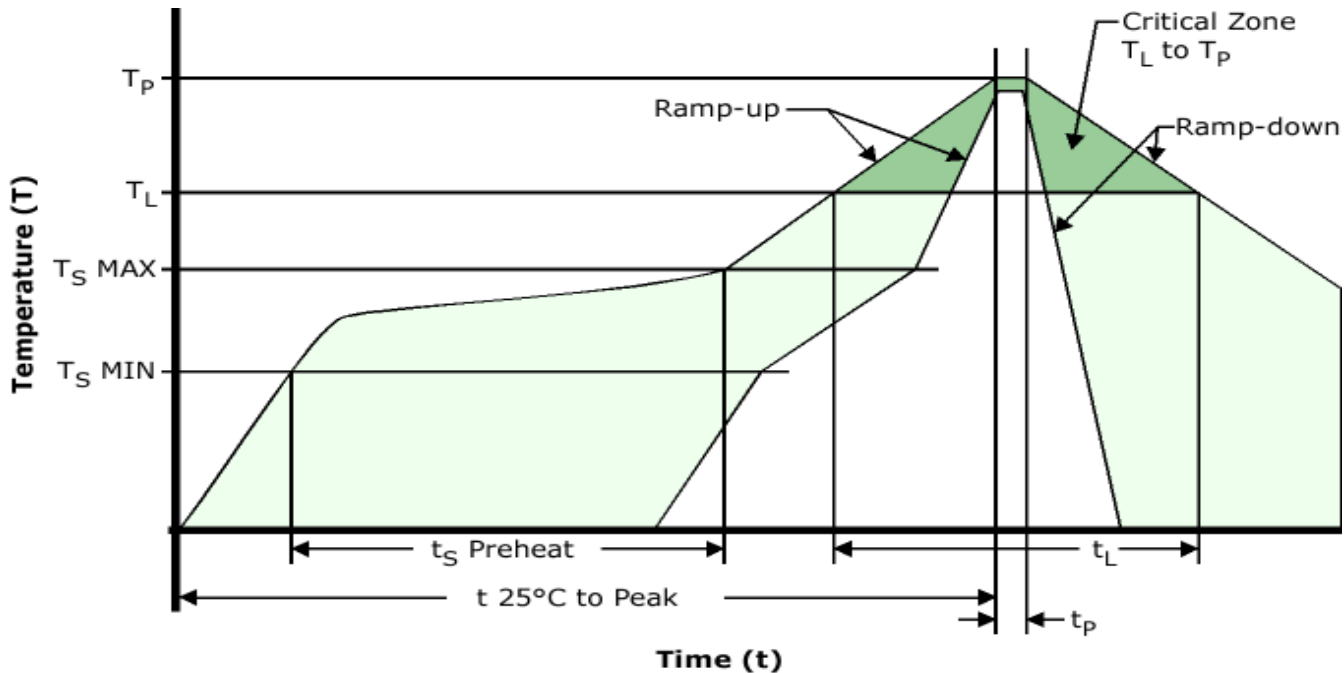
All Dimensions in Millimeters

Compliant to EIA-481



EV34C6A5A1-17.664M TR

Recommended Solder Reflow Methods



High Temperature Infrared/Convection

T_s MAX to T_L (Ramp-up Rate) 3°C/Second Maximum

Preheat

- Temperature Minimum (T_s MIN) 150°C
- Temperature Typical (T_s TYP) 175°C
- Temperature Maximum (T_s MAX) 200°C
- Time (t_s MIN) 60 - 180 Seconds

Ramp-up Rate (T_L to T_P) 3°C/Second Maximum

Time Maintained Above:

- Temperature (T_L) 217°C
- Time (t_L) 60 - 150 Seconds

Peak Temperature (T_P) 260°C Maximum for 10 Seconds Maximum

Target Peak Temperature (T_P Target) 250°C +0/-5°C

Time within 5°C of actual peak (t_p) 20 - 40 Seconds

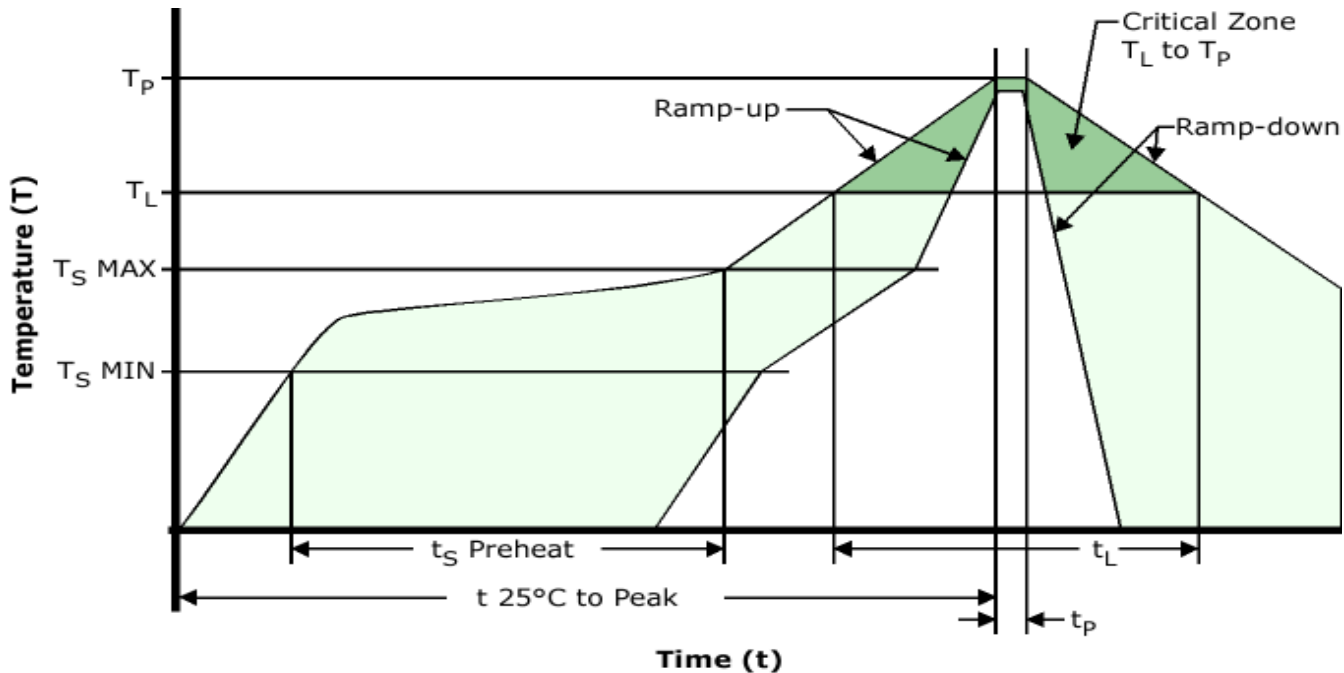
Ramp-down Rate 6°C/Second Maximum

Time 25°C to Peak Temperature (t) 8 Minutes Maximum

Moisture Sensitivity Level Level 1

EV34C6A5A1-17.664M TR [↗](#)

Recommended Solder Reflow Methods



Low Temperature Infrared/Convection 240°C

T_s MAX to T_L (Ramp-up Rate) 5°C/Second Maximum

Preheat

- Temperature Minimum (T_s MIN) N/A
- Temperature Typical (T_s TYP) 150°C
- Temperature Maximum (T_s MAX) N/A
- Time (t_s MIN) 60 - 120 Seconds

Ramp-up Rate (T_L to T_P) 5°C/Second Maximum

Time Maintained Above:

- Temperature (T_L) 150°C
- Time (t_L) 200 Seconds Maximum

Peak Temperature (T_P) 240°C Maximum

Target Peak Temperature (T_P Target) 240°C Maximum 2 Times / 230°C Maximum 1 Time

Time within 5°C of actual peak (t_p) 10 Seconds Maximum 2 Times / 80 Seconds Maximum 1 Time

Ramp-down Rate 5°C/Second Maximum

Time 25°C to Peak Temperature (t) N/A

Moisture Sensitivity Level Level 1

Low Temperature Manual Soldering

185°C Maximum for 10 Seconds Maximum, 2 times Maximum.

High Temperature Manual Soldering

260°C Maximum for 5 Seconds Maximum, 2 times Maximum.