

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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Not recommended  
for new design

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# HAT1043M

Silicon P Channel Power MOS FET  
Power Switching

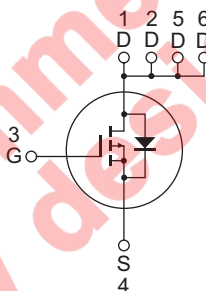
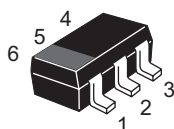
REJ03G1151-0600  
(Previous: ADE-208-754D)  
Rev.6.00  
Sep 07, 2005

## Features

- Low on-resistance
- Low drive current
- High density mounting
- 2.5 V gate drive device can be driven from 3 V source

## Outline

RENESAS Package code: PTSP0006FA-A  
(Package name: TSOP-6)



4 Source  
3 Gate  
1, 2, 5, 6 Drain

Not recommend  
for new design

## Absolute Maximum Ratings

(Ta = 25°C)

| Item                                   | Symbol   | Value       | Unit |
|--|--|-------------|------|
| Drain to source voltage                | V <sub>DSS</sub>                               | -20         | V    |
| Gate to source voltage                 | V <sub>GSS</sub>                               | ±12         | V    |
| Drain current                          | I <sub>D</sub>                                 | -4.4        | A    |
| Drain peak current                     | I <sub>D (pulse)</sub> <sup>Note 1</sup>       | -17.6       | A    |
| Body-drain diode reverse drain current | I <sub>DR</sub> <sup>Note 2</sup>              | -4.4        | A    |
| Channel dissipation                    | P <sub>ch (pulse)</sub> <sup>Note 2</sup>      | 2.0         | W    |
| Channel dissipation                    | P <sub>ch (continuous)</sub> <sup>Note 3</sup> | 1.05        | W    |
| Channel temperature                    | T <sub>ch</sub>                                | 150         | °C   |
| Storage temperature                    | T <sub>stg</sub>                               | -55 to +150 | °C   |

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%

2. When using the alumina ceramic board (50 × 50 × 0.7 mm), PW ≤ 5 s, Ta = 25°C

3. When using the alumina ceramic board (50 × 50 × 0.7 mm), Ta = 25°C

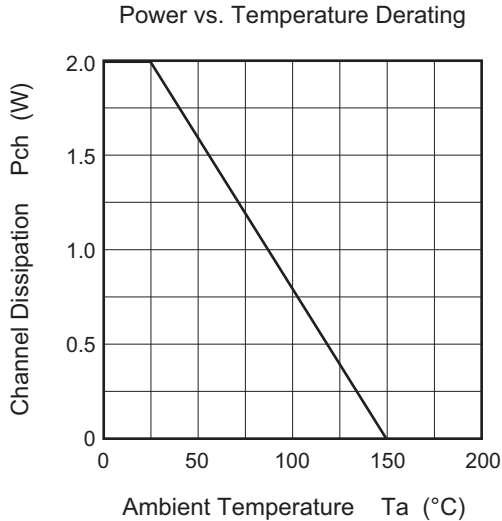
## Electrical Characteristics

(Ta = 25°C)

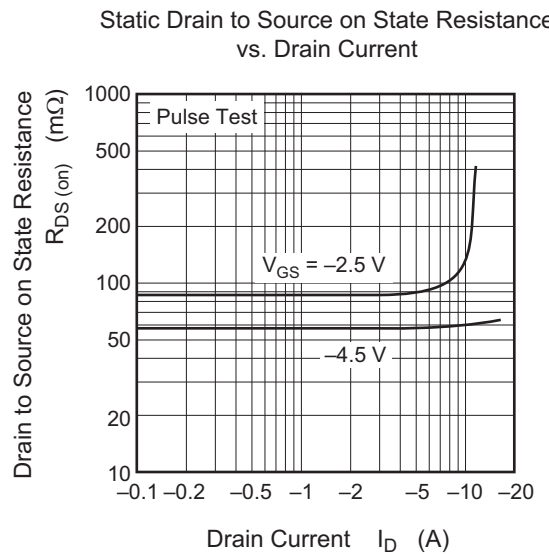
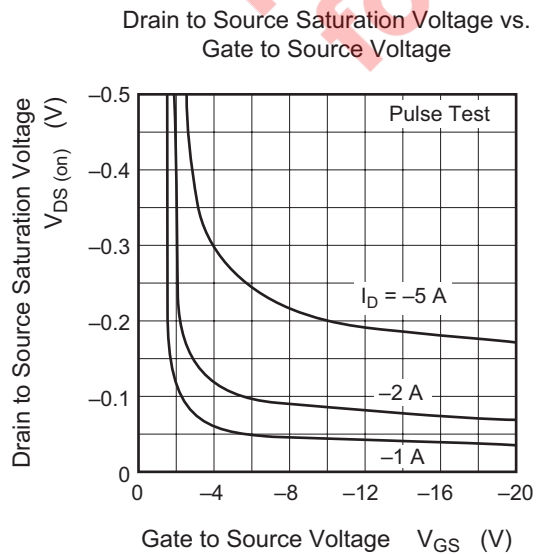
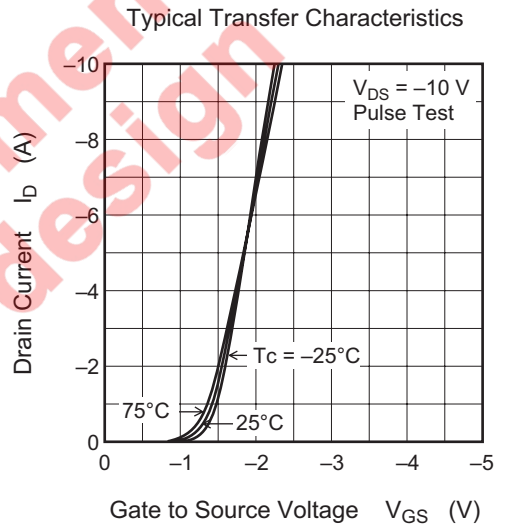
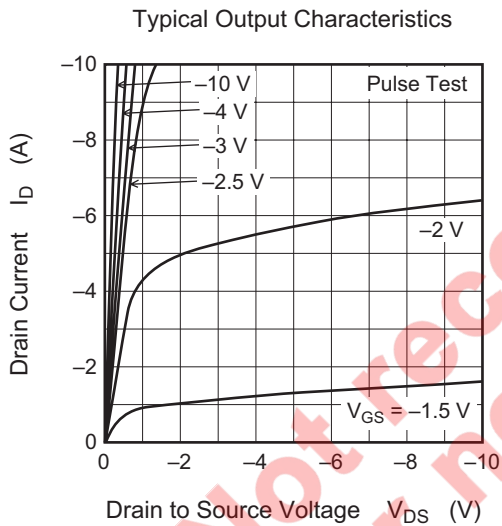
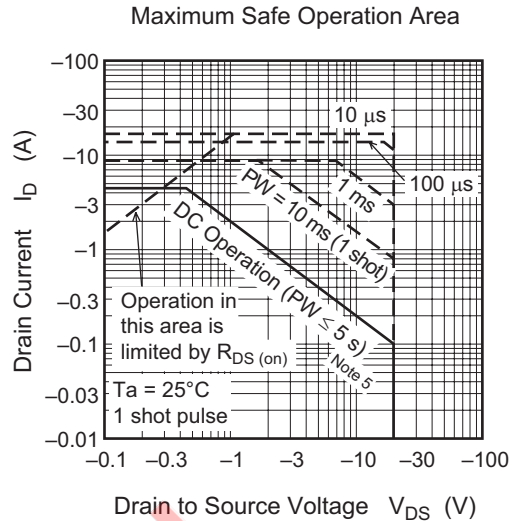
| Item                                       | Symbol                | Min  | Typ   | Max   | Unit | Test Conditions  |
|--|-----------------------|------|-------|-------|------|--|
| Drain to source breakdown voltage          | V <sub>(BR) DSS</sub> | -20  | —     | —     | V    | I <sub>D</sub> = -10 mA, V <sub>GS</sub> = 0                                   |
| Gate to source leak current                | I <sub>GSS</sub>      | —    | —     | ±0.1  | μA   | V <sub>GS</sub> = ±12 V, V <sub>DS</sub> = 0                                   |
| Zero gate voltage drain current            | I <sub>DSS</sub>      | —    | —     | -1    | μA   | V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0                                   |
| Gate to source cutoff voltage              | V <sub>GS (off)</sub> | -0.4 | —     | -1.4  | V    | I <sub>D</sub> = -1 mA, V <sub>DS</sub> = -10 V                                |
| Static drain to source on state resistance | R <sub>DS (on)</sub>  | —    | 55    | 65    | mΩ   | I <sub>D</sub> = -3 A, V <sub>GS</sub> = -4.5 V <sup>Note 4</sup>              |
|  | R <sub>DS (on)</sub>  | —    | 85    | 110   | mΩ   | I <sub>D</sub> = -3 A, V <sub>GS</sub> = -2.5 V <sup>Note 4</sup>              |
| Forward transfer admittance                | y <sub>fs</sub>       | 4    | 7     | —     | S    | I <sub>D</sub> = -3 A, V <sub>DS</sub> = -10 V <sup>Note 4</sup>               |
| Input capacitance                          | C <sub>iss</sub>      | —    | 750   | —     | pF   | V <sub>DS</sub> = -10 V  |
| Output capacitance                         | C <sub>oss</sub>      | —    | 310   | —     | pF   | V <sub>GS</sub> = 0  |
| Reverse transfer capacitance               | C <sub>rss</sub>      | —    | 220   | —     | pF   | f = 1 MHz  |
| Total gate charge                          | Q <sub>g</sub>        | —    | 11    | —     | nC   | V <sub>DD</sub> = -10 V  |
| Gate to source charge                      | Q <sub>gs</sub>       | —    | 2     | —     | nC   | V <sub>GS</sub> = -4.5 V   |
| Gate to drain charge                       | Q <sub>gd</sub>       | —    | 3.5   | —     | nC   | I <sub>D</sub> = -4.4 A  |
| Turn-on delay time                         | t <sub>d (on)</sub>   | —    | 15    | —     | ns   | V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -3 A,<br>R <sub>L</sub> = 3.3 Ω     |
| Rise time                                  | t <sub>r</sub>        | —    | 100   | —     | ns   |  |
| Turn-off delay time                        | t <sub>d (off)</sub>  | —    | 85    | —     | ns   |  |
| Fall time                                  | t <sub>f</sub>        | —    | 100   | —     | ns   |  |
| Body-drain diode forward voltage           | V <sub>DF</sub>       | —    | -0.95 | -1.23 | V    | I <sub>F</sub> = -4.4 A, V <sub>GS</sub> = 0                                   |
| Body-drain diode reverse recovery time     | t <sub>rr</sub>       | —    | 50    | —     | ns   | I <sub>F</sub> = -4.4 A, V <sub>GS</sub> = 0<br>di <sub>F</sub> /dt = -20 A/μs |

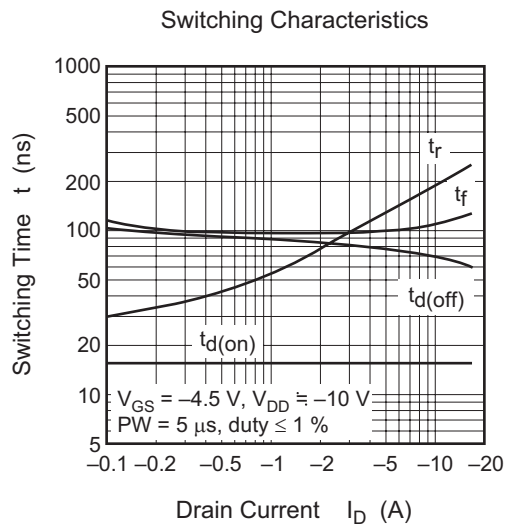
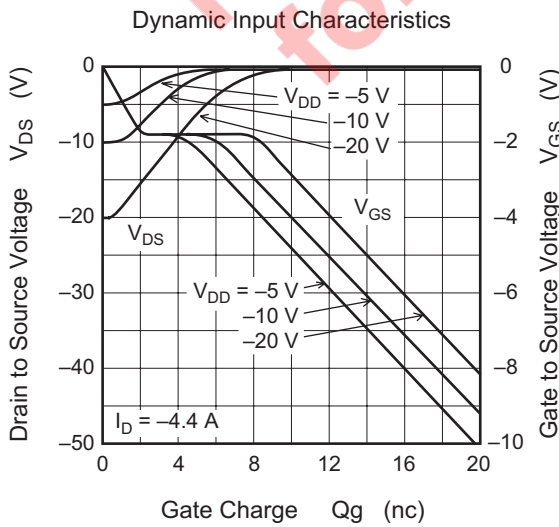
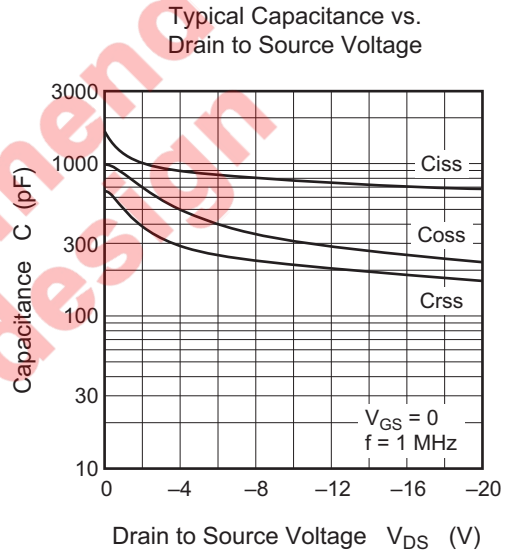
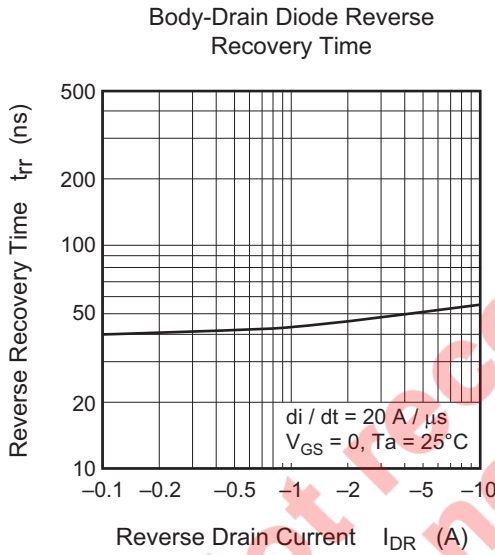
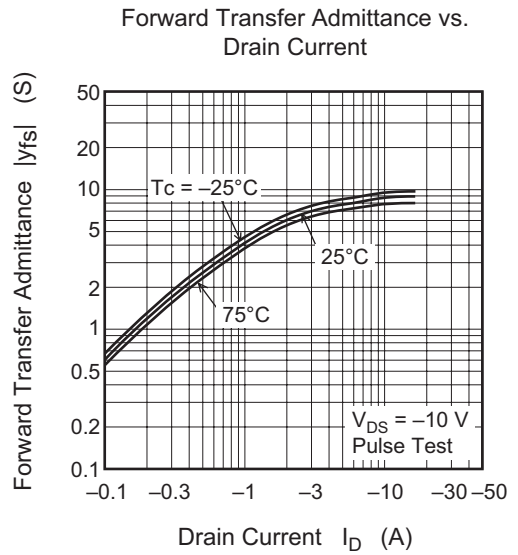
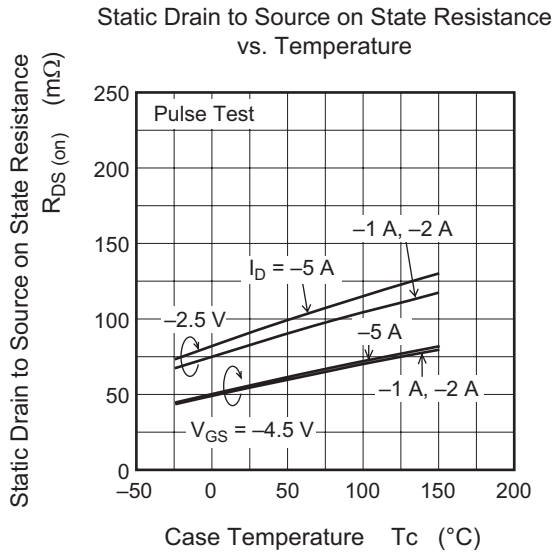
Note: 4. Pulse test

Main Characteristics

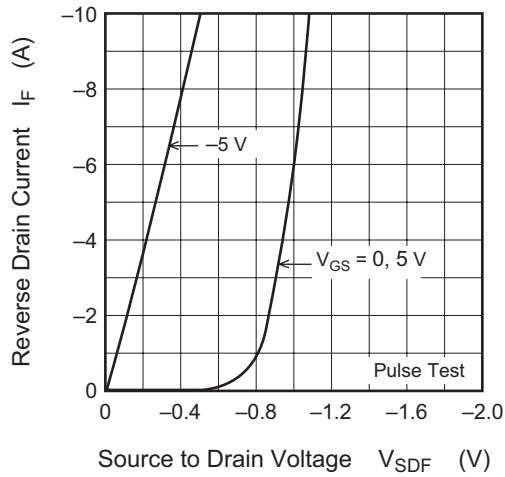


Test Condition:  
When using the alumina ceramic board  
(50 × 50 × 0.7 mm), ( $PW \leq 5$  s)

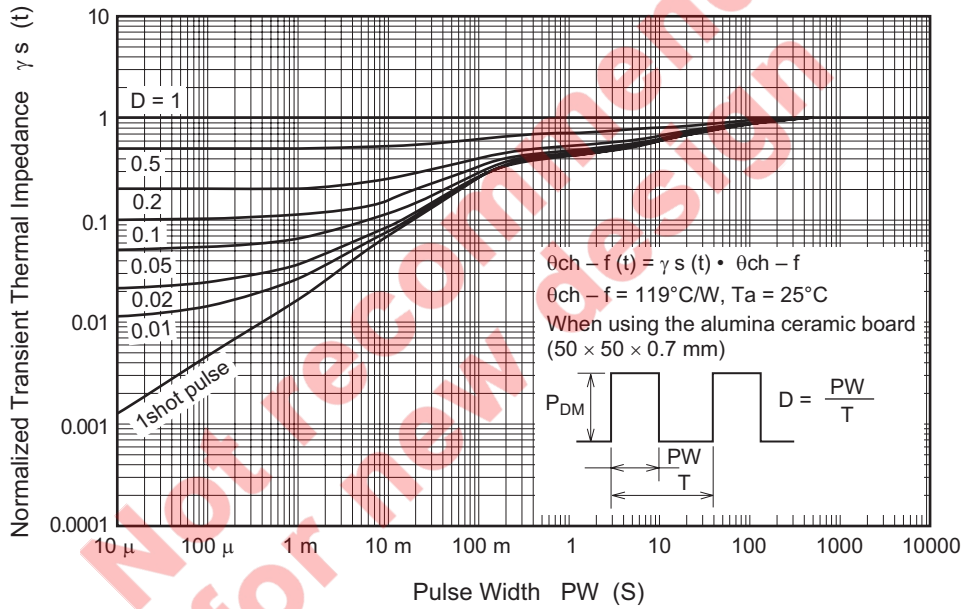




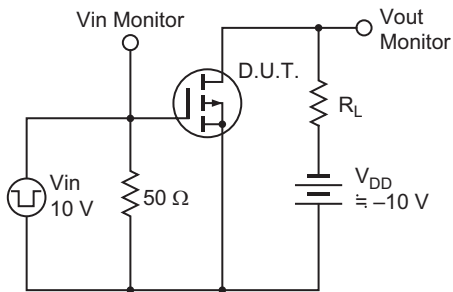
Reverse Drain Current vs. Source to Drain Voltage



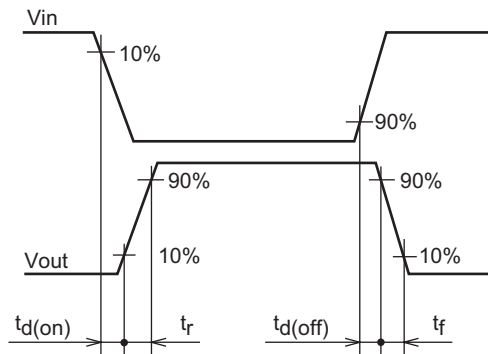
Normalized Transient Thermal Impedance vs. Pulse Width



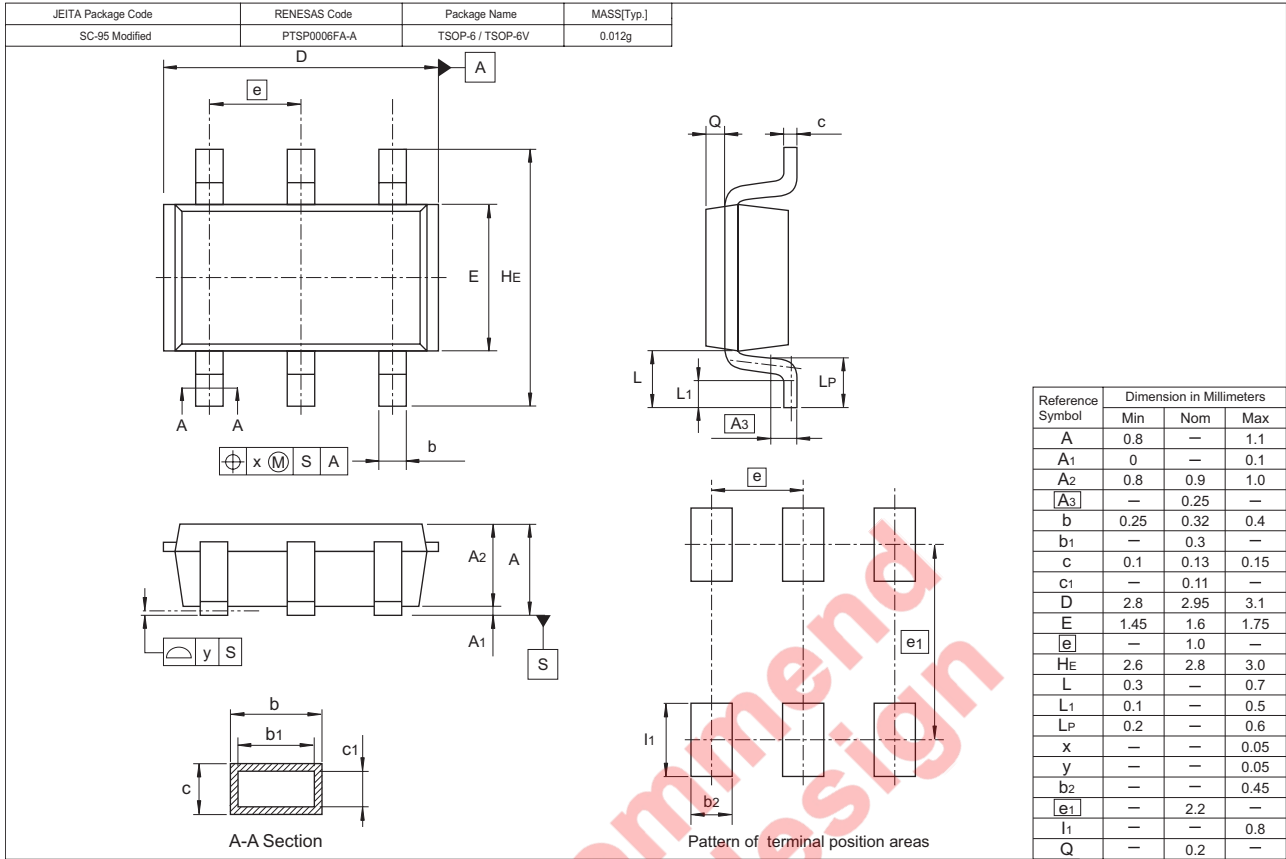
Switching Time Test Circuit



Switching Time Waveform



### Package Dimensions



### Ordering Information

| Part Name     | Quantity | Shipping Container |
|---------------|----------|--------------------|
| HAT1043M-EL-E | 3000 pcs | Taping             |

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