8253

Programmable Interval Timer
iAPX86 Family
MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

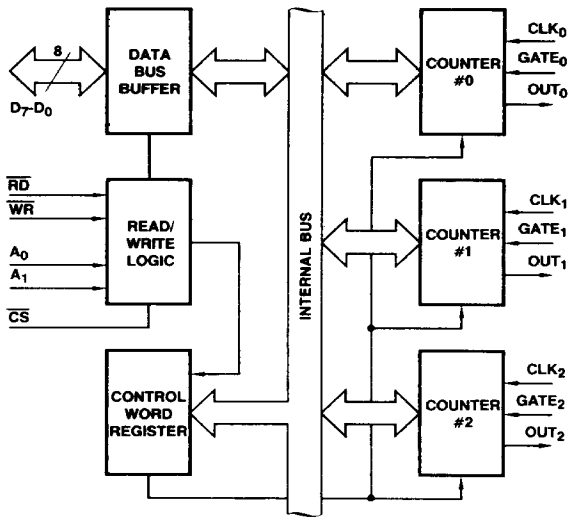
- SMD/DESC qualified
- Both Binary and BCD counting
- Single +5-V supply
- Three independent 16-bit counters
- DC to 5 MHz
- Programmable counter modes
- Bus-oriented I/O

GENERAL DESCRIPTION

The 8253 is a programmable counter/timer chip designed for use with 8080A/8085A microprocessors. It uses NMOS technology with a single +5-V supply and is a direct replacement for Intel's 8253/8253-5.

Each device is organized as three independent 16-bit counters, each counter having a rate of up to 5 MHz. All modes of operation are software-programmable. For improved performance devices, see the Am9513A System Timing Controller.

BLOCK DIAGRAM

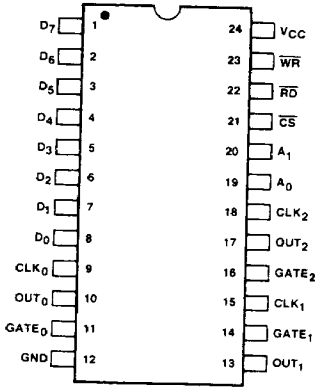


BD003760

Power Supplies { +5 V, GND

Publication # 07935 | Rev. B | Amendment /0
Issue Date: November 1987

CONNECTION DIAGRAM
Top View



CD005671

Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

Standard Military Drawing (SMD)/DESC Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. Standard Military Drawing (SMD)/DESC products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for SMD/DESC products is formed by a combination of: **a. Military Drawing Part Number**
b. Device Type
c. Case Outline
d. Lead Finish

5962-87520 01 J X

- **d. LEAD FINISH**
  X = Any Lead Finish Acceptable
- **c. CASE OUTLINE**
  J = 24-Pin Ceramic DIP (CD 024)
- **b. MILITARY DEVICE TYPE**
  01 = 2.6 MHz; t_{RD} = 300 ns (8253)
  03 = 2.6 MHz; t_{RD} = 200 ns (8253-5)
- **a. MILITARY DRAWING NO./DESCRIPTION**
  5962-87520
  Programmable Interval Timer

Valid Combinations	
5962-8752001	JX
5962-8752003	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

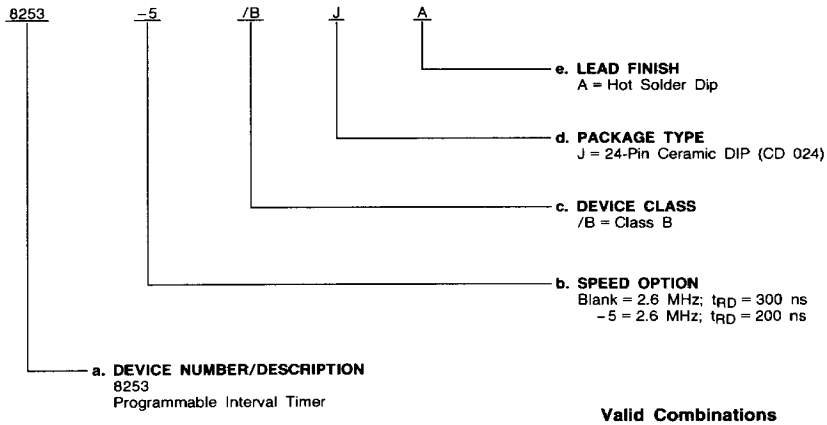
Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

MILITARY ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
8253	/BJA
8253-5	

Group A Tests
Group A Tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage On Any Pin
with Respect to Ground ..... −0.5 to +7.0 V
Power Dissipation ..... 1 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C) ..... −55 to 125°C
Supply Voltage (V_{CC}) ..... 5 V ±10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

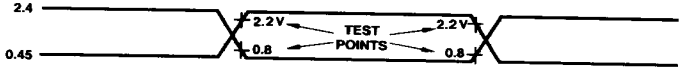
Parameter Symbol	Parameter Description	Test Conditions	8253-5		8253		Unit
			Min.	Max.	Min.	Max.	
V_{IL}	Input LOW Voltage	V_{CC} = 5 V ±10%	−.5*	.7	−.5*	.7	V
V_{IH}	Input HIGH Voltage	V_{CC} = 5 V ±10%	2.2	V_{CC} + .5 V*	2.2	V_{CC} + .5 V*	V
V_{OL}	Output LOW Voltage	I_{OL} = 1.6 mA, V_{CC} = 5 V ±10%		0.45		0.45	V
V_{OH}	Output HIGH Voltage	I_{OH} = −150 μA, V_{CC} = 5 V ±10%	2.4		2.4		V
I_{IL}	Input Load Current	V_{IN} = V_{CC} to 0 V, V_{CC} = Max.		±20		±20	μA
I_{OFL}	Output Float Leakage	V_{OUT} = V_{CC} to 0 V, V_{CC} = Max.		±20		±20	μA
I_{CC}	V_{CC} Supply Current	V_{CC} = Max., Outputs Unloaded (Static) (Note 1)		140		140	mA

CAPACITANCE T_C = 25°C; f_c = 1 MHz; V_{CC} = GND = 0 V

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN} †	Input Capacitance	f_c = 1 MHz			10*	pF
$C_{I/O}$ †	I/O Capacitance	Unmeasured pins returned to V_{SS}			20*	pF

*Guaranteed by design; not tested.
†Not included in Group A tests.

SWITCHING TEST WAVEFORM



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Input

See Section 6 of the MOS Microprocessors and Peripherals Data Book (Order #09067A) for Thermal Characteristics information.

SWITCHING CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Note 2)

No.	Parameter Symbol	Parameter Description	8253 Min.	8253 Max.	8253-5 Min.	8253-5 Max.	Unit
READ CYCLE							
1	t_{AR}	Address Stable Before $\overline{READ}$	50		30		ns
2	t_{RA}	Address Hold Time for $\overline{READ}$	5		5		ns
3	t_{RR}	$\overline{READ}$ Pulse Width	400		300		ns
4	t_{RD} (Note 3)	Data Delay from $\overline{READ}$		300		200	ns
5	t_{DF}	$\overline{READ}$ to Data Floating	35	175	25	100	ns
6	t_{RV}	Recovery Time Between $\overline{READ}$ and Any Other Control Signal	1		1		μs
WRITE CYCLE							
7	t_{AW}	Address Stable Before $\overline{WRITE}$	50		30		ns
8	t_{WA}	Address Hold Time for $\overline{WRITE}$	30		30		ns
9	t_{WW}	$\overline{WRITE}$ Pulse Width	400		300		ns
10	t_{DW}	Data Setup Time for $\overline{WRITE}$	300		250		ns
11	t_{WD}	Data Hold Time for $\overline{WRITE}$	40		30		ns
12	t_{RV}	Recovery Time Between $\overline{WRITE}$ and Any Other Control Signal	1		1		μs
CLOCK AND GATE TIMING (Note 2)							
13	t_{CLK}	Clock Period	380	DC	380	DC	ns
14	t_{PWH}	HIGH Pulse Width	230		230		ns
15	t_{PWL}	LOW Pulse Width	150		150		ns
16	t_{GW}	Gate Width HIGH	150		150		ns
17	t_{GL}	Gate Width LOW	100		100		ns
18	t_{GS}	Gate Setup Time to CLK↑	100		100		ns
19	t_{GH}	Gate Hold Time After CLK↑	55		55		ns
20	t_{OD} (Note 3)	Output Delay from CLK↓		400		400	ns
21	t_{ODG} (Note 3)	Output Delay from Gate↓		300		300	ns

Notes: 1. I_{CC} is measured in a static condition with no output loads applied.
2. Test Conditions: $V_{CC} = 5\ V \pm 10\%$
$V_{IL} = 0.45\ V$, $V_{IH} = 2.4\ V$
$V_{OL} = 0.8\ V$, $V_{OH} = 2.2\ V$
$I_{OL} = 1.6\ mA$, $I_{OH} = 150\ \mu A$
3. Test Condition: $C_L = 100\ pF \pm 20\ pF$.