High Efficiency Integrated Power Solution for Multicell Lithium Ion Applications

Data Sheet **ADP5080**

FEATURES

- **Wide input voltage range: 4.0 V to 15 V**
- **High efficiency architecture**
- **Up to 2 MHz switching frequency**
- **6 synchronous rectification dc-to-dc converters**
  - **Channel 1 buck regulator: 3 A maximum**
  - **Channel 2 buck regulator: 1.15 A maximum**
  - **Channel 3 buck regulator: 1.5 A maximum**
  - **Channel 4 buck regulator: 0.8 A maximum**
  - **Channel 5 buck regulator: 2 A maximum**
  - **Channel 6 configurable buck or buck boost regulator**
    - **2 A maximum for buck regulator configuration**
    - **1.5 A maximum for buck boost regulator configuration**
  - **Channel 7 high voltage, high performance LDO regulator: 30 mA maximum**
- **2 low quiescent current keep-alive LDO regulators**
  - **LDO1 regulator: 400 mA maximum**
  - **LDO2 regulator: 300 mA maximum**
- **Control circuit**
  - **Charge pump for internal switching driver power supply**
  - **I²C-programmable output levels and power sequencing**
- **Package: 72-ball, 4.5 mm × 4.0 mm × 0.6 mm WLCSP (0.5 mm pitch)**

APPLICATIONS

- **DSLR cameras**
- **Non-reflex (mirrorless) cameras**
- **Portable instrumentation**

FUNCTIONAL BLOCK DIAGRAM

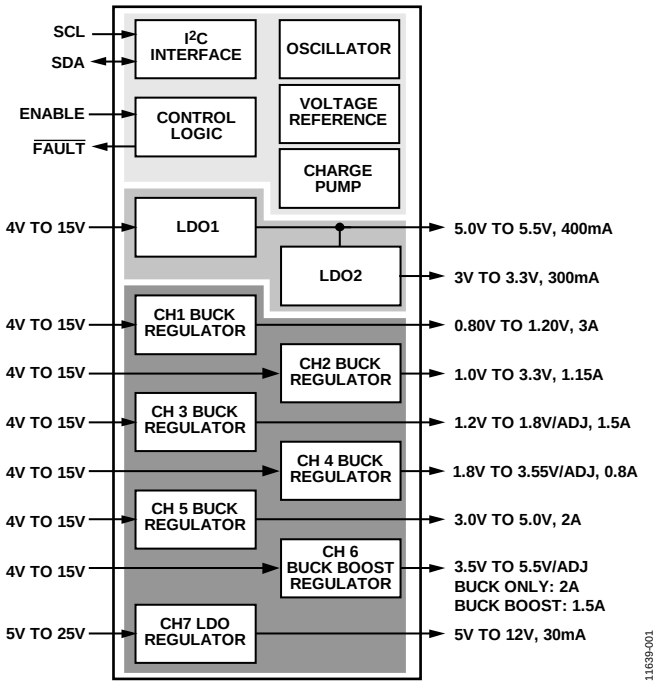

Figure 1.

GENERAL DESCRIPTION

The ADP5080 is a fully integrated, high efficiency power solution for multicell lithium ion battery applications. The device can connect directly to the battery, which eliminates the need for preregulators and, therefore, increases the battery life of the system.

The ADP5080 integrates two keep-alive LDO regulators, five synchronous buck regulators, a configurable four-switch buck boost regulator, and a high voltage LDO regulator. The ADP5080 is a highly integrated power solution that incorporates all power MOSFETs, feedback loop compensation, voltage setting resistor dividers, and discharge switches, as well as a charge pump to generate a global bootstrap voltage.

All these features help to minimize the number of external components and PCB space required, providing significant advantages for portable applications. The switching frequency is selectable on each channel from 750 kHz to 2 MHz.

Key functions for power applications, such as soft start, selectable preset output voltage, and flexible power-up and power-down sequences, are provided on chip and are programmable via the I²C interface with fused factory defaults. The ADP5080 is available in a 72-ball WLCSP 0.5 mm pitch package.

Rev. A Document Feedback

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- ADP5080 Evaluation Board

DOCUMENTATION

Data Sheet

- ADP5080: High Efficiency Integrated Power Solution for Multicell Lithium Ion Applications Data Sheet

User Guides

- UG-752: Operating the ADP5080 High Efficiency, 6-Channel PMU Evaluation Board
- UG-773: Installing the ADP5080 Evaluation Board Hardware and Software

TOOLS AND SIMULATIONS

- ADIsimPower™ Voltage Regulator Design Tool

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- ADP5080 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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REVISION HISTORY

4/14—Revision A: Initial Version

SPECIFICATIONS

T_J = 25°C, V_{VBATT} = 7.2 V, V_{VREG1} = V_{VDRx} = 5 V, V_{VREG2} = V_{VDDIO} = 3.3 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT SUPPLY VOLTAGE RANGE						
VBATT	V_{VBATT}	4.0		15	V	Applies to PVIN1, PVIN2, PVIN3, PVIN4, PVIN5, and PVIN6
VILDO7	V_{VILDO7}	5		25	V	
VDDIO	V_{VDDIO}	1.6		3.6	V	
QUIESCENT CURRENT						
Operating Quiescent Current	$I_{Q\ (VIN)}$		8	11	mA	All channels on, nonswitching
VDDIO	$I_{Q\ (VDDIO\_OP)}$		0.2		µA	V_{VDDIO} = V_{SCL} = V_{SDA} = 3.3 V
Standby Current	$I_{Q\ (VBATT\_STNBY1)}$		12	20	µA	Includes LDO1 and LDO2, EN low
	$I_{Q\ (VBATT\_STNBY2)}$		1.25		mA	All channels off, EN high, SEL_FSW = 1, FREQ_CP = 01
UNDERVOLTAGE LOCKOUT	UVLO					
UVLO Rising Threshold	$V_{UVLO\ (R)}$	3.45	3.7	3.85	V	At PVIN1
UVLO Falling Threshold	$V_{UVLO\ (F)}$		3.45	3.55	V	At PVIN1
VBATT UVLO Threshold	$V_{UVLO\ (BATT)}$		3.3		V	At VBATT, falling
Reset Threshold	$V_{UVLO\ (POR)}$		2.4		V	At VREG2, falling
OSCILLATOR CIRCUIT						
Switching Frequency	f_{SW}	1.98	2.0	2.02	MHz	R_{OSC} = 100 kΩ, SEL_FSW = 0
		1.48	1.5	1.52	MHz	R_{OSC} = 100 kΩ, SEL_FSW = 1
SYNC Pin, Input Clock						
Frequency Range	f_{SYNC}	0.5		2.0	MHz	R_{OSC} = 100 kΩ
Minimum On Pulse Width	$t_{SYNC\_MIN\_ON}$	100			ns	
Minimum Off Pulse Width	$t_{SYNC\_MIN\_OFF}$	100			ns	
High Logic	$V_{H\ (SYNC)}$			0.8 × V_{VREG2}	V	V_{VREG2} = 3.3 V, −25°C ≤ T_J ≤ +85°C
Low Logic	$V_{L\ (SYNC)}$	0.3 × V_{VREG2}			V	V_{VREG2} = 3.3 V, −25°C ≤ T_J ≤ +85°C
LOGIC INPUTS						
EN Pin						
High Level Threshold	$V_{IH\ (EN)}$			2.15	V	V_{VREG2} = 3.3 V, −25°C ≤ T_J ≤ +85°C
Low Level Threshold	$V_{IL\ (EN)}$	1.45			V	V_{VREG2} = 3.3 V, −25°C ≤ T_J ≤ +85°C
EN34 Pin						
High Level Threshold	$V_{IH\ (EN34)}$			1.25	V	V_{VREG2} = 3.3 V, −25°C ≤ T_J ≤ +85°C
Low Level Threshold	$V_{IL\ (EN34)}$	0.70			V	V_{VREG2} = 3.3 V, −25°C ≤ T_J ≤ +85°C
SCL and SDA Pins						
High Level Threshold	$V_{IH\ (I2C)}$			0.75 × V_{VDDIO}	V	V_{VDDIO} = 3.3 V, −25°C ≤ T_J ≤ +85°C
Low Level Threshold	$V_{IL\ (I2C)}$	0.3 × V_{VDDIO}			V	V_{VDDIO} = 3.3 V, −25°C ≤ T_J ≤ +85°C
LOGIC OUTPUTS						
SDA Pin						
Low Level Output Voltage	$V_{OL\ (SDA)}$			0.4	V	3.0 mA sink current, −25°C ≤ T_J ≤ +85°C
Leakage Current	$I_{LEAK\ (SDA)}$		10		nA	V_{SDA} = 3.3 V
CLKO Pin						
High Level Output Voltage	$V_{OH\ (CLKO)}$	V_{VREG2} − 0.4			V	3.0 mA sink current, −25°C ≤ T_J ≤ +85°C
Low Level Output Voltage	$V_{OL\ (CLKO)}$			0.4	V	3.0 mA sink current, −25°C ≤ T_J ≤ +85°C
$\overline{\text{FAULT}}$ Pin						
Low Level Output Voltage	$V_{OL\ (\overline{FAULT})}$			0.4	V	3.0 mA source current, −25°C ≤ T_J ≤ +85°C
Leakage Current	$I_{LEAK\ (\overline{FAULT})}$		10		nA	$V_{\overline{FAULT}}$ = 3.3 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER GOOD						
Rising Threshold	$V_{PGOOD\ (R)}$		83		%	Measured at V_{OUT}
Falling Threshold	$V_{PGOOD\ (F)}$		79		%	Measured at V_{OUT}
OVERVOLTAGE/UNDERVOLTAGE						
OVP Threshold	V_{OVP}		125	137	%	Measured at V_{OUT}
UVP Threshold	V_{UVP}	48	65		%	Measured at V_{OUT}
THERMAL SHUTDOWN	TSD					
Rising Threshold	T_{TSD}		165		°C	
Hysteresis	T_{TSD_HYS}		15		°C	

HOUSEKEEPING BLOCK SPECIFICATIONS

T_J = 25°C, V_{VBATT} = 7.2 V, V_{VREG1} = V_{VDRx} = 5 V, V_{VREG2} = V_{VDDIO} = 3.3 V, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LDO1						
Output Voltage (VREG1 Pin)						
Fixed Voltage Range, 1 Bit	V_{VREG1}	5.0		5.5	V	V_{VBATT} = V_{VREG1} + 0.5 V, I_{VREG1} = 10 mA
Voltage Accuracy	$V_{VREG1\ (DEFAULT)}$	−2		+2	%	V_{VBATT} = V_{VREG1} + 0.5 V, I_{VREG1} = 10 mA
Load Regulation	$\Delta V_{VREG1}/I_{VREG1}$		3.5		%/A	I_{VREG1} = 4 mA to 95 mA
Line Regulation	$\Delta V_{VREG1}/V_{VBATT}$		0.03		%/V	V_{VBATT} = (V_{VREG1} + 0.5 V) to 15 V
Current-Limit Threshold	I_{LDO1_ILIM}	390	550		mA	V_{VREG1} = 90% of nominal
Dropout Voltage			0.15		V	I_{VREG1} = 100 mA, V_{VREG1} = 5 V
Input Select Switch On Resistance	R_{DSON_VISW1}		795		mΩ	V_{VISW1} = 5 V
C_{OUT} Discharge Switch On Resistance	R_{DIS_LDO1}		1		kΩ	V_{VREG1} = 1 V
LDO2						
Output Voltage (VREG2 Pin)						
Fixed Voltage Range, 2 Bits	V_{VREG2}	3.0		3.3	V	I_{VREG2} = 10 mA
Voltage Accuracy	$V_{VREG2\ (DEFAULT)}$	−2		+2	%	I_{VREG2} = 10 mA
Load Regulation	$\Delta V_{VREG2}/I_{VREG2}$		5.5		%/A	I_{VREG2} = 4 mA to 95 mA
Current-Limit Threshold	I_{LDO2_ILIM}	290	400		mA	V_{VREG2} = 90% of nominal
Input Select Switch On Resistance	R_{DSON_VISW2}		1409		mΩ	V_{VISW2} = 3.3 V
C_{OUT} Discharge Switch On Resistance	R_{DIS_LDO2}		12		Ω	V_{VREG2} = 1 V
CHARGE PUMP						
C+ Switch On Resistance						
Low-Side	R_{DSON_C+SW1}		1.1		Ω	Source, PVINCP to C+
High-Side	R_{DSON_C+SW2}		1.0		Ω	Sink, C+ to BSTCP
C− Switch On Resistance						
High-Side	R_{DSON_C-SW1}		1.0		Ω	Source, VDR5 to C−
Low-Side	R_{DSON_C-SW2}		785		mΩ	Sink, C− to PGND5
Shunt Switch On Resistance	R_{DSON_CP}		3.3		Ω	BSTCP to PVINCP, EN low
Charge Pump Start-Up Threshold	CP_{START}		4.0		V	At VBATT

DC-TO-DC CONVERTER BLOCK SPECIFICATIONS

T_J = 25°C, V_{VBATT} = 7.2 V, V_{VREG1} = V_{VDRx} = 5 V, V_{VREG2} = V_{VDDIO} = 3.3 V, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CHANNEL 1 SYNC BUCK REGULATOR						
Channel 1 Output Voltage (FB1 Pin)						
Fixed Voltage Range, 5 Bits	V_{FB1}	0.89		1.20	V	REDUCE_VOUT1 = 0
		0.80		1.11	V	REDUCE_VOUT1 = 1
Feedback Voltage Accuracy at Default VID Code	$V_{FB1\ (DEFAULT)}$	−0.8		+0.8	%	
		−1.3		+1.3	%	−25°C ≤ T_J ≤ +85°C
Load Regulation	$\Delta V_{FB1}/I_{LOAD1}$		0.15		%/A	I_{LOAD1} = 20 mA to 2 A, AUTO-PSM1 = 0
Line Regulation	$\Delta V_{FB1}/V_{PVIN1}$		0.004		%/V	V_{PVIN1} = 5 V to 15 V, I_{LOAD} = 1 A
SW1A Pin						
High-Side Power FET On Resistance	R_{DSON_1AH}		250		mΩ	I_D = 100 mA
Low-Side Power FET On Resistance	R_{DSON_1AL}		130		mΩ	I_D = 100 mA
SW1B Pin						
High-Side Power FET On Resistance	R_{DSON_1BH}		175		mΩ	I_D = 100 mA, GATE_SCAL1 = 0
Low-Side Power FET On Resistance	R_{DSON_1BL}		95		mΩ	I_D = 100 mA
SW1A and SW1B Pins						
Switch Current Limit	I_{CL1}	3.1	4.0		A	Valley current, −25°C ≤ T_J ≤ +85°C
Minimum Off Time	$t_{OFF1\ (MIN)}$		115		ns	
Minimum Duty Cycle	D_{MIN1}		0		%	
Soft Start Time	t_{SS1}		4		ms	SS1 = 10
C_{OUT} Discharge Switch On Resistance	R_{DIS1}		125		Ω	V_{FB1} = 1 V
CHANNEL 2 SYNC BUCK REGULATOR						
Channel 2 Output Voltage (FB2 Pin)						
Fixed Voltage Range, 4 Bits	V_{FB2}	1.0		3.3	V	
Feedback Voltage Accuracy at Default VID Code	$V_{FB2\ (DEFAULT)}$	−0.8		+0.8	%	
		−1.3		+1.3	%	−25°C ≤ T_J ≤ +85°C
Load Regulation	$\Delta V_{FB2}/I_{LOAD2}$		0.25		%/A	I_{LOAD2} = 10 mA to 1.0 A, AUTO-PSM2 = 0
Line Regulation	$\Delta V_{FB2}/V_{PVIN2}$		0.004		%/V	V_{PVIN2} = 5 V to 15 V, I_{LOAD2} = 500 mA
SW2 Pins						
High-Side Power FET On Resistance	R_{DSON_2H}		235		mΩ	I_D = 100 mA
Low-Side Power FET On Resistance	R_{DSON_2L}		165		mΩ	I_D = 100 mA
Switch Current Limit	I_{CL2}	1.2	1.8		A	Valley current, −25°C ≤ T_J ≤ +85°C
Minimum Off Time	$t_{OFF2\ (MIN)}$		100		ns	
Minimum Duty Cycle	D_{MIN2}		0		%	
Soft Start Time	t_{SS2}		4		ms	SS2 = 10
C_{OUT} Discharge Switch On Resistance	R_{DIS2}		125		Ω	V_{FB2} = 1 V
CHANNEL 3 SYNC BUCK REGULATOR						
Channel 3 Output Voltage (FB3 Pin)						
Fixed Voltage Range, 3 Bits	V_{FB3}	1.2		1.8	V	
Minimum Adjustable Voltage			0.8		V	VID3 = 111
Feedback Voltage Accuracy at Default VID Code	$V_{FB3\ (DEFAULT)}$	−0.8		+0.8	%	
		−1.3		+1.3	%	−25°C ≤ T_J ≤ +85°C
Load Regulation	$\Delta V_{FB3}/I_{LOAD3}$		0.17		%/A	I_{LOAD3} = 15 mA to 1.5 A, AUTO-PSM3 = 0
Line Regulation	$\Delta V_{FB3}/V_{PVIN3}$		0.003		%/V	V_{PVIN3} = 5 V to 15 V, I_{LOAD3} = 700 mA

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SW3 Pins						
High-Side Power FET On Resistance	R_{DSON_3H}		155		mΩ	I_D = 100 mA
Low-Side Power FET On Resistance	R_{DSON_3L}		100		mΩ	I_D = 100 mA
Switch Current Limit	I_{CL3}	2.05	2.8		A	Valley current, −25°C ≤ T_J ≤ +85°C
Minimum Off Time	$t_{OFF3\ (MIN)}$		90		ns	
Minimum Duty Cycle	D_{MIN3}		0		%	
Soft Start Time	t_{SS3}		4		ms	SS3 = 10
C_{OUT} Discharge Switch On Resistance	R_{DIS3}		125		Ω	V_{FB3} = 1 V
CHANNEL 4 SYNC BUCK REGULATOR						
Channel 4 Output Voltage (FB4 Pin)						
Fixed Voltage Range, 3 Bits	V_{FB4}	1.8		3.55	V	
Minimum Adjustable Voltage			0.8		V	VID4 = 111
Feedback Voltage Accuracy at Default VID Code	$V_{FB4\ (DEFAULT)}$	−1		+1	%	
		−2		+2	%	−25°C ≤ T_J ≤ +85°C
Load Regulation	$\Delta V_{FB4}/I_{LOAD4}$		0.10		%/A	I_{LOAD4} = 10 mA to 800 mA, AUTO-PSM4 = 0
Line Regulation	$\Delta V_{FB4}/V_{PVIN4}$		0.003		%/V	V_{PVIN4} = 5 V to 15 V, I_{LOAD4} = 400 mA
SW4 Pin						
High-Side Power FET On Resistance	R_{DSON_4H}		350		mΩ	I_D = 100 mA
Low-Side Power FET On Resistance	R_{DSON_4L}		345		mΩ	I_D = 100 mA
Switch Current Limit	I_{CL4}	0.96	1.4		A	Peak current, −25°C ≤ T_J ≤ +85°C
Minimum On Time	$t_{ON4\ (MIN)}$		75		ns	
Maximum Duty Cycle	D_{MAX4}		100		%	
Soft Start Time	t_{SS4}		4		ms	SS4 = 10
C_{OUT} Discharge Switch On Resistance	R_{DIS4}		125		Ω	V_{FB4} = 1 V
CHANNEL 5 SYNC BUCK REGULATOR						
Channel 5 Output Voltage (FB5 Pin)						
Fixed Voltage Range, 3 Bits	V_{FB5}	3.0		5.0	V	
Feedback Voltage Accuracy at Default VID Code	$V_{FB5\ (DEFAULT)}$	−1		+1	%	
		−2		+2	%	−25°C ≤ T_J ≤ +85°C
Load Regulation	$\Delta V_{FB5}/I_{LOAD5}$		0.05		%/A	I_{LOAD5} = 20 mA to 2 A, AUTO-PSM5 = 0
Line Regulation	$\Delta V_{FB5}/V_{PVIN5}$		0.001		%/V	V_{PVIN5} = 5 V to 15 V, I_{LOAD5} = 1 A
SW5 Pins						
High-Side Power FET On Resistance	R_{DSON_5H}		200		mΩ	I_D = 100 mA
Low-Side Power FET On Resistance	R_{DSON_5L}		120		mΩ	I_D = 100 mA
Switch Current Limit	I_{CL5}	2.4	3		A	Peak current, −25°C ≤ T_J ≤ +85°C
Minimum On Time	$t_{ON5\ (MIN)}$		75		ns	
Maximum Duty Cycle	D_{MAX5}		100		%	
Soft Start Time	t_{SS5}		4		ms	SS5 = 10
C_{OUT} Discharge Switch On Resistance	R_{DIS5}		125		Ω	V_{FB5} = 1 V
CHANNEL 6 BUCK BOOST REGULATOR						
Channel 6 Output Voltage (FB6 Pin)						
Fixed Voltage Range, 4 Bits	V_{FB6}	3.5		5.5	V	
Minimum Adjustable Voltage			0.8		V	VID6 = 1111
Accuracy at Default VID Code	$V_{VOUT6\ (DEFAULT)}$	−1		+1	%	
		−2		+2	%	−25°C ≤ T_J ≤ +85°C
Load Regulation	$\Delta V_{VOUT6}/I_{LOAD6}$		0.05		%/A	Buck boost configuration, I_{LOAD6} = 15 mA to 1.5 A, AUTO-PSM6 = 0
Line Regulation	$\Delta V_{VOUT6}/V_{PVIN6}$		0.001		%/V	V_{PVIN6} = 5 V to 15 V, I_{LOAD6} = 700 mA

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SW6A Pins						
Low-Side Power FET On Resistance	R_{DSON_6AL}		95		mΩ	I_D = 100 mA, V_{VDR6} = 5 V
High-Side Power FET On Resistance	R_{DSON_6AH}		60		mΩ	I_D = 100 mA, V_{VDR6} = 5 V
High-Side Switch Current Limit	I_{CL6A}	3.2	4.4		A	Peak current, −25°C ≤ T_J ≤ +85°C
Minimum On Time	$t_{ON6\ (MIN)}$		80		ns	SW6A high-side on time
SW6B Pins						
Low-Side Power FET On Resistance	R_{DSON_6BL}		50		mΩ	I_D = 100 mA
High-Side Power FET On Resistance	R_{DSON_6BH}		55		mΩ	I_D = 100 mA
Boost Minimum Duty Cycle	D_{MIN6B}		0		%	SW6B low-side duty cycle
Soft Start Time	t_{SS6}		4		ms	SS6 = 10
C_{OUT} Discharge Switch On Resistance	R_{DIS6}		110		Ω	V_{VOUT6} = 1 V

LINEAR REGULATOR BLOCK SPECIFICATIONS

T_J = 25°C, V_{VBATT} = 7.2 V, V_{VREG1} = V_{VDRx} = 5 V, V_{VREG2} = V_{VDDIO} = 3.3 V, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CHANNEL 7 LDO REGULATOR						
Channel 7 Output Voltage	V_{VOLDO7}	5		12	V	V_{VILDO7} = V_{VOLDO7} + 0.5 V
Voltage Accuracy	$V_{VOLDO7\ (DEFAULT)}$	−1.5		+1.5	%	V_{VILDO7} = V_{VOLDO7} + 0.5 V, I_{LOAD7} = 1 mA
		−2.5		+2.5	%	V_{VILDO7} = V_{VOLDO7} + 0.5 V, I_{LOAD7} = 1 mA, −25°C ≤ T_J ≤ +85°C
Load Regulation	$\Delta V_{VOLDO7}/I_{LOAD7}$		0.005		%/mA	V_{VILDO7} = V_{VOLDO7} + 0.5 V, I_{LOAD7} = 1 mA to 20 mA
Line Regulation	$\Delta V_{VOLDO7}/V_{VILDO7}$		0.007		%/V	V_{VILDO7} = (V_{VOLDO7} + 0.5 V) to 25 V, I_{LOAD7} = 1 mA
Dropout Voltage[1]	V_{DROP}		75		mV	V_{VOLDO7} programmed to 12 V, I_{VOLDO7} = 10 mA
Current Limit	I_{CL7}	30	50		mA	V_{VOLDO7} = 95% of nominal
Soft Start Time	t_{SS7}		4		ms	SS7 = 1
C_{OUT} Discharge Switch On Resistance	R_{DIS7}		1		kΩ	V_{VOLDO7} = 1 V

[1] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage.

I²C INTERFACE TIMING SPECIFICATIONS

T_J = 25°C, V_{VBATT} = 7.2 V, V_{VDRx} = 5 V, V_{VREG2} = V_{VDDIO} = 3.3 V, unless otherwise noted.

Table 5.

Parameter	Min	Typ	Max	Unit	Description
f_{SCL}			400	kHz	SCL clock frequency
t_{HIGH}	0.6			µs	SCL high time
t_{LOW}	1.3			µs	SCL low time
$t_{SU,DAT}$	100			ns	Data setup time
$t_{HD,DAT}$	0		0.9	µs	Data hold time[1]
$t_{SU,STA}$	0.6			µs	Setup time for repeated start
$t_{HD,STA}$	0.6			µs	Hold time for start or repeated start
t_{BUF}	1.3			µs	Bus free time between a stop condition and a start condition
$t_{SU,STO}$	0.6			µs	Setup time for a stop condition
t_R	20 + 0.1 × C_B[2]		300	ns	Rise time of SCL and SDA
t_F	20 + 0.1 × C_B[2]		300	ns	Fall time of SCL and SDA
t_{SP}	0		50	ns	Pulse width of suppressed spike
C_B[2]			400	pF	Capacitive load for each bus line

[1] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} minimum of the SCL signal) to bridge the undefined region of the SCL falling edge.
[2] C_B is the total capacitance of one bus line in picofarads (pF).

Timing Diagram

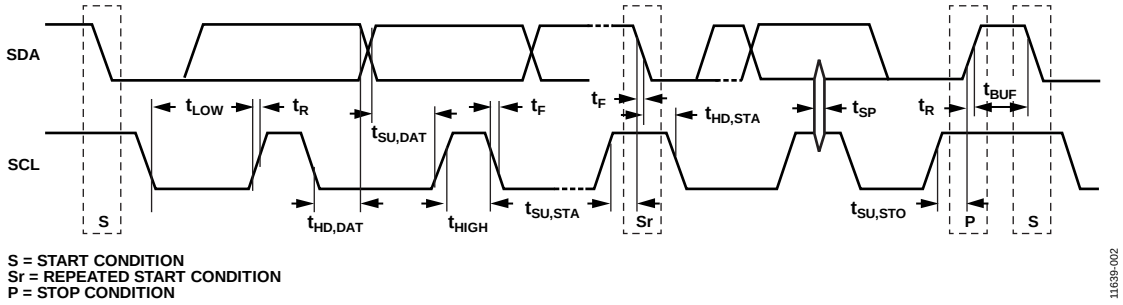

Figure 2. I²C Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
VBATT to GND	−0.3 V to +18 V
VDDIO to GND	−0.3 V to +4.0 V
VISW1 to GND	−0.3 V to +6.5 V
VISW2 to GND	−0.3 V to +4.0 V
VREG1 to GND	−0.3 V to +6.5 V
VREG2 to GND	−0.3 V to +4.0 V
EN to GND	−0.3 V to +18 V
EN34 to GND	−0.3 V to +6.5 V
$\overline{\text{FAULT}}$ to GND	−0.3 V to +4.0 V
BSTCP to PVINCP	−0.3 V to +6.5 V
BSTCP to GND	−0.3 V to +23 V
C+ to PVINCP	−0.3 V to (V_{VDR5} + 0.3 V)
C− to PGND5	−0.3 V to (V_{VDR5} + 0.3 V)
PVINx to PGNDx	−0.3 V to +18 V
VDRx to PGNDx	−0.3 V to +6.5 V
BST16, BST23, BST45 to PVINx	−0.3 V to +6.5 V
FB1, FB2, FB3 to GND	−0.3 V to +4.0 V
FB4, FB5, FB6 to GND	−0.3 V to +6.5 V
VOUT6 to PGND6	−0.3 V to +6.5 V
SW1A, SW1B to PGND1	−2.0 V to +18 V
SW2 to PGND2	−2.0 V to +18 V
SW3 to PGND3	−2.0 V to +18 V
SW4 to PGND4	−2.0 V to +18 V
SW5 to PGND5	−2.0 V to +18 V
SW6A to PGND6	−2.0 V to +18 V
SW6B to PGND6	−0.5 V to (V_{VOUT6} + 2.0 V) or +6.5 V, whichever is lower
PGNDx to GND	−0.3 V to +0.3 V
VILDO7 to GND	−0.3 V to +28 V
VOLDO7 to GND	−0.3 V to +18 V
FREQ to GND	−0.3 V to (V_{VREG2} + 0.3 V)
SYNC to GND	−0.3 V to +4.0 V
CLKO to GND	−0.3 V to (V_{VREG2} + 0.3 V)
SCL to GND	−0.3 V to +4.0 V
SDA to GND	−0.3 V to +4.0 V
Storage Temperature Range	−65°C to +150°C
Operating Ambient Temperature Range	−25°C to +85°C
Operating Junction Temperature Range	−25°C to +125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for worst-case conditions; that is, a device soldered in a circuit board for surface-mount packages. Note that actual θ_{JA} depends on the application environment.

Table 7. Thermal Resistance

PCB Type[1]	θ_{JA}[2]	θ_{JB}[2]	Unit
1S0P	60.6	7.3	°C/W
2S2P	26.9	4.5	°C/W

[1] PCB type conforms to JEDEC JESD51-9 standard.
[2] 1.25 W power dissipation with zero airflow.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

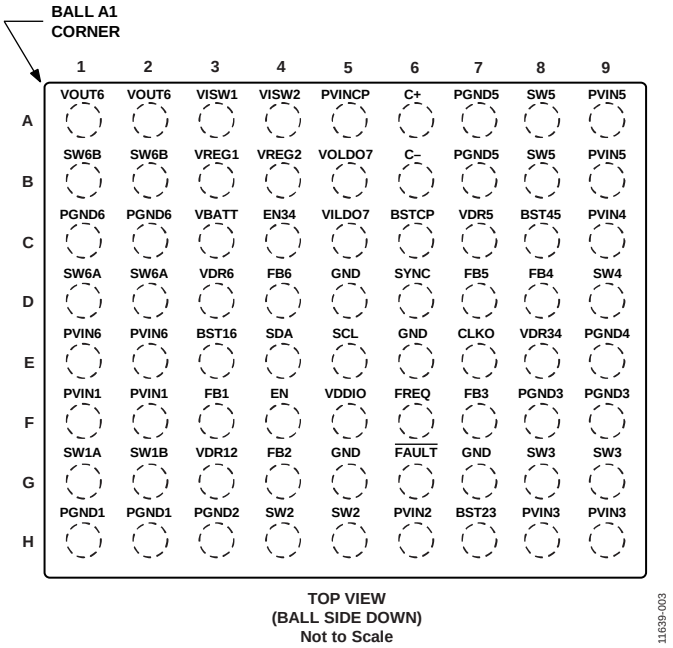

Figure 3. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1A	VOUT6	Output Voltage for Channel 6.
2A	VOUT6	Output Voltage for Channel 6.
3A	VISW1	Input for an External Regulator Output. A 5.0 V to 5.5 V regulator connected to the VISW1 pin can take over from LDO1 to supply the internal circuit of the ADP5080 and the VREG1 load. If this pin is not used, connect it to GND.
4A	VISW2	Input for an External Regulator Output. A 3.0 V to 3.3 V regulator connected to the VISW2 pin can take over from LDO2 to supply the internal circuit of the ADP5080 and the VREG2 load. If this pin is not used, connect it to GND.
5A	PVINCP	Input Power Supply for the Charge Pump.
6A	C+	Flying Capacitor Terminal for the Charge Pump.
7A	PGND5	Power Ground for Channel 5.
8A	SW5	Switching Node for Channel 5.
9A	PVIN5	Input Power Supply for Channel 5.
1B	SW6B	Secondary Side Boost Switching Node for Channel 6.
2B	SW6B	Secondary Side Boost Switching Node for Channel 6.
3B	VREG1	Output Voltage for LDO1.
4B	VREG2	Output Voltage for LDO2.
5B	VOLDO7	Output Voltage for Channel 7. Leave this pin open if not used.
6B	C–	Flying Capacitor Terminal for the Charge Pump.
7B	PGND5	Power Ground for Channel 5.
8B	SW5	Switching Node for Channel 5.
9B	PVIN5	Input Power Supply for Channel 5.
1C	PGND6	Power Ground for Channel 6.
2C	PGND6	Power Ground for Channel 6.
3C	VBATT	Power Supply Input for the Internal Circuits. Connect this pin to the battery.
4C	EN34	Independent Enable Input for Channel 3 and Channel 4. If this pin is not used, connect it to GND.
5C	VILDO7	Input Power Supply for Channel 7. If this pin is not used, connect it to VBATT.
6C	BSTCP	Output Voltage for Charge Pump.
7C	VDR5	Low-Side FET Driver Power Supply for Channel 5. Connect this pin to VREG1.
8C	BST45	High-Side FET Driver Power Supply for Channel 4 and Channel 5.

Pin No.	Mnemonic	Description
9C	PVIN4	Input Power Supply for Channel 4.
1D	SW6A	Primary Side Switching Node for Channel 6.
2D	SW6A	Primary Side Switching Node for Channel 6.
3D	VDR6	Low-Side FET Driver Power Supply for Channel 6. Connect this pin to VREG1.
4D	FB6	Feedback Node for Channel 6.
5D	GND	Ground. All GND pins must be connected.
6D	SYNC	External Clock Input (CMOS Input Port). If this pin is not used, connect it to GND.
7D	FB5	Feedback Node for Channel 5.
8D	FB4	Feedback Node for Channel 4.
9D	SW4	Switching Node for Channel 4.
1E	PVIN6	Input Power Supply for Channel 6.
2E	PVIN6	Input Power Supply for Channel 6.
3E	BST16	High-Side FET Driver Power Supply for Channel 1 and Channel 6.
4E	SDA	Data Input/Output for I^2C Interface. Open-drain I/O port.
5E	SCL	Clock Input for I^2C Interface. For start-up requirements, see the I^2C Interface section.
6E	GND	Ground. All GND pins must be connected.
7E	CLKO	Clock Output (CMOS Output Port). CLKO replicates the Channel 1 switching clock. This output is not available when the SYNC pin is driven by an external clock. If this pin is not used, leave it open.
8E	VDR34	Low-Side FET Driver Power Supply for Channel 3 and Channel 4. Connect this pin to VREG1.
9E	PGND4	Power Ground for Channel 4.
1F	PVIN1	Input Power Supply for Channel 1.
2F	PVIN1	Input Power Supply for Channel 1.
3F	FB1	Feedback Node for Channel 1.
4F	EN	Enable Control Input.
5F	VDDIO	Supply Voltage for I^2C Interface. Typically, this pin is connected externally to VREG2 or to the host I/O voltage.
6F	FREQ	Frequency Pin for the Internal Oscillator. To select the internal clock source oscillator, connect an external 100 kΩ resistor from the FREQ pin to GND.
7F	FB3	Feedback Node for Channel 3.
8F	PGND3	Power Ground for Channel 3.
9F	PGND3	Power Ground for Channel 3.
1G	SW1A	Switching Node for Channel 1.
2G	SW1B	Switching Node for Channel 1.
3G	VDR12	Low-Side FET Driver Power Supply for Channel 1 and Channel 2. Connect this pin to VREG1.
4G	FB2	Feedback Node for Channel 2.
5G	GND	Ground. All GND pins must be connected.
6G	$\overline{\text{FAULT}}$	Fault Status Output Pin. This open-drain output port goes low when a fault occurs. Leave open if not used.
7G	GND	Ground. All GND pins must be connected.
8G	SW3	Switching Node for Channel 3.
9G	SW3	Switching Node for Channel 3.
1H	PGND1	Power Ground for Channel 1.
2H	PGND1	Power Ground for Channel 1.
3H	PGND2	Power Ground for Channel 2.
4H	SW2	Switching Node for Channel 2.
5H	SW2	Switching Node for Channel 2.
6H	PVIN2	Input Power Supply for Channel 2.
7H	BST23	High-Side FET Driver Power Supply for Channel 2 and Channel 3.
8H	PVIN3	Input Power Supply for Channel 3.
9H	PVIN3	Input Power Supply for Channel 3.

TYPICAL PERFORMANCE CHARACTERISTICS

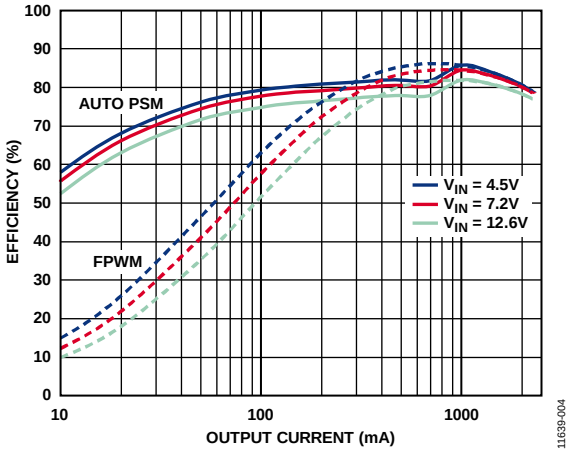

Figure 4. Channel 1 Efficiency, V_{OUT} = 1.1 V

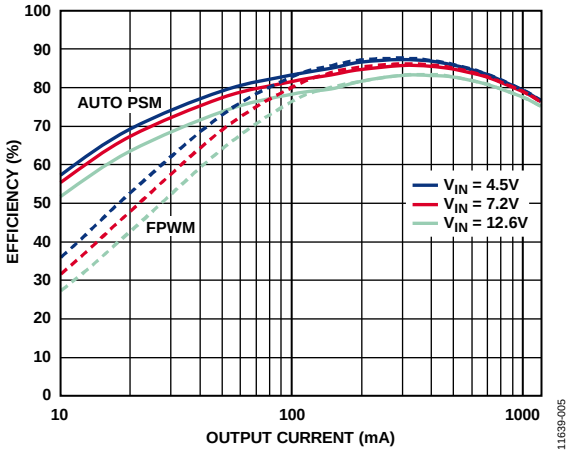

Figure 5. Channel 2 Efficiency, V_{OUT} = 1.2 V

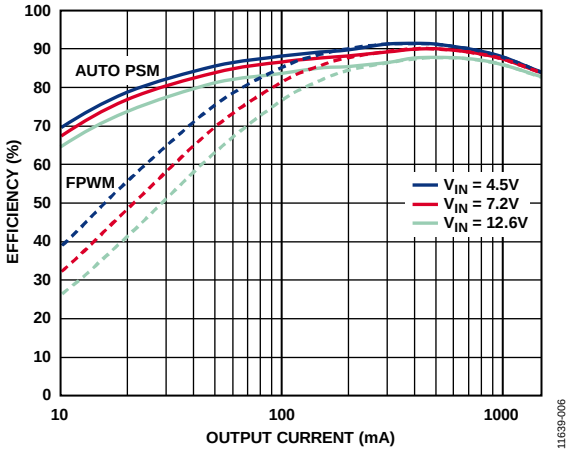

Figure 6. Channel 3 Efficiency, V_{OUT} = 1.8 V

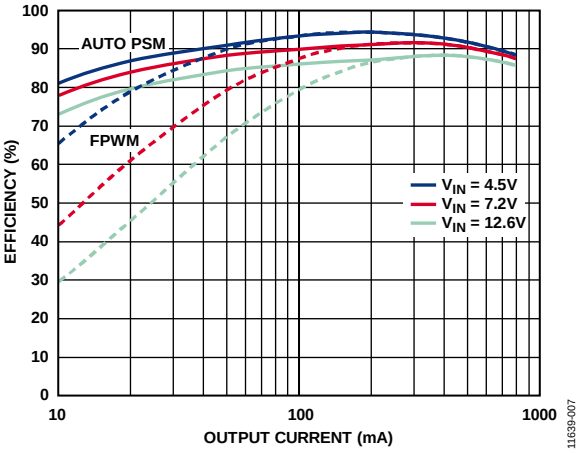

Figure 7. Channel 4 Efficiency, V_{OUT} = 3.3 V

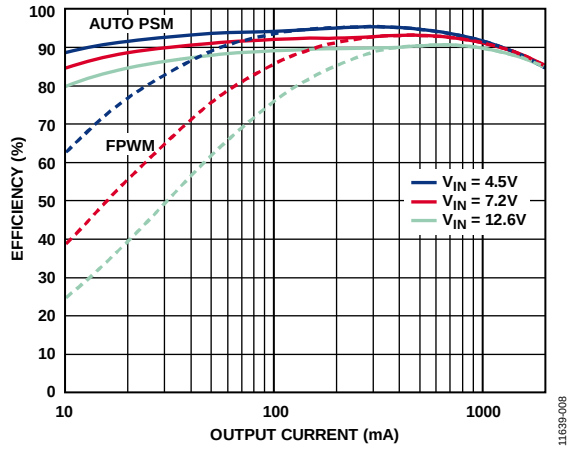

Figure 8. Channel 5 Efficiency, V_{OUT} = 3.3 V

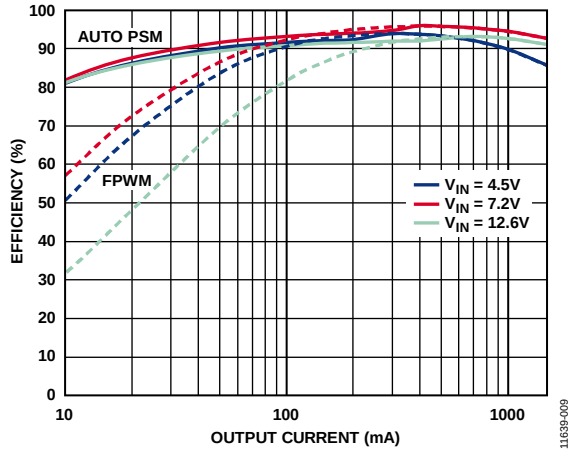

Figure 9. Channel 6 Efficiency, V_{OUT} = 5 V

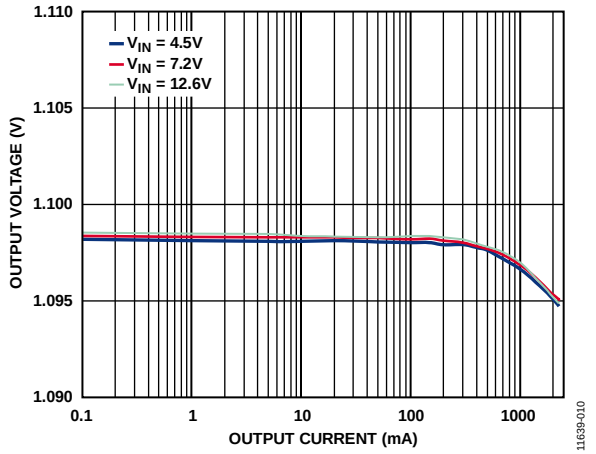

Figure 10. Channel 1 Load Regulation

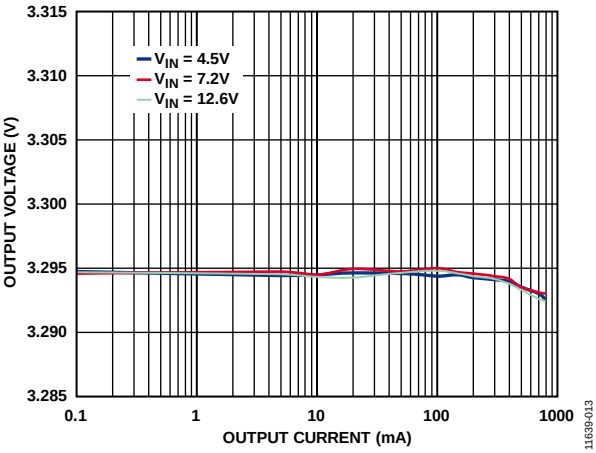

Figure 13. Channel 4 Load Regulation

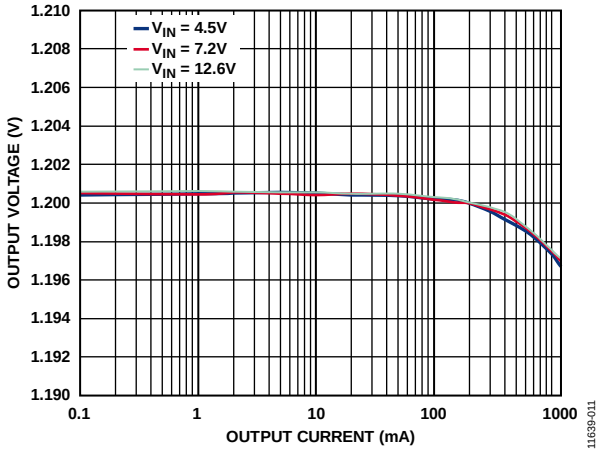

Figure 11. Channel 2 Load Regulation

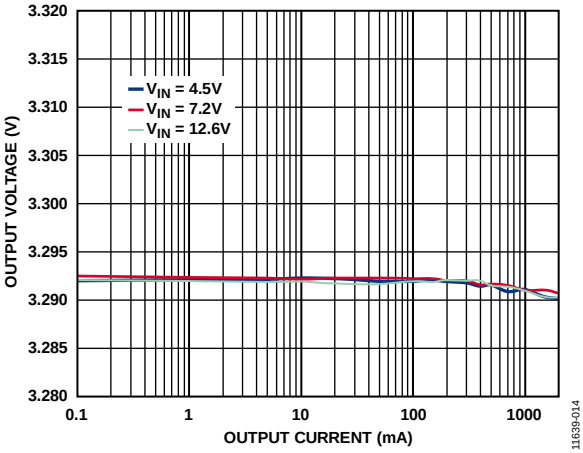

Figure 14. Channel 5 Load Regulation

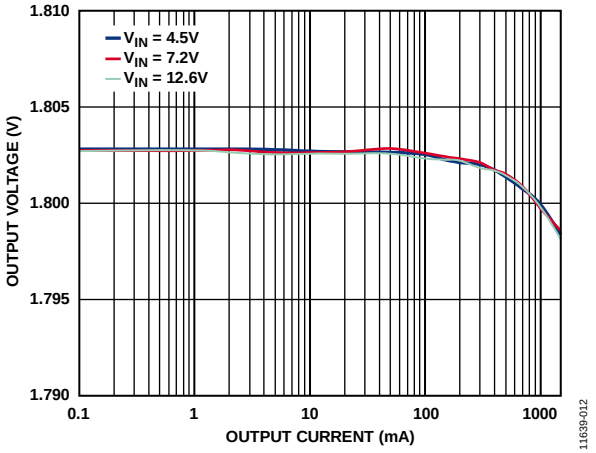

Figure 12. Channel 3 Load Regulation

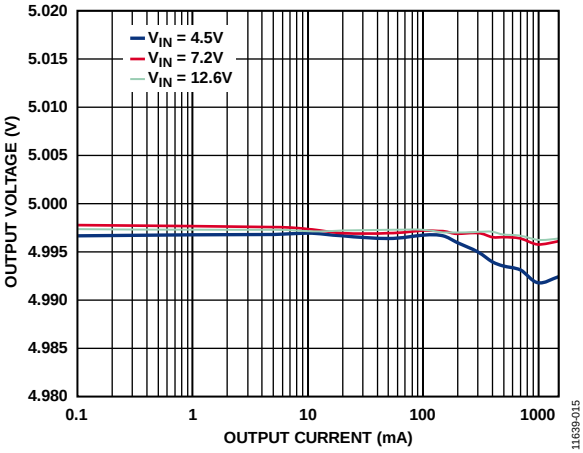

Figure 15. Channel 6 Load Regulation

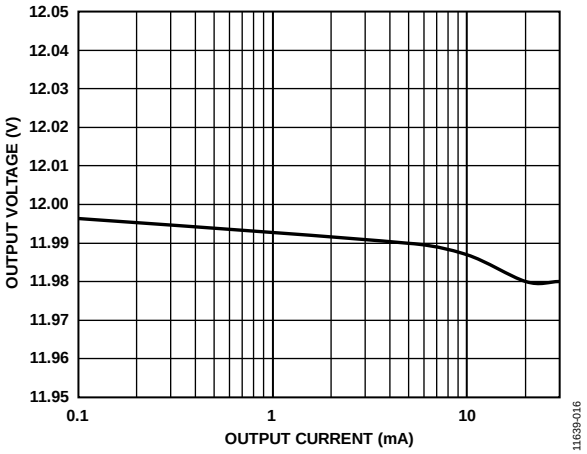

Figure 16. Channel 7 Load Regulation, VILDO7 = 16 V

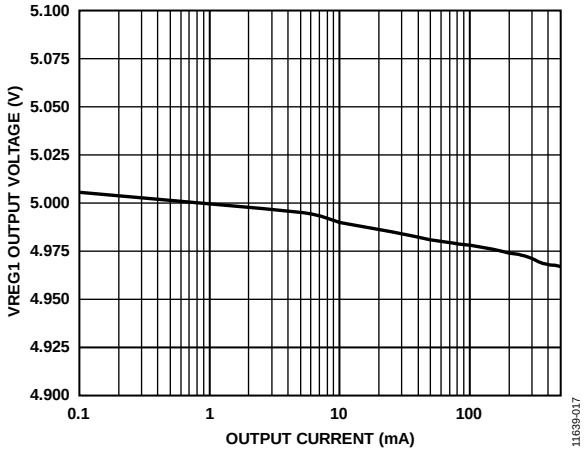

Figure 17. VREG1 Load Regulation

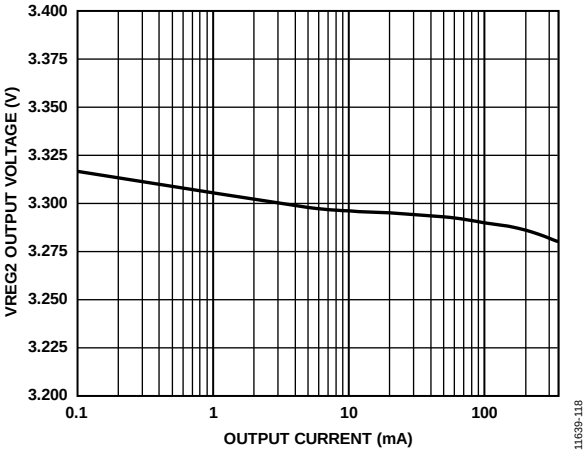

Figure 18. VREG2 Load Regulation

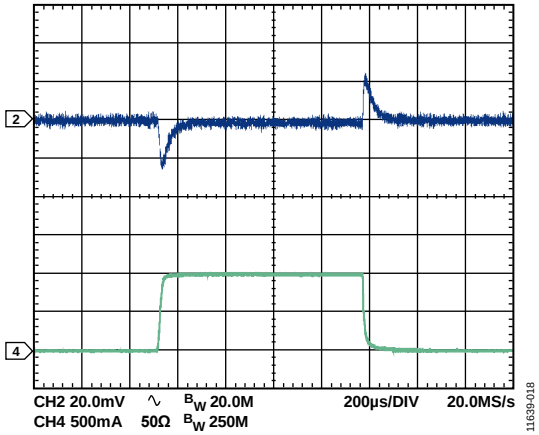

Figure 19. Channel 1 Load Transient, V_{OUT} = 1.1 V, FPWM Mode

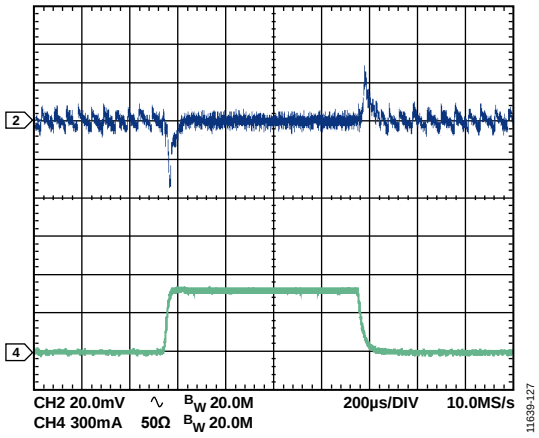

Figure 20. Channel 1 Load Transient, V_{OUT} = 1.1 V, Auto PSM Mode

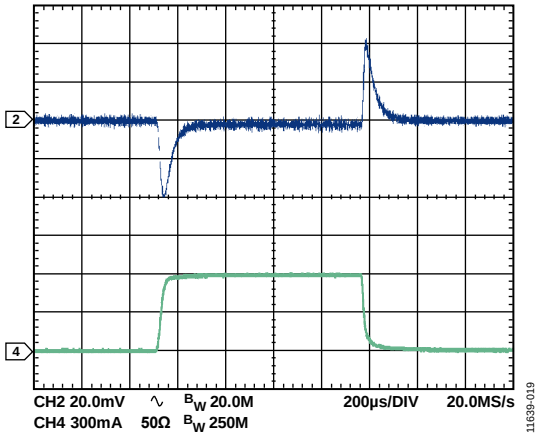

Figure 21. Channel 2 Load Transient, V_{OUT} = 1.2 V, FPWM Mode

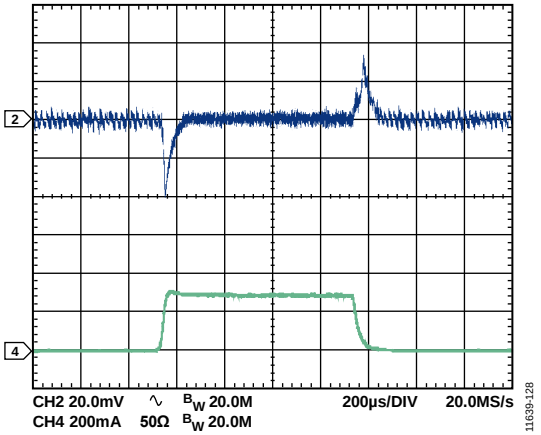

Figure 22. Channel 2 Load Transient, V_{OUT} = 1.2 V, Auto PSM Mode

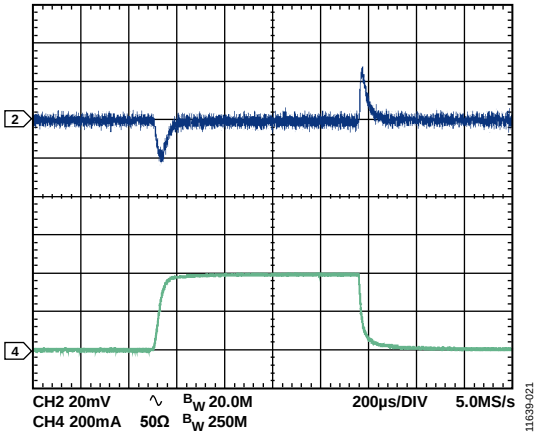

Figure 25. Channel 4 Load Transient, V_{OUT} = 3.3 V, FPWM Mode

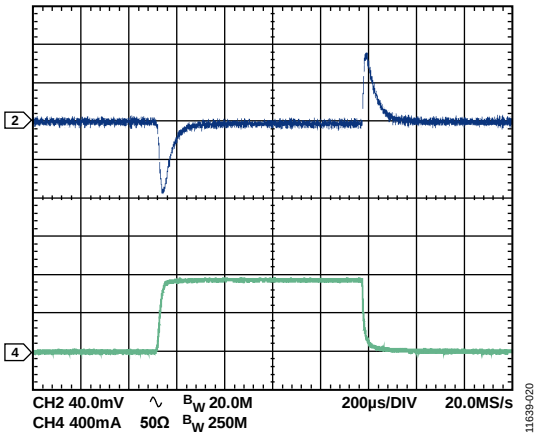

Figure 23. Channel 3 Load Transient, V_{OUT} = 1.8 V, FPWM Mode

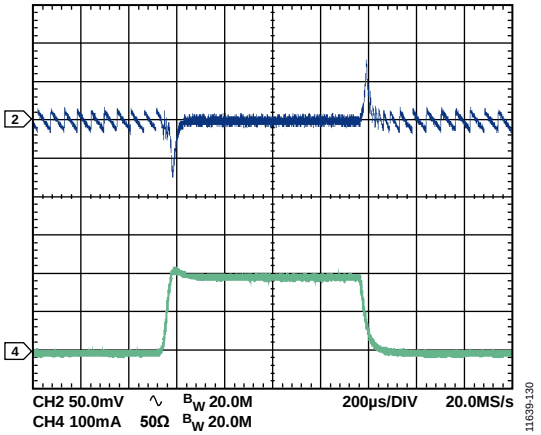

Figure 26. Channel 4 Load Transient, V_{OUT} = 3.3 V, Auto PSM Mode

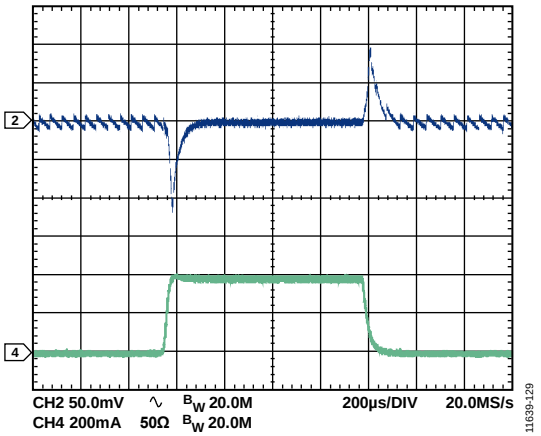

Figure 24. Channel 3 Load Transient, V_{OUT} = 1.8 V, Auto PSM Mode

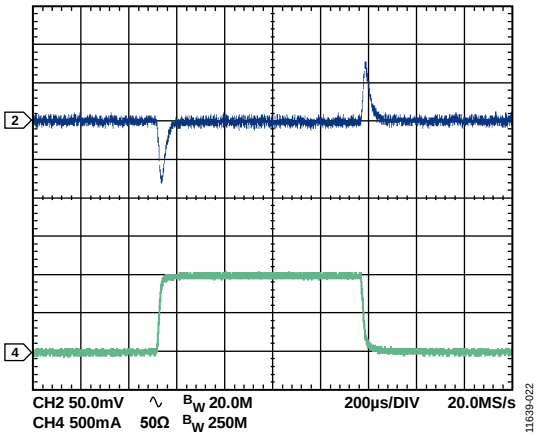

Figure 27. Channel 5 Load Transient, V_{OUT} = 3.3 V, FPWM Mode

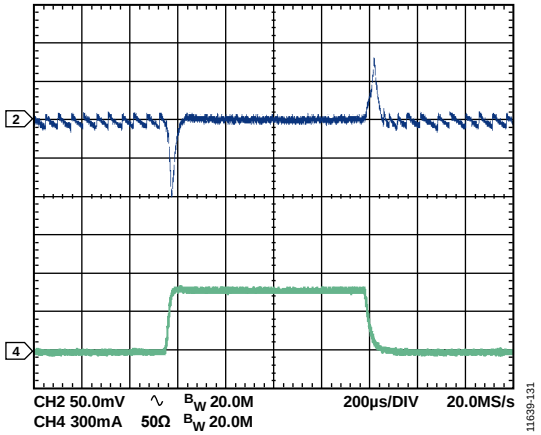

Figure 28. Channel 5 Load Transient, V_{OUT} = 3.3 V, Auto PSM Mode

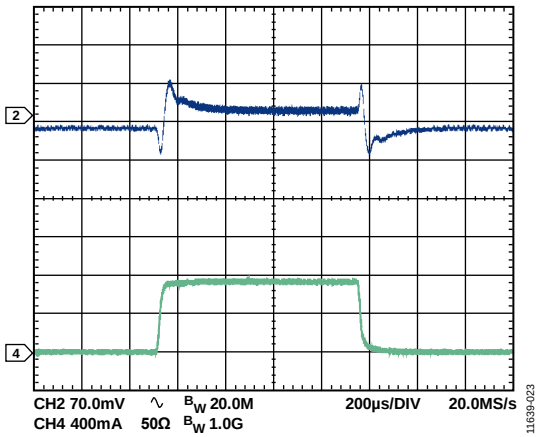

Figure 29. Channel 6 Load Transient, V_{OUT} = 5 V, FPWM Mode

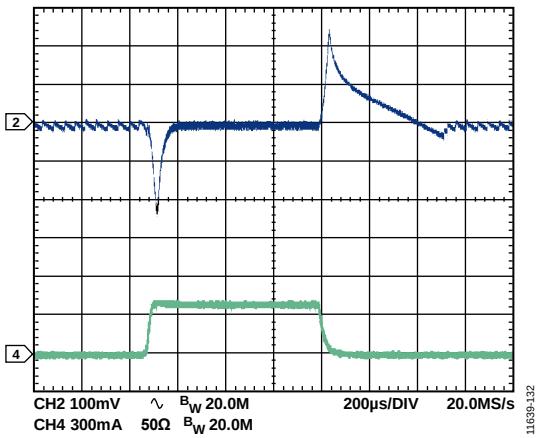

Figure 30. Channel 6 Load Transient, V_{OUT} = 5 V, Auto PSM Mode

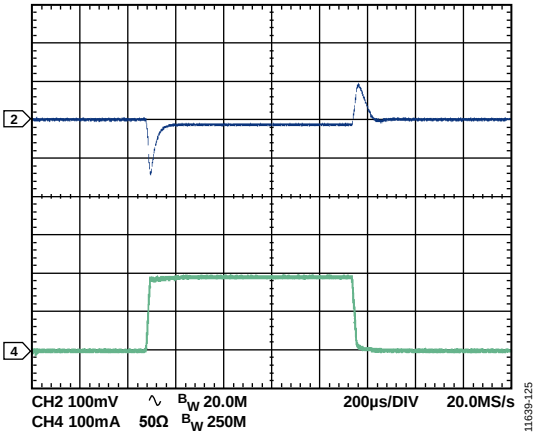

Figure 31. VREG1 Load Transient, VREG1 = 5 V

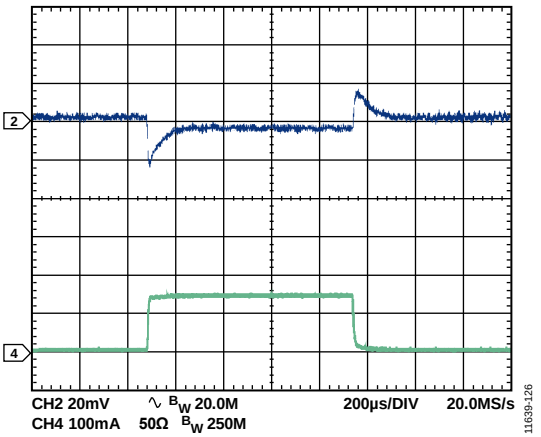

Figure 32. VREG2 Load Transient, VREG2 = 3.3 V

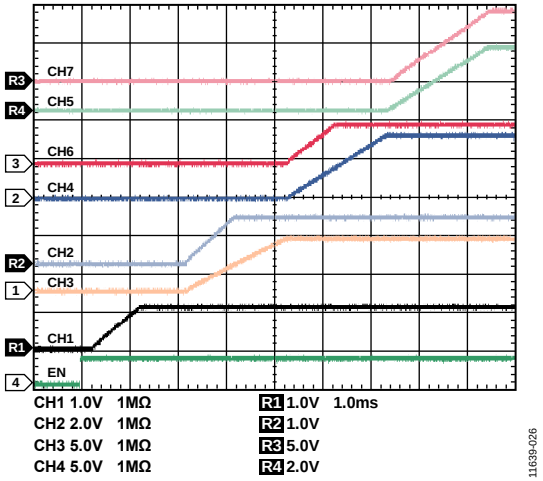

Figure 33. Startup

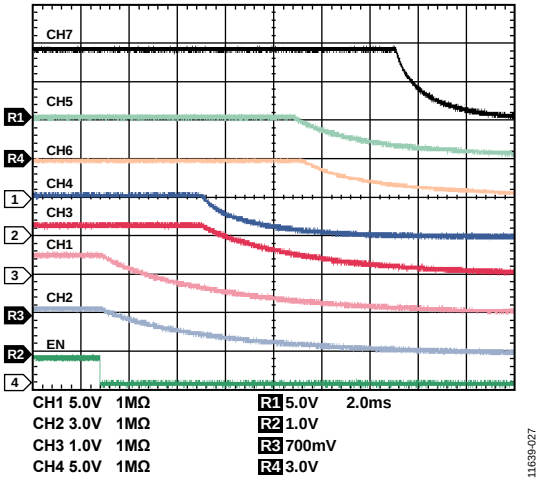

Figure 34. Shutdown

APPLICATION CIRCUIT

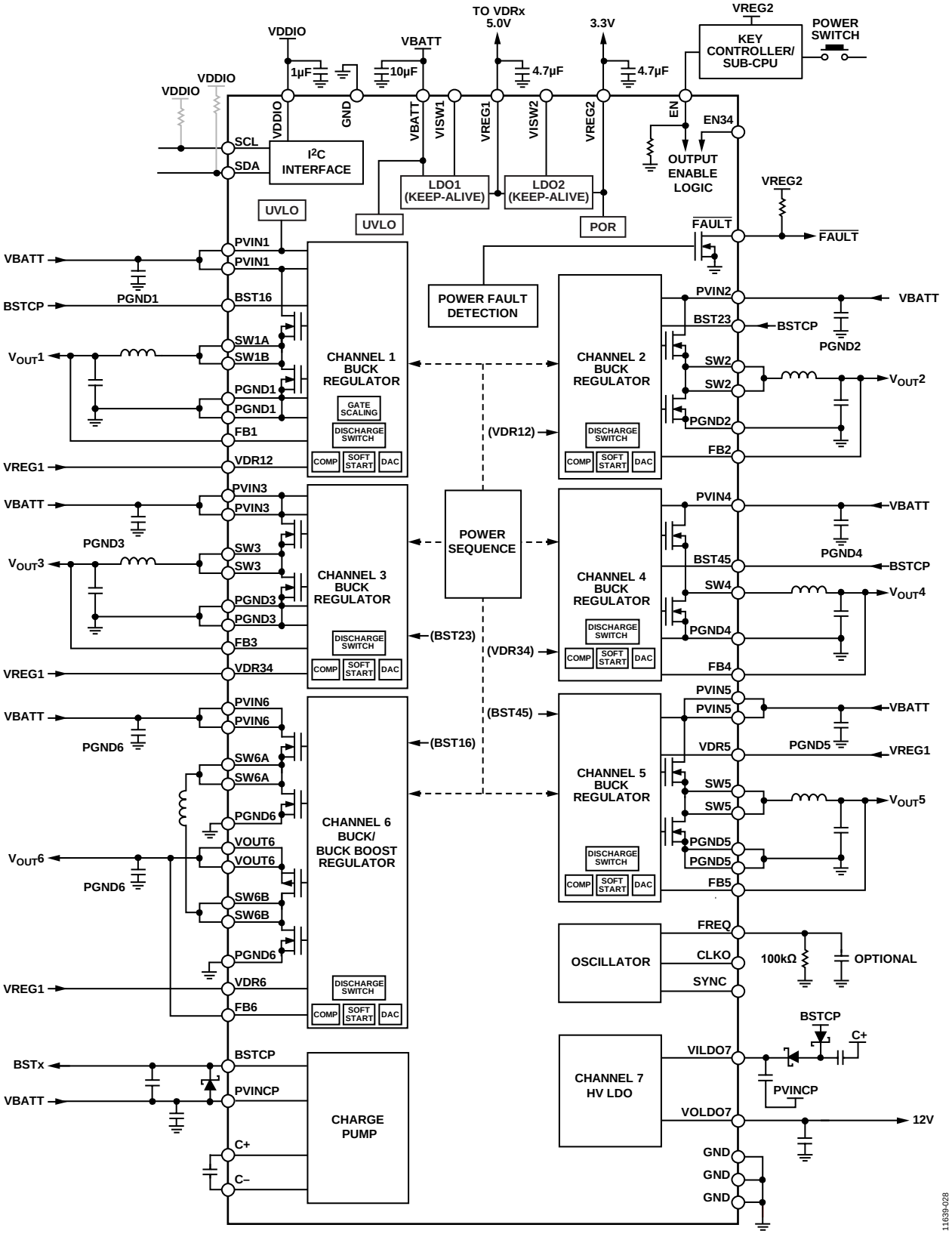

Figure 35. Typical Application Circuit

THEORY OF OPERATION

The ADP5080 is a fully integrated, high efficiency power solution for multicell lithium ion battery applications. The device can connect directly to the battery, which eliminates the need for preregulators and increases the battery life of the system.

The ADP5080 integrates two keep-alive LDO regulators, five synchronous buck regulators, one configurable buck boost regulator, and one high voltage LDO regulator. An integrated charge pump provides the switch driver power supply. Along with the integrated power FETs and drivers, integrated compensation, soft start, and FB dividers contribute to minimize the number of external components and the PCB layout space, providing significant advantages for portable applications.

Factory programming sets the default values for the output voltages, fault behavior, switching frequency, start-up time, and other functions. These values can also be programmed via the I^2C interface. The ADP5080 features a built-in sequencer that provides automatic startup and shutdown timing based on these settings.

UVLO AND POR

The undervoltage lockout (UVLO) and power-on reset (POR) functions prevent abnormal behavior and force a smooth shutdown when input voltages fall below the minimum required levels. The ADP5080 incorporates UVLO on VBATT, PVIN1, and VDR12; it incorporates POR on VREG2. The thresholds are low enough to ensure normal operation down to 4 V at VBATT with ample hysteresis to avoid chattering.

Undervoltage Lockout (UVLO)

If the PVIN1 voltage of Channel 1 falls below the UVLO threshold ($V_{UVLO\ (F)}$), all channels, as well as the charge pump, are turned off. However, LDO1 and LDO2 remain operational.

As the input voltage rises, the regulator channels do not restart automatically. EN must be toggled after a UVLO event to restart channels in sequencer mode or manual mode. For more information about enabling channels using sequencer mode and manual mode, see the Enabling and Disabling the Output Channels section.

The VDRx pins provide the gate drive voltage to the internal power FETs. If the VDR12 voltage falls below 2.9 V (typical), all channels except LDO1 and LDO2 shut down to prevent malfunction of the power FETs. As with a PVIN UVLO event, EN must be toggled to restart channel operation.

Power-On Reset (POR)

If the VBATT voltage falls below its UVLO threshold ($V_{UVLO\ (BATT)}$), all channels, including LDO1 and LDO2, are shut down. This event forces a power-on reset.

VREG2 is the voltage supply for the internal digital circuit blocks. If the VREG2 voltage falls below the power-on reset threshold ($V_{UVLO\ (POR)}$) of 2.4 V typical, the ADP5080 shuts down, and all registers are reset to their default values.

DISCHARGE SWITCH

The ADP5080 integrates discharge switches for Channel 1 to Channel 7. These switches help to discharge the output capacitors quickly when a channel is turned off. The discharge switches are turned on when the EN signal goes low or when a channel is manually turned off via I^2C control, provided that the discharge function was enabled by setting the DSCGx_ON bit (x is 1 to 7) in Register 1. The default values for the discharge switches are factory fuse programmed.

KEEP-ALIVE LDO REGULATORS

The keep-alive LDO linear regulators (LDO1 and LDO2) are kept alive as long as a valid supply voltage is applied to the VBATT pin. The LDO regulators are used to power the internal control block of the ADP5080 so that the device is ready for the enable (EN) signal. The outputs of LDO1 and LDO2 are also available via the VREG1 and VREG2 pins for external circuits that are also kept alive during system standby.

When VBATT initially rises above the UVLO threshold, LDO1 begins operation, followed by LDO2. When all UVLO thresholds are cleared, the ADP5080 is in standby mode and ready to be enabled. If an external voltage is used to drive VDDIO, VDDIO can be on before VBATT; otherwise, LDO2 provides power to VDDIO via the VREG2 output.

LDO1

LDO1 regulates the supply voltage applied to the VBATT pin to either 5.0 V or 5.5 V and is capable of providing up to 400 mA. LDO1 internally supplies LDO2, as well as external circuits, including the VDRx pins supplied through the VREG1 pin.

The LDO1 output is enabled when the VBATT pin voltage rises above the UVLO threshold and is disabled when the VBATT pin voltage falls below the UVLO threshold.

VISW1 Input

A 5.0 V to 5.5 V regulator connected to the VISW1 pin can take over from LDO1 to supply the internal circuit of the ADP5080 and the VREG1 load. To enable this feature, set the SEL_INP_LDO1 bit (Bit 0 in Register 33) high after the VISW1 pin voltage settles above 4.7 V.

If the VISW1 pin voltage falls below 4.5 V, LDO1 resumes control automatically. However, if the VISW1 source is disabled, it is recommended that the SEL_INP_LDO1 bit be reset to 0 before turning off the VISW1 pin source.

The use of an external regulator connected to the VISW1 pin is intended to achieve better system power efficiency by allowing a switching power supply to take over the LDO1 linear regulator when the system is powered up to operation. If the VISW1 input is not used, tie it to GND. The VISW1 input is not active until EN is high.

Current Limit for LDO1

LDO1 is rated to a maximum load current of 400 mA. Above this level, the current-limit feature limits the current to protect the device.

The VISW1 input has an independent current-limit circuit with a typical threshold of 500 mA. If this overcurrent threshold is exceeded, the VISW1 input is immediately disconnected and LDO1 takes over to supply the VREG1 current. After the VISW1 input is turned off due to a current-limit event, it can be reset only by toggling the EN pin.

Discharge Switch for LDO1

A discharge switch at the VREG1 pin turns on during low VBATT pin voltage (3.5 V ± 0.1 V hysteresis), removing the charge of the external capacitor via a 1 kΩ resistor.

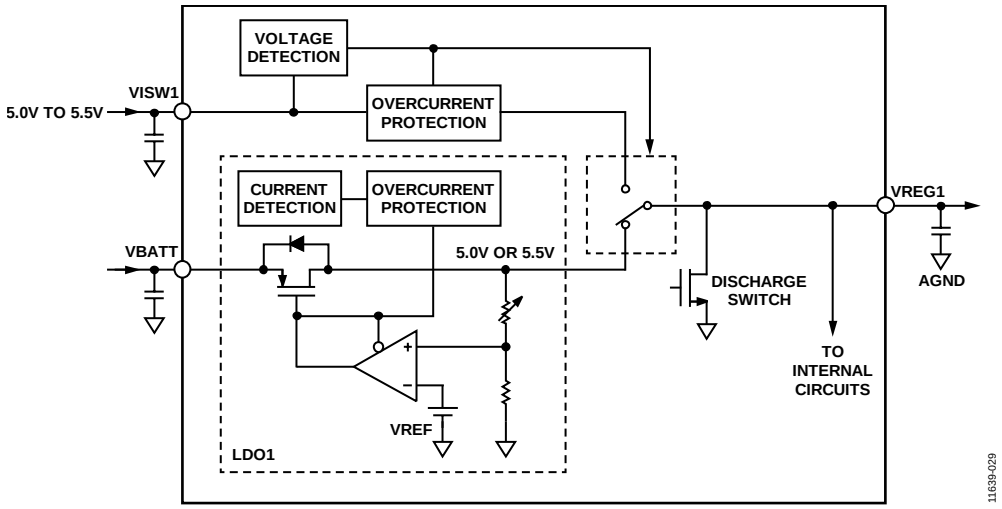

Figure 36. VREG1, LDO1, and VISW1

LDO2

LDO2 regulates the internally routed VREG2 pin voltage to 3 V, 3.15 V, 3.2 V, or 3.3 V and is capable of providing up to 300 mA. LDO2 internally supplies the control block of the ADP5080, as well as external circuits supplied through the VREG2 pin.

The LDO2 output is enabled when the VBATT pin voltage rises above the UVLO threshold and is disabled when the VBATT pin voltage falls below the UVLO threshold.

VISW2 Input

A 3.0 V to 3.3 V regulator connected to the VISW2 pin can take over from LDO2 to supply the internal circuit of the ADP5080 and the VREG2 load. To enable this feature, set the SEL_INP_LDO2 bit (Bit 4 in Register 33) high after the VISW2 pin voltage settles above 2.7 V.

If the VISW2 pin voltage falls below 2.55 V, LDO2 resumes control automatically. However, if the VISW2 source is disabled, it is recommended that the SEL_INP_LDO2 bit be reset to 0 before turning off the VISW2 pin source.

The use of an external regulator connected to the VISW2 pin is intended to achieve better system power efficiency by allowing a switching power supply to take over the LDO2 linear regulator when the system is powered up to operation. If the VISW2 input is not used, tie it to GND. The VISW2 input is not active until EN is high.

Because the VISW2 input supplies VREG2 with no regulation, the maximum voltage that can be applied to VISW2 is 3.3 V. The VISW2 input has a relatively high resistance compared to the LDO2 path. As a result, VISW2 regulation may not be sufficient when used to supply heavier loads.

Current Limit for LDO2

LDO2 is rated to a maximum load current of 300 mA. Above this level, the current-limit feature limits the current to protect the device.

The VISW2 input has an independent current-limit circuit with a typical threshold of 300 mA. If this overcurrent threshold is exceeded, the VISW2 input is immediately disconnected and LDO2 takes over to supply the VREG2 current. After the VISW2 input is turned off due to a current-limit event, it can be reset only by toggling the EN pin.

Discharge Switch for LDO2

A discharge switch at the VREG2 pin turns on during low VBATT pin voltage (3.5 V ± 0.1 V hysteresis), removing the residual charge of the external capacitor via a 12 Ω resistor.

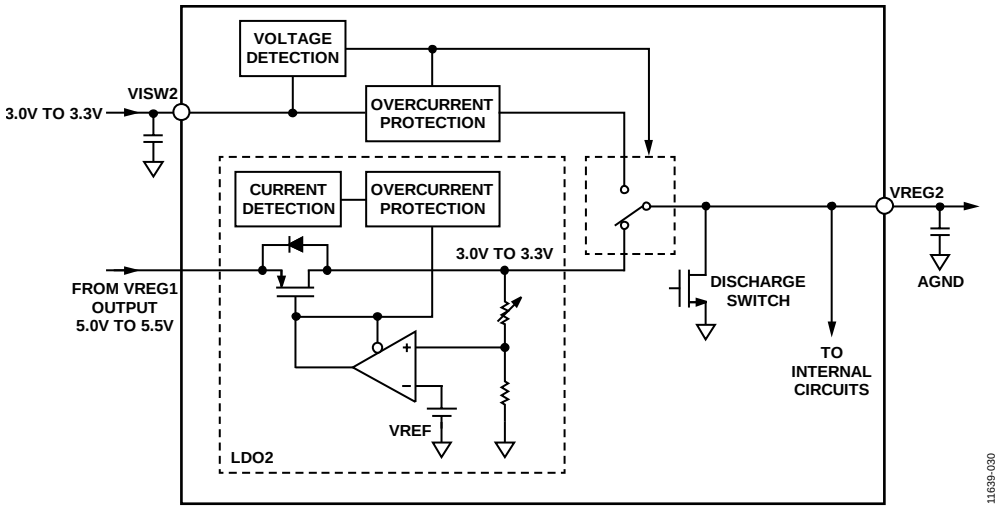

Figure 37. VREG2, LDO2, and VISW2

DC-TO-DC CONVERTER CHANNELS

The ADP5080 integrates five buck regulators and a configurable buck only/buck boost regulator. These regulators can be configured for various functions including auto PSM, auto DCM, DVS, and gate scaling. Each function is included only in the channels where it is most effective (see Table 9).

Channel 1, Channel 2, and Channel 3: Buck Regulators with Flex-Mode Architecture

Channel 1, Channel 2, and Channel 3 feature Flex-Mode™ current mode control, which eliminates minimum on time requirements and allows duty cycles as low as 0%. Flex-Mode uses a unique adaptive control architecture that maintains stable operation over a wide range of application conditions. With Flex-Mode control, very high step-down ratios can be achieved while maintaining high efficiency and excellent transient performance.

Selecting the Output Voltage, Channel 1 to Channel 3

The output voltage of Channel 1, Channel 2, or Channel 3 is selected from one of the preset values available in the VIDx bits, where x is 1, 2, or 3 (see Table 39 and Table 41). The default output voltage value is factory fuse programmed.

Channel 3 has an adjustable mode option that can be selected using the VID3 bits. When the adjustable output voltage mode is selected, the output voltage is set by an external feedback resistor divider. Select resistor values such that the desired output voltage is divided down to 0.8 V and the paralleled resistance seen from the dividing node does not exceed 25 kΩ (see the Setting the Output Voltage (Adjustable Mode Channels) section). Channel 1 can also be used in adjustable output mode by setting the VID1 bits to 0.8 V and using external feedback resistors with values less than 1 kΩ. When using the adjustable mode for Channel 1 or Channel 3, be aware of the minimum off time restriction, which may limit the range of available output voltages.

Channel 1, Channel 2, and Channel 3 are designed for very low duty cycle operation. However, at very high duty cycle, these channels have a limited range due to the minimum off time restriction (see Table 3). The minimum input voltage capability for a given output voltage can be determined using the following equation:

$$V_{IN\_MIN} = V_{OUT}/(1 - t_{OFF\_MIN} \times f_{SW})$$

If the input voltage falls below this level, the output voltage droops below its nominal value.

Current-Limit Protection, Channel 1 to Channel 3

Channel 1, Channel 2, and Channel 3 use valley mode current limit (see Figure 38). In valley mode current-limit protection, inductor current is sensed during the low-side on cycle, immediately before the high-side FET turns on. If the inductor current is above the current-limit threshold at this point, the next switching pulse is skipped.

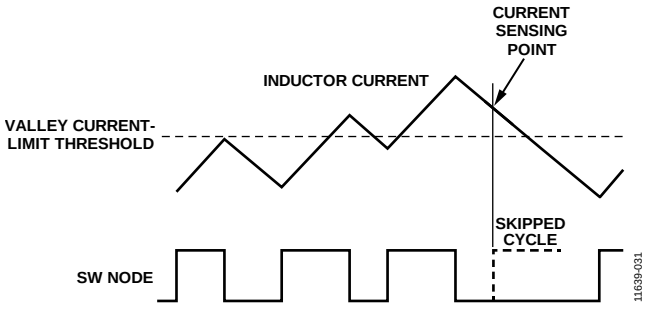

Figure 38. Valley Mode Current Limit

Switching does not resume until the current falls below the limit threshold. This behavior creates an inherent frequency foldback feature, which makes valley mode current-limit protection very robust against runaway inductor current. Because this type of current limit senses current before switching, it is also relatively immune to switching noise.

Table 3 provides the valley current threshold specifications. The actual load current-limit threshold varies with inductor value, frequency, and input and output voltage.

When the current-limit threshold is exceeded, load current is not allowed to increase further. Therefore, as the load impedance is reduced, the current limit forces the output voltage to fall. The falling output voltage in turn toggles the PWRGx, UVx, and $\overline{\text{FAULT}}$ error flags.

In the extreme event of an output voltage short circuit, the UVP function protects the device against excessive current during the on cycle (see the Undervoltage Protection (UVP) section).

Table 9. DC-to-DC Converter Specifications and Functions

Channel	Regulator Type	V_{IN} Range (V)	V_{OUT} Range (V)	Adjustable Mode (V)	I_{OUT} (A)	Auto PSM	Auto DCM	DVS	Gate Scaling
1	Buck	4 to 15	0.8 to 1.2[1]	0.8 to 1.2	3	Yes	N/A	Yes	Yes
2	Buck	4 to 15	1.0 to 3.3	N/A	1.15	Yes	N/A	Yes	N/A
3	Buck	4 to 15	1.2 to 1.8	0.8 to 3.6	1.5	Yes	N/A	N/A	N/A
4	Buck	4 to 15	1.8 to 3.55	1.0 to 5.0	0.8	Yes	N/A	N/A	N/A
5	Buck	4 to 15	3.0 to 5.0	N/A	2	Yes	Yes	N/A	N/A
6	Buck or buck boost	4 to 15	3.5 to 5.5	1.0 to 5.0	2 (buck) 1.5 (buck boost)	Yes	Yes	N/A	N/A

[1] Channel 1 has two available voltage ranges.

Discharge Switch, Channel 1 to Channel 3

Each channel incorporates a discharge switch. For Channel 1 and Channel 2, the discharge switch is located at the FB1 and FB2 pins, respectively; for Channel 3, the discharge switch is located at the SW3 pin. The discharge switch can be turned on when the corresponding channel output is turned off, removing the residual charge of the external capacitor via a 125 Ω resistor. The discharge switch can be enabled by setting the appropriate DSCGx_ON bit in Register 1.

Gate Scaling (Channel 1 Only)

Channel 1 features a gate scaling function, which improves efficiency in light load conditions. When enabled by setting the GATE_SCAL1 bit in Register 32, gate scaling halves the size of the Channel 1 switching FETs, reducing the gate charge-up current—which is a non-negligible loss element in light load conditions—while allowing increased R_{DSON}, whose effect is less significant in these conditions. When gate scaling is enabled, only SW1A is used for the Channel 1 switch node because it is assumed that the load current is light.

Dynamic Voltage Scaling (DVS) Function

Channel 1 and Channel 2 incorporate a dynamic voltage scaling (DVS) function. DVS provides a stair-step transition in output voltage when the preset value for the output voltage is reprogrammed on the fly (see Figure 39).

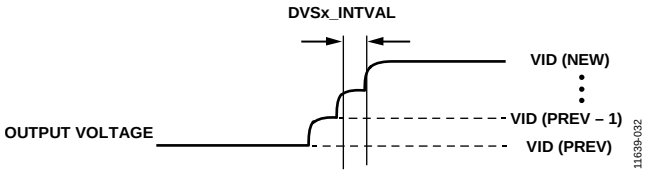

Figure 39. DVS Operation

The output voltage for Channel 1 is programmed using the VID1 bits in Register 12; the output voltage for Channel 2 is programmed using the VID2 bits in Register 13. When the DVS function is enabled, the voltage transition takes place according to the steps set by the VID1 or VID2 bits (see Table 39 and Table 41). The transition time from one step to the next is specified by the interval programmed in Register 17 using the DVSx_INTVAL bits (where x is 1 or 2). The DVS function is enabled by setting the EN_DVSx bit in Register 17.

For Channel 2, DVS operation is limited to an output voltage range of 1.0 V to 1.25 V.

When Channel 1 or Channel 2 is configured for DVS operation, toggling EN low does not immediately reset the VID code to its initial state. Instead Channel 1 or Channel 2 returns to its configured output voltage according to the steps set by the VID1 or VID2 bits (see Table 39 and Table 41, respectively).

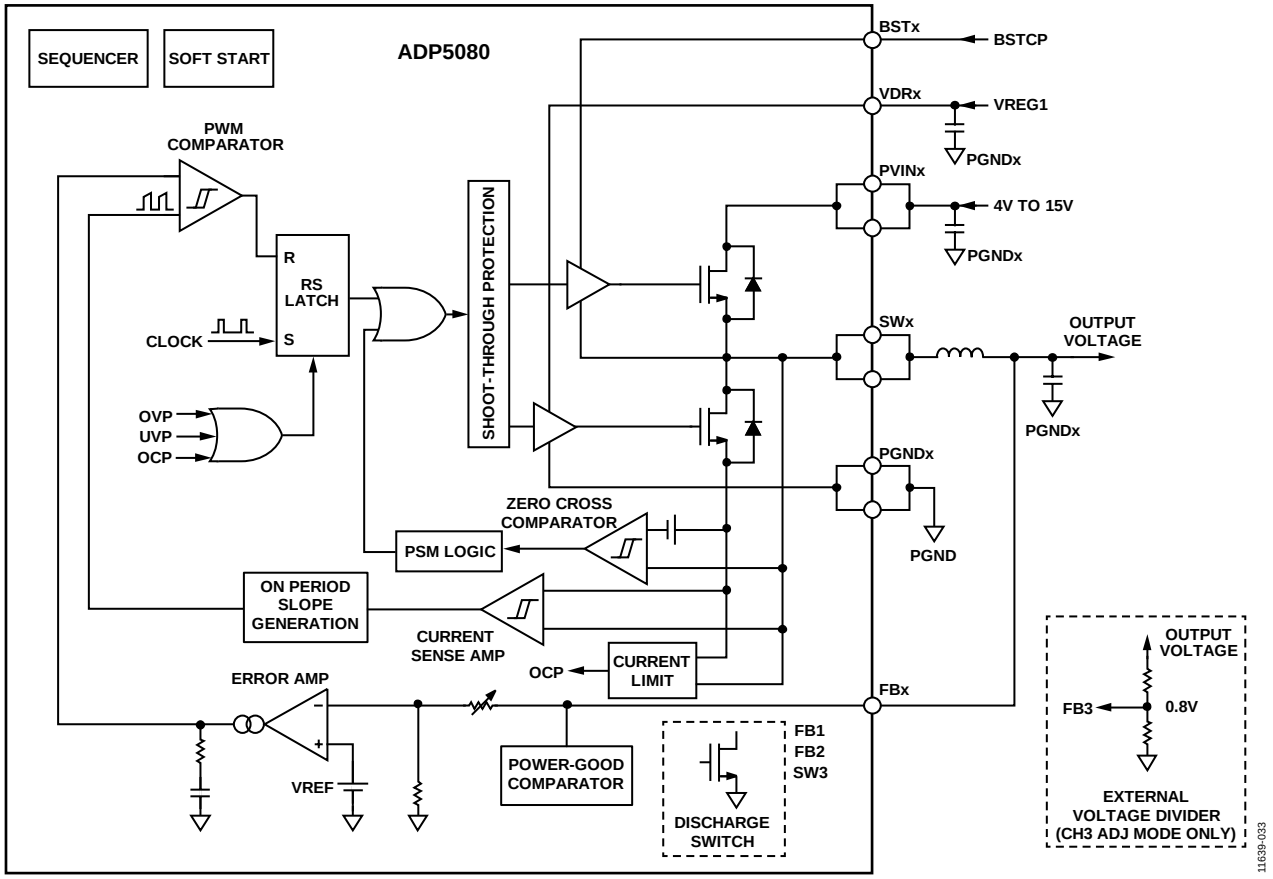

Figure 40. Buck Regulator Block Diagram: Channel 1, Channel 2, and Channel 3

Channel 4 and Channel 5: Current Mode Buck Regulators

Channel 4 and Channel 5 are internally compensated current mode control buck regulators (see Figure 41). Combined with the integrated charge pump, these channels are designed to operate at high duty cycles up to 100%.

Selecting the Output Voltage, Channel 4 and Channel 5

The output voltage of Channel 4 or Channel 5 is selected from one of the preset values available in the VIDx bits, where x is 4 or 5 (see Table 43). The default output voltage value is factory fuse programmed.

Channel 4 has an adjustable mode option that can be selected using the VID4 bits. When the adjustable output voltage mode is selected, the output voltage is set by an external feedback resistor divider. Select resistor values such that the desired output voltage is divided down to 0.8 V and the paralleled resistance seen from the dividing node does not exceed 25 kΩ (see the Setting the Output Voltage (Adjustable Mode Channels) section). When using the adjustable mode for Channel 4, be aware of the minimum on time restriction, which may limit the range of available output voltages.

Channel 4 and Channel 5 are designed for very high duty cycle operation. However, at very low duty cycle, these channels have a limited range due to the minimum on time restriction (75 ns typical) inherent in current mode control. The maximum input voltage capability for a given output voltage can be determined using the following equation:

$$V_{IN\_MAX} = V_{OUT}/(t_{ON\_MIN} \times f_{SW})$$

If the input voltage rises above this level, the output voltage continues to be regulated; however, switching pulses are skipped, which may increase output voltage ripple.

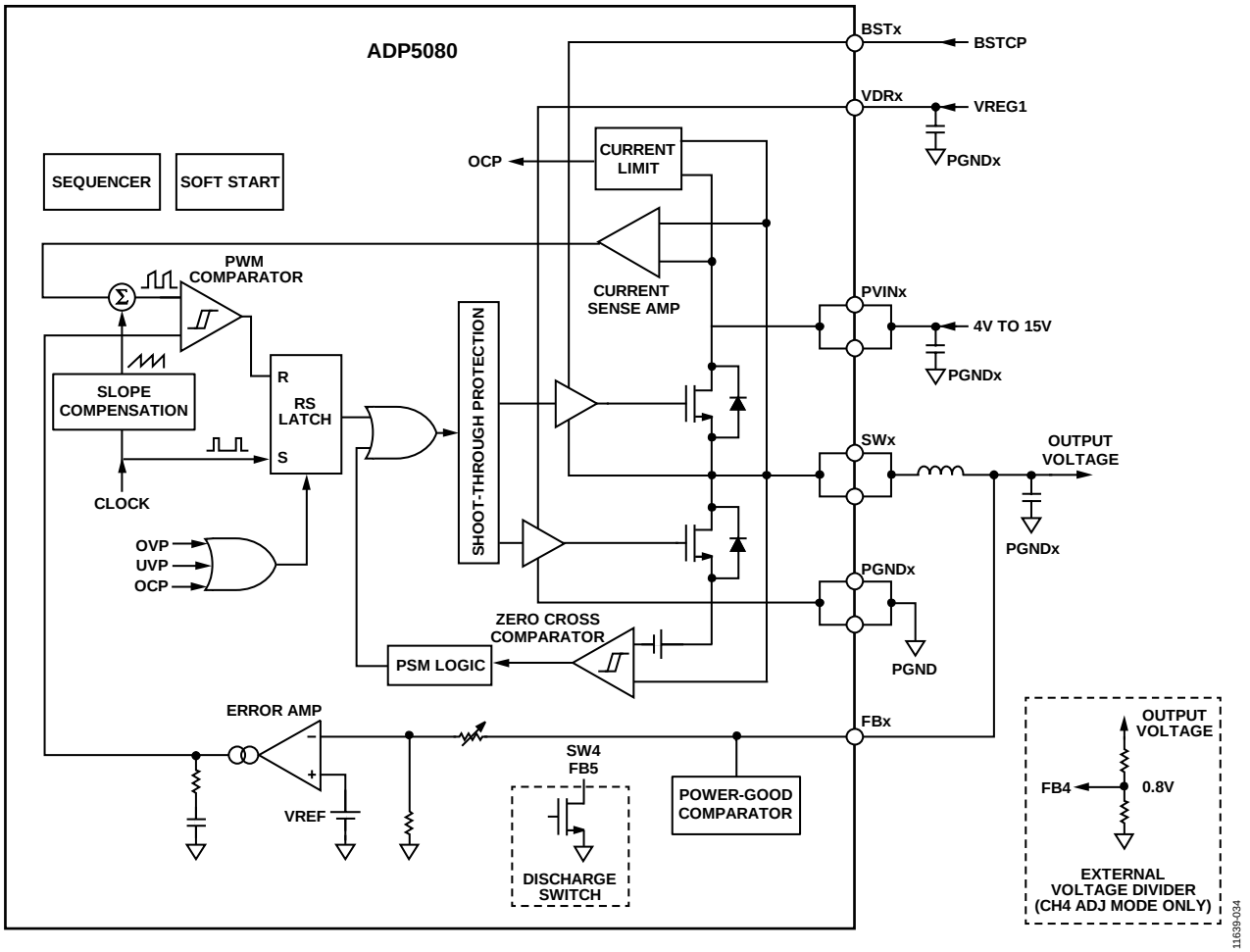

Figure 41. Buck Regulator Block Diagram: Channel 4 and Channel 5

Current-Limit Protection, Channel 4 and Channel 5

Channel 4 and Channel 5 have integrated cycle-by-cycle current-limit protection. In this type of current-limit protection, inductor current is sensed throughout the high-side on cycle. If the inductor current rises above the current-limit threshold during this time, the switching pulse is immediately terminated until the next cycle. This behavior causes the duty cycle to decrease, which in turn causes the output voltage to fall. The falling output voltage then toggles the PWRGx, UVx, and $\overline{\text{FAULT}}$ error flags. Because there is substantial parasitic noise at the rising edge of the high-side switch, some blanking time is required to prevent false current-limit triggering. This required blanking time determines the minimum on time of the channel.

Unlike valley mode current-limit protection, peak mode current-limit protection has no inherent frequency foldback. In extreme conditions such as a short circuit or inductor saturation, peak mode current limit is susceptible to runaway inductor current. To prevent this, the ADP5080 provides frequency foldback on Channel 4, Channel 5, and Channel 6. When the output voltage falls below approximately 80% of its nominal value, the switching frequency is halved. The frequency is halved again if the output voltage falls below approximately 40% of its nominal value. The frequency foldback feature allows more time for inductor current to decay, eliminating the possibility of current runaway.

Table 3 provides the peak current-limit threshold specifications. The actual load current-limit threshold varies with inductor value, frequency, and input and output voltage.

Discharge Switch, Channel 4 and Channel 5

Each channel incorporates a discharge switch. For Channel 4, the discharge switch is located at the SW4 pin; for Channel 5, the discharge switch is located at the FB5 pin. The discharge switch can be turned on when the corresponding channel output is turned off, removing the residual charge of the external capacitor via a 125 Ω resistor. The discharge switch can be enabled by setting the appropriate DSCGx_ON bit in Register 1.

Channel 6: Buck or Buck Boost Regulator

Channel 6 is a current mode control, four-switch buck boost regulator that can be configured as a buck only regulator. In a system in which the input voltage never falls below the Channel 6 output, using the buck only configuration reduces the losses caused by the switching FETs of the boost side. The buck only configuration yields better power efficiency, as well as lower output ripple and noise.

Buck Only Configuration

For the buck only configuration, set the BUCK6_ONLY bit (Bit 4 in Register 30) to 1. The default value of this bit is factory fuse programmed. When Channel 6 is configured for buck only mode, connect the inductor between the SW6A and VOUT6 pins, leaving the SW6B pin open (see Figure 42). This configuration bypasses the boost side switching FET.

Buck Boost Configuration

For the buck boost configuration, set the BUCK6_ONLY bit (Bit 4 in Register 30) to 0. The default value of this bit is factory fuse programmed. For the buck boost configuration, connect the inductor between the SW6A and SW6B pins (see Figure 42). Make sure that no capacitor is connected to the SW6B pin.

In buck boost operation, Channel 6 automatically switches between the buck and boost modes as the input voltage varies.

- In buck mode, the primary FETs (SW6A) switch with the SW6B high-side FET operating at 100% duty cycle.
- In boost mode, all four FETs are typically switching, although the primary high-side FET is capable of a 100% duty cycle.

When the input voltage is close to the output voltage, Channel 6 operates in buck boost mode with all four power FETs switching. This four-switch mode of operation ensures a smooth transition and excellent regulation, regardless of input voltage conditions.

The BOOST6_VTH bits (Bits[1:0] in Register 30) set the input voltage threshold for the boost FETs to start switching. A lower threshold provides higher efficiency because the region where all four switches are in operation is smaller. The lowest setting for these bits (11) sets an input voltage threshold that is still high enough to prevent dropout in most cases. However, under heavy load current at the lowest threshold setting, the buck side may reach a 100% duty cycle and some output droop may occur. The second lowest setting for these bits (00) is recommended for heavy load applications. The default value of these bits is factory fuse programmed.

Selecting the Output Voltage, Channel 6

The output voltage of Channel 6 is selected from one of the preset values available in the VID6 bits (see Table 45). The default output voltage value is factory fuse programmed.

Channel 6 has an adjustable mode option that can be selected using the VID6 bits. When the adjustable output voltage mode is selected, the output voltage is set by an external feedback resistor divider. Select resistor values such that the desired output voltage is divided down to 0.8 V while the paralleled resistance seen from the dividing node does not exceed 25 kΩ (see the Setting the Output Voltage (Adjustable Mode Channels) section).

Because Channel 6 can operate in boost mode, there is no practical output voltage limitation other than the maximum rating. When using the adjustable output voltage in buck only mode, be aware of the minimum on time restriction, which may limit the range of available output voltages. The minimum on time limitation is essentially the same as for Channel 4 and Channel 5 (see the Selecting the Output Voltage, Channel 4 and Channel 5 section).

Current-Limit Protection, Channel 6

Like Channel 4 and Channel 5, Channel 6 has integrated cycle-by-cycle current-limit protection. In this type of current-limit protection, inductor current is sensed throughout the high-side on cycle. The Channel 6 current limit is sensed on the primary high-side FET (SW6A). For more information, see the Current-Limit Protection, Channel 4 and Channel 5 section.

Discharge Switch, Channel 6

Each channel incorporates a discharge switch. For Channel 6, the discharge switch is located at the VOUT6 pin. The discharge switch can be turned on when the Channel 6 output is turned off, removing the residual charge of the external capacitor via a 110 Ω resistor. The discharge switch can be enabled by setting the DSCG6_ON bit in Register 1.

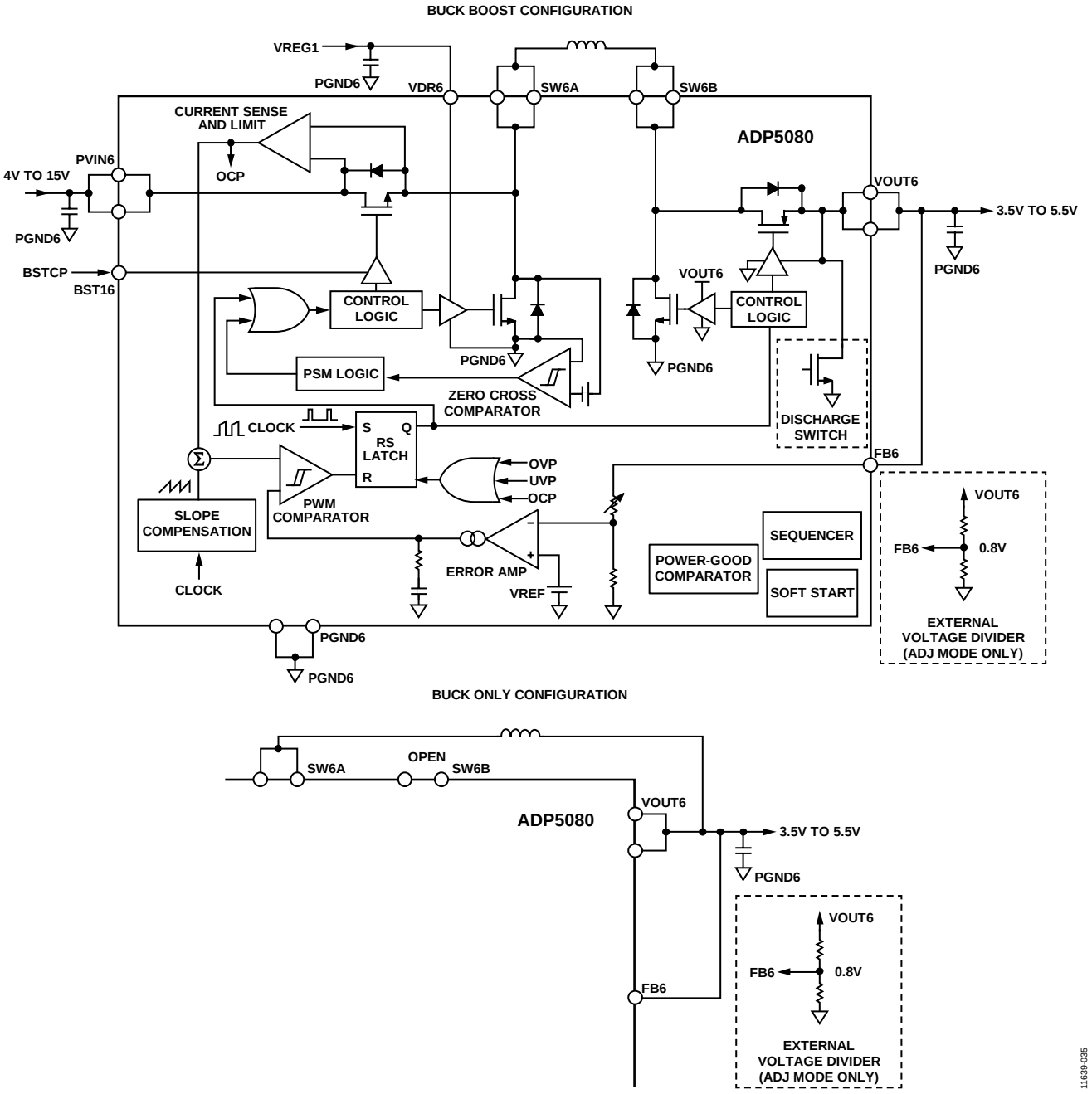

Figure 42. Channel 6 Buck or Buck Boost Regulator Block Diagram

LIGHT LOAD AND OTHER MODES OF OPERATION FOR THE DC-TO-DC CONVERTER CHANNELS

Each dc-to-dc converter channel in the ADP5080 has two or three options to handle light load conditions, whereas asynchronous dc-to-dc converters simply transition to discontinuous conduction mode (DCM). Although light load modes provide higher efficiency and longer battery life, they are also associated with increased ripple and noise. This trade-off requires the user to select the option that best suits the application, usually on a channel by channel basis (see Table 9). The modes of operation are illustrated in Figure 43, which shows the inductor current and the switch node in auto PSM, auto DCM, and FPWM modes.

Slew Rate Adjustment

Each channel has a slew rate adjustment option, which is set using the ADJ_SRx bit (where x is 1 to 6) in the OPT_SR_ADJ register (Register 31). When the ADJ_SRx bit is set, the switch node slew rate for the channel is reduced, which in turn reduces high frequency spike noise. Enabling this feature reduces the efficiency of the channel, however, due to increased switching losses. For this reason, use the slew rate adjustment feature only when low output noise is critical.

Forced PWM (FPWM) Mode

Forced pulse-width modulation (FPWM) mode maintains PWM operation despite light load conditions, allowing negative current to flow from the inductor through the low-side switching FET. This mode is also referred to as continuous conduction mode (CCM). The FPWM option has the lowest efficiency, but may be selected when constant frequency and low ripple are absolutely required, regardless of load.

Auto DCM

Automatic discontinuous conduction mode (auto DCM) is available on Channel 5 and Channel 6. Auto DCM turns off the low-side switching FET when the inductor current falls to zero during the t_{OFF} period, preventing negative current from flowing through the low-side FET. This operation is equivalent to that of traditional flywheel diode-based PWM regulators. Auto DCM has higher efficiency than FPWM mode because negative inductor current is not allowed, but rather is recirculated to the input side. At very light loads in auto DCM, some pulse skipping occurs and, therefore, switching is not at a constant frequency.

Auto PSM

Automatic power save mode (auto PSM) is similar to auto DCM, except that it intentionally turns on the high-side FET with a fixed period (approximately 80% of nominal t_{ON}). This operation forces the regulator to skip a number of PWM cycles. Compared to auto DCM, auto PSM skips a larger number of cycles and begins skipping cycles at a higher load current. Auto PSM reduces switching losses dramatically and improves efficiency, as shown in Figure 44. However, in light load conditions, larger output voltage ripple can be expected.

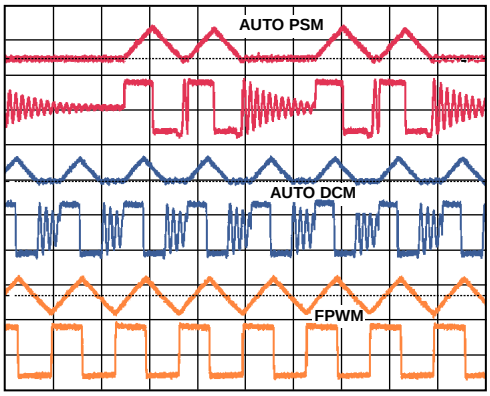

Figure 43. Auto PSM, Auto DCM, and FPWM Operation (Switch Node and Inductor Current Shown, Dashed Line Indicates 0 A)

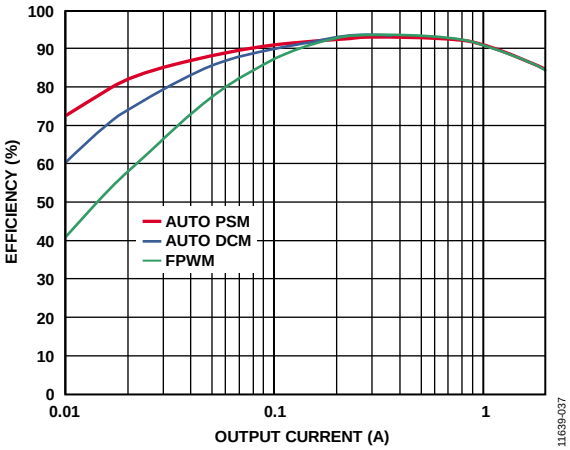

Figure 44. Efficiency of Auto PSM, Auto DCM, and FPWM Operation

Selecting Light Load Switching Modes

Each dc-to-dc converter channel can be configured with its own light load switching mode using the AUTO-PSMx bits in Register 28 and, for Channel 5 and Channel 6, the DCM56 bit in Register 32 (see Table 10 and Table 11).

Table 10. Light Load Switching Modes, Channel 1 to Channel 4

AUTO-PSMx Bit	Light Load Switching Mode
0	FPWM
1	Auto PSM

Table 11. Light Load Switching Modes, Channel 5 and Channel 6

AUTO-PSMx Bit	DCM56 Bit	Light Load Switching Mode
0	X[1]	FPWM
1	0	Auto PSM
1	1	Auto DCM

[1] X = don't care.

SWITCHING CLOCK

The ADP5080 integrates a highly accurate switching clock for the dc-to-dc converters and the charge pump. As shown in Figure 45, the internal clock can also be bypassed and the system synchronized to an external clock. When the internal clock source is used, the switching frequency for each dc-to-dc converter and the charge pump can be configured.

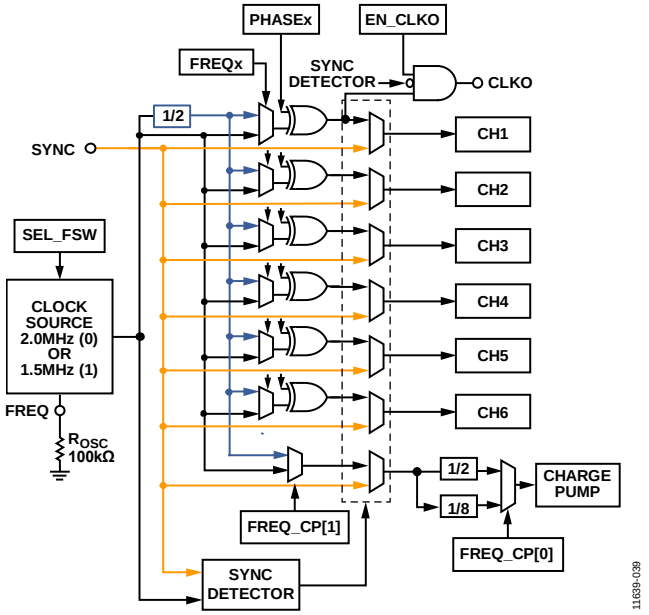

Figure 45. Switching Clock Distribution

External Synchronization Mode

When an external clock is present at the SYNC pin, all dc-to-dc converters and the charge pump automatically use it as their master switching clock; the FREQx bit settings in Register 18 are ignored. When using external synchronization mode, ensure that the external clock is already stable before the EN signal is asserted to avoid unexpected behavior in the converters. When an external clock is used, the clock must operate within the specifications listed in Table 1.

Selecting the Internal Clock Frequency

If the SYNC pin is tied high or low, the device uses the internal clock. The internal oscillator generates a master clock at either 2.0 MHz or 1.5 MHz, as specified by the SEL_FSW bit in Register 18. The internal clock is active when EN is high.

The master clock is divided down by half so that each dc-to-dc converter can select 1× or 1/2× the master clock frequency. The frequency of each channel is set using the FREQx bit (where x is 1 to 6) in Register 18. For example, if the master clock is set to 1.5 MHz, Channel 1 through Channel 6 can be configured to operate at 750 kHz or 1.5 MHz, but not at 1 MHz or 2 MHz.

For the charge pump, the FREQ_CP bits set the switching frequency (see the Charge Pump Switching Frequency section).

Selecting the External Resistor

An external 100 kΩ resistor from the FREQ pin to GND is required for the internal clock source oscillator. To obtain an accurate clock frequency, select a high precision resistor with a low temperature coefficient. A 1 nF bypass capacitor is also recommended at the FREQ pin.

Phase Shifting

Each dc-to-dc converter can be configured to use the inverted phase of the master clock by setting the PHASEx bit (where x is 1 to 6) in Register 20. Setting channels out of phase with each other helps reduce rms current stress on the input capacitors and spreads switching energy over two cycles. Phase shifting reduces possible interference in a system due to propagated switching noise on the input rail.

When any channel is operated at 1/2 × f_{SW}, the higher frequency channel must be set out of phase to have any effect on the apparent phase of the lower frequency channel (see Figure 46).

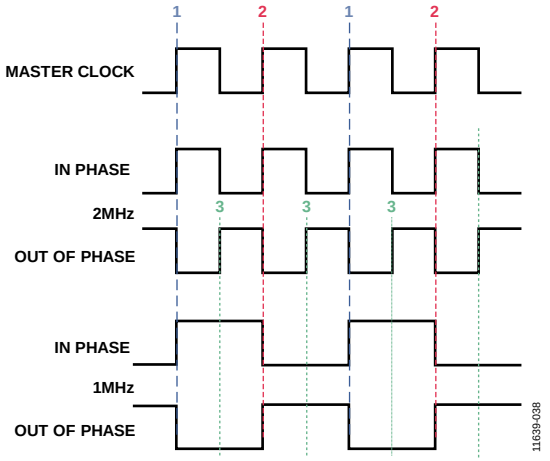

Figure 46. Switching Phase Relationships

Any channel at 1 × f_{SW} has the expected, set phase relationship to the master clock. However, when a channel operates at 1/2 × f_{SW}, it always appears to be in phase with the master clock and with any in-phase channel at 1 × f_{SW}. This relationship is illustrated by the lines labeled 1 and 2 in Figure 46; regardless of the phase setting, Line 1 or Line 2 is always aligned to the rising edge.

To set a channel operating at 1/2 × f_{SW} out of phase, the highest frequency channel must be set out of phase. Referring to the lines labeled 3 in Figure 46, the channel operating at 1/2 × f_{SW} is now out of phase with the channel operating at 1 × f_{SW}, regardless of the phase setting.

CLKO Pin

The clock output (CLKO) pin can output the internal switching clock used for Channel 1. The output is enabled by setting the EN_CLKO bit in Register 19 to 1. The CLKO output stays low when external clocking is used or when the EN_CLKO bit is set to 0.

SOFT START FUNCTION

To provide controlled output voltage ramping on startup, the ADP5080 incorporates soft start control for each dc-to-dc converter. The ramp-up period to reach the target voltage can be set to 1 ms, 2 ms, 4 ms, or 8 ms using the SSx bit (where x is 1 to 6) in Register 2 or Register 3. The default soft start values are factory fuse programmed. It is not recommended that the ADP5080 be started up into a full load condition.

CHANNEL 7: HIGH VOLTAGE LDO REGULATOR

The ADP5080 integrates a high voltage LDO linear regulator, which allows input voltages up to 25 V (see Figure 47). The LDO regulator outputs one of four preset regulated voltages and is capable of providing up to 30 mA.

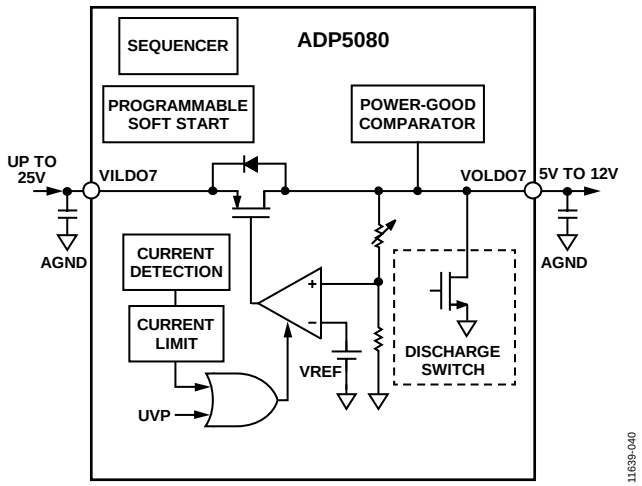

Figure 47. High Voltage LDO (Channel 7)

Selecting the Output Voltage, Channel 7

The output voltage of Channel 7 is selected from one of the preset values (12 V, 9 V, 6 V, or 5 V) using the VID7 bits in Register 16. The default value is factory fuse programmed.

Discharge Switch, Channel 7

Each channel incorporates a discharge switch. For Channel 7, the discharge switch is located at the VOLDO7 pin. The discharge switch can be turned on when Channel 7 is turned off, removing the residual charge of the external capacitor via an internal 1 kΩ resistor. The discharge switch can be enabled by setting the DSCG7_ON bit in Register 1.

CHARGE PUMP

The ADP5080 includes an integrated charge pump, which provides power to the high-side switching NMOS FET driver (see Figure 48). The charge pump raises the voltage applied to the PVINCP pin by the VDR5 pin voltage, making the voltage available at the BSTCP pin. In a typical application, the PVINCP pin is supplied by the battery (VBATT), and the VDR5 pin is supplied by VREG1 (5 V or 5.5 V). Thus, the output voltage at the BSTCP pin is VBATT + 5 V or 5.5 V, which is ideal for driving the high-side FET driver supply pin for each channel, BSTx.

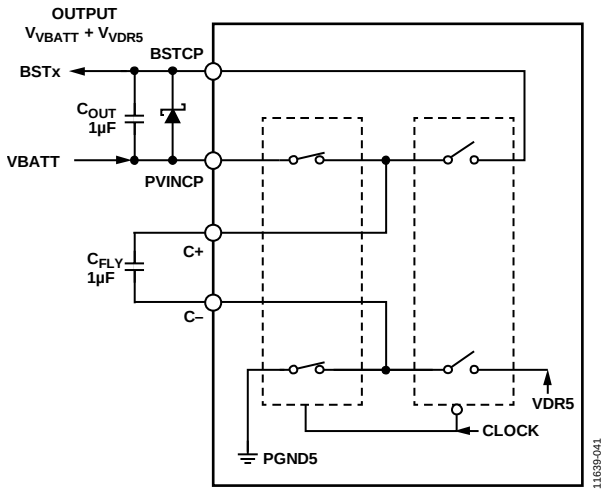

Figure 48. Charge Pump for BSTx Supply

The charge pump requires a minimum VBATT voltage to start up. In some cases, the start-up threshold, which is 4 V typical, may be higher than the rising UVLO threshold.

If the BSTCP voltage drops approximately 2.5 V below the nominal value, the ADP5080 shuts down to prevent abnormal switching. An OVP or UVP fault is not indicated in this case.

Charge Pump Switching Frequency

The internal clock source generates either 2.0 MHz or 1.5 MHz, as set by the SEL_FSW bit in Register 18. This master frequency is further divided by 1/2, 1/4, 1/8, or 1/16 by the FREQ_CP bits in Register 19 (see Table 53). If the master clock frequency is set to 2.0 MHz, the charge pump switching clock frequency can be 1.0 MHz, 500 kHz, 250 kHz, or 125 kHz. If the master frequency is set to 1.5 MHz, the charge pump switching clock frequency can be 750 kHz, 375 kHz, 188 kHz, or 94 kHz. Typically, a setting of 1/4 in 1.5 MHz operation or 1/8 in 2 MHz operation is recommended for the best efficiency. Lower settings may not provide enough boost voltage when all channels are operating at load.

If an external clock is used, the charge pump frequency can be set to 1/4 or 1/8 of the external frequency using the FREQ_CP bits. Charge pump efficiency is slightly affected by the duty cycle of the external clock; a 50% duty cycle is the optimal point of operation.

Capacitor Selection

A 1 µF capacitor is used for each charge pump capacitor (C_{FLY} and C_{OUT}; see Figure 48). The voltage rating of these capacitors must be adequate for the charge-up voltage, that is, the PVINCP pin voltage across C_{FLY} and the VDR5 pin voltage across C_{OUT}.

Protection Diode

It is strongly recommended that a protection diode be mounted as shown in Figure 48 to avoid problems during power-up while the BSTCP voltage is charging. Use a Schottky diode that can withstand a 1 A peak current.

Using the Charge Pump as the Channel 7 Input Supply

The charge pump can also be used to generate a high voltage for the Channel 7 input. This configuration is enabled by adding the circuit shown in Figure 49 in parallel with the BSTx generating circuit shown in Figure 48.

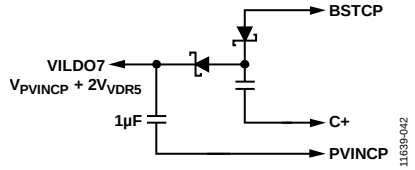

Figure 49. Charge Pump Used as a High Voltage Supply for Channel 7

The circuit shown in Figure 49 generates VILDO7 with the voltage V_{PVINCP} + 2 × V_{VDR5}. In a typical application, this voltage is equivalent to V_{VBATT} + 10 V to 11 V (PVINCP = VBATT; VDR5 = VREG1 = 5.5 V or 5 V).

ENABLING AND DISABLING THE OUTPUT CHANNELS

Each channel (Channel 1 to Channel 7) can be turned on and off using the sequencer mode or the manual mode. A channel configured for sequencer mode is automatically turned on and off by assertion and deassertion of the EN pin, with individually programmed delay times. A channel configured for manual mode does not automatically start when EN goes high, but can be turned on or off via I²C control, as required.

Sequencer Mode

When the MODE_ENx bit (x is 1 to 7) is set in Register 29, the specified channel turns on and off under the control of the internal sequencer, which is triggered by the EN pin (see Figure 50).

When the EN pin goes high, each channel controlled by the sequencer begins a soft start after the delay time specified by the EN_DLYx bits (see Table 23, Table 25, Table 27, and Table 29). Similarly, when the EN pin goes low, the channel turns off after the delay time specified by the DIS_DLYx bits (see Table 31, Table 33, Table 35, and Table 37).

Note that Figure 50 shows the logical states of each channel; it does not show soft start and discharge ramps. The disable delay time for all channels can be increased to four times its configured value by setting the DIS_DLY_EXTEND bit in Register 35.

When all channels controlled by the sequencer are turned on, each channel can be manually turned off or on using the CHx_ON bit (x is 1 to 7) in Register 48. When the CHx_ON bit is used to turn a channel on or off, the enable state of the channel changes immediately, regardless of the settings of the EN_DLYx and DIS_DLYx bits.

When using the sequencer mode, note the following:

- A channel that is controlled by the sequencer cannot be turned off manually until after the sequencer turns on all the channels that it controls and the soft start period has ended. This ready state can be identified by reading the PWRGx bits (x is 1 to 7) in Register 24.
- After the EN pin is asserted, writing to the VIDx bits is forbidden while the internal sequencer is in operation to prevent unexpected behavior. The internal sequencer is in operation from the assertion of the EN pin until the PWRGx bits in Register 24 go high.

Manual Mode

When the MODE_ENx bit (x is 1 to 7) is cleared in Register 29, the specified channel turns on and off under I²C control. All channels that are not configured for sequencer mode can be manually turned on or off using the CHx_ON bits (x is 1 to 7) in the PCTRL register (Register 48). Writing 1 to the CHx_ON bit enables the channel only when the EN pin is logic high.

When the EN pin is taken low, all channels configured for manual mode turn off immediately, and all the CHx_ON bits are reset to 0. While the EN pin is low, any data written to or read from the CHx_ON bits is not valid.

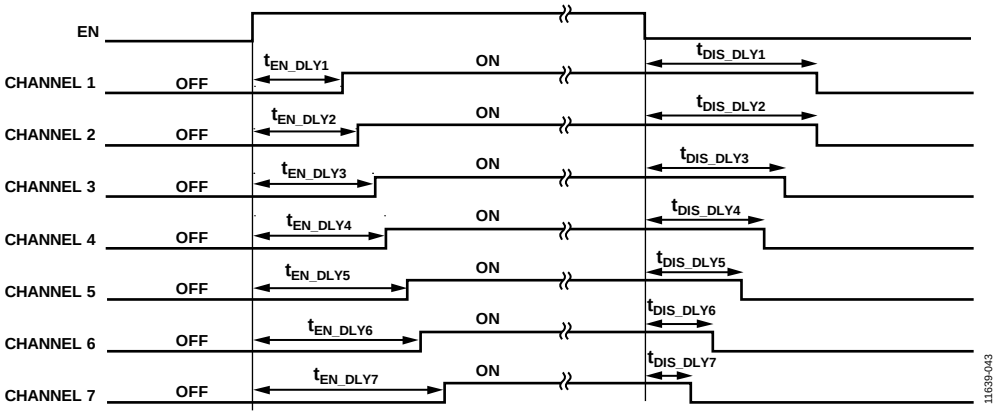

Figure 50. Example Power-Up/Power-Down Sequence Using Sequencer Mode

EN Function

The EN pin has an internal pull-down resistor that holds the ADP5080 in standby mode until the pin is actively pulled high. The EN function does not take effect until the device is ready for operation, that is, until all the following conditions are met:

- VBATT pin voltage ($V_{UVLO\ (BATT)}$) is above 3.3 V.
- VREG1 pin voltage is within the specified range.
- VREG2 pin voltage ($V_{UVLO\ (POR)}$) is within the specified range.
- Device is not in thermal shutdown.
- Internal oscillator is stable (typically 250 µs).
- PVIN1 pin voltage ($V_{UVLO\ (R)}$) is above 3.7 V.
- VDR12 pin voltage is above 2.95 V.

If any of these conditions are not met during operation, the ADP5080 shuts down, as described in the UVLO and POR section.

EN34 Function

The EN34 pin allows Channel 3, Channel 4, or both channels to be independently enabled and disabled using the EN34 pin. This functionality can be enabled on either or both channels using the DIS_EN34_CHx bits (x is 3 or 4) in Register 35.

When the DIS_EN34_CHx bit is set low, the channel is not turned on until both the EN and EN34 pins are high. If Channel 3 or Channel 4 is in sequencer mode, EN34 must be high before EN goes high to maintain the enable delay timing on the channels (see the Sequencer Mode section). If EN is high when the EN34 pin is taken high, Channel 3 or Channel 4 is immediately enabled or disabled, regardless of whether the channel is configured for manual mode or sequencer mode.

When the DIS_EN34_CHx bit is set high, Channel 3 or Channel 4 is enabled and disabled in the same way as all the other channels in the device, and the EN34 pin has no effect on the operation of the channel.

Regardless of the state of the DIS_EN34_CHx bits, disabling Channel 3 and Channel 4 does not cause $\overline{\text{FAULT}}$ to go low (see the Fault Function section). This means that the power-good flags for Channel 3 and Channel 4 do not need to be masked. $\overline{\text{FAULT}}$ goes low only when Channel 3 or Channel 4 is enabled using the CH3_ON or CH4_ON bit and the PWRG3 or PWRG4 bit subsequently goes low.

POWER-GOOD FUNCTION

The power-good status of each channel (PWRGx bit) can be read back from the PWRG register (Register 24). A value of 1 for the PWRGx bit indicates that the regulated output voltage of Channel x is within 85% to 125% of its nominal value. When the regulated output voltage of a channel falls below this level, the PWRGx bit is set to 0. As shown in Figure 51, hysteresis is applied to both the upper and lower boundaries to minimize power-good chattering.

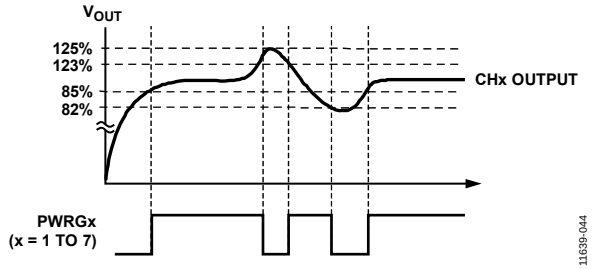

Figure 51. Power-Good Status Bit

FAULT FUNCTION

The $\overline{\text{FAULT}}$ pin is an open-drain output that indicates the logical OR status of the PWRGx bits for all channels. When any PWRGx bit = 0, the $\overline{\text{FAULT}}$ pin goes low. As shown in Figure 52, $\overline{\text{FAULT}}$ has approximately 70 ms of blanking time after EN is asserted to allow for the enable delay and soft start times. After the blanking period, a PWRGx low bit causes $\overline{\text{FAULT}}$ to go low immediately. $\overline{\text{FAULT}}$ remains low until the EN pin is toggled or power is cycled. If an OVP or UVP condition at startup forces a shutdown before the $\overline{\text{FAULT}}$ blanking period ends, $\overline{\text{FAULT}}$ does not go low.

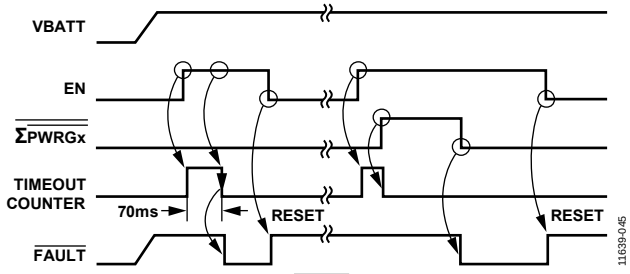

Figure 52. $\overline{\text{FAULT}}$ Function

If a channel is not enabled manually or via the sequencer, the PWRGx bit remains low. This forces $\overline{\text{FAULT}}$ low unless the channel is masked by the MASK_PWRGx bit in Register 25. This does not apply to Channel 3 and Channel 4, as described in the EN34 Function section.

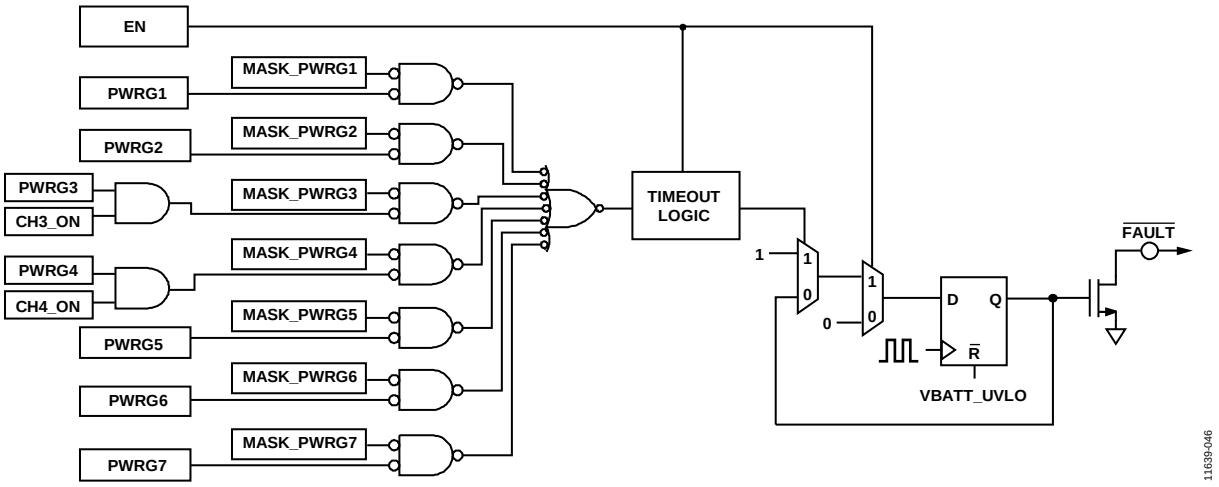

Figure 53. Fault Function Logic Diagram

Table 12. Channel 5 Standalone Undervoltage Detection Option

	Undervoltage Detected		
SEL_IND_UV5 Bit	**Any Channel Other Than Channel 5**	**Channel 5**	**Output**
0	Yes	Yes	All channels shut down
	Yes	No	All channels shut down
	No	Yes	All channels shut down
	No	No	All channels are operational
1	Yes	Yes	All channels shut down
	Yes	No	All channels shut down
	No	Yes	Channel 5 shuts down; all other channels are operational
	No	No	All channels are operational

UNDERVOLTAGE PROTECTION (UVP)

The ADP5080 incorporates undervoltage protection (UVP) on Channel 1 to Channel 7. When the output of any channel falls below 65% of the specified voltage, UVP shuts down all seven channels by internally resetting the CHx_ON bits in Register 48. Channel 5 can be configured for standalone undervoltage protection (see the Channel 5 Standalone Undervoltage Detection Option section).

UVP Detection Delay

Undervoltage detection includes a debounce delay, which is configured in Register 23 (see Table 57). The undervoltage condition is recognized only after it continues for the period specified by the UV_DLY bits in Register 23 (see Figure 54). Setting the UV_DLY bits to 11 disables UVP.

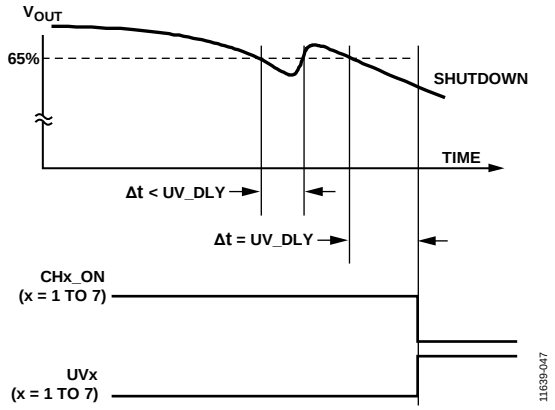

Figure 54. Undervoltage Detection Delay

Channel 5 Standalone Undervoltage Detection Option

If desired, undervoltage protection on Channel 5 can be isolated from UVP on all the other channels. When the SEL_IND_UV5 bit is set high in Register 34, an undervoltage condition on Channel 5 causes only Channel 5 to be shut down (see Table 12). If this option is selected, the UV_DLY5 bits in Register 34 can be used to set a UVP detection delay for Channel 5 only.

Recovering from UVP

After the cause of the undervoltage condition is removed, the outputs can be recovered by toggling EN from low to high. If standalone Channel 5 undervoltage shutdown is enabled (by setting the SEL_IND_UV5 bit in Register 34), Channel 5 can be recovered by setting the CH5_ON bit in Register 48 to 1.

The undervoltage status of a channel is stored in the UVPST register (Register 26) after shutdown and can be read back from the UVx bit in Register 26. The UVx bit is cleared by writing a 1 to it.

OVERVOLTAGE PROTECTION (OVP)

The ADP5080 incorporates overvoltage protection (OVP) on Channel 1 to Channel 6. When the output of any of these channels rises above 125% of the specified voltage, OVP shuts down all six channels by internally resetting the CHx_ON bits in Register 48.

OVP Detection Delay

Overvoltage detection includes a debounce delay, which is configured in Register 23 (see Table 57). The overvoltage condition is recognized only after it continues for the period specified by the OV_DLY bits in Register 23 (see Figure 55). Setting the OV_DLY bits to 11 disables OVP.

Recovering from OVP

After the cause of the overvoltage condition is removed, the outputs can be recovered by toggling EN from low to high. The overvoltage status of a channel is stored in the OVPST register (Register 27) after shutdown and can be read back from the OVx bit in Register 27. The OVx bit is cleared by writing a 1 to it.

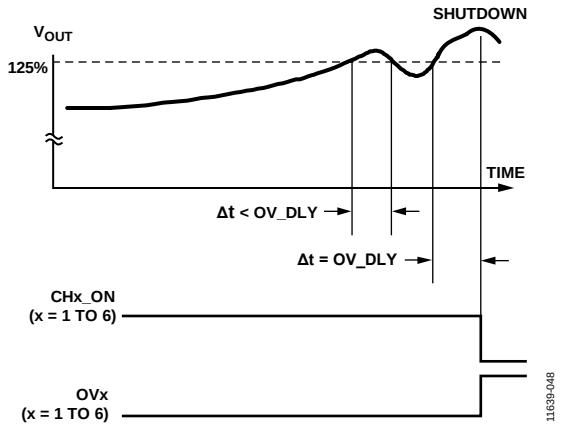

Figure 55. Overvoltage Detection Delay

APPLICATIONS INFORMATION

This section provides component and PCB layout guidelines to ensure optimal device performance, efficiency, stability, and minimal switching noise and crosstalk.

COMPONENT SELECTION FOR THE BUCK AND BUCK BOOST REGULATORS

Setting the Output Voltage (Adjustable Mode Channels)

Channel 3, Channel 4, and Channel 6 can be configured for an adjustable output voltage. Table 9 provides the adjustable output voltage range for these channels. When any of these channels is configured for adjustable mode, connect a resistor divider to the FBx pin between V_{OUT} and GND, as shown in Figure 56.

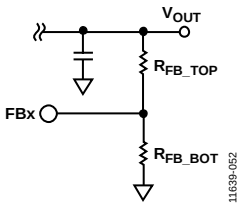

Figure 56. Feedback Resistors for Adjustable Output

The resistor values can be calculated as follows, where 0.8 V is the typical FB voltage, and 20 kΩ is a good typical value for R_{FB_BOT}.

$$R_{FB\_TOP} = \frac{(V_{OUT} - 0.8\text{V}) \times R_{FB\_BOT}}{0.8\text{V}}$$

Note that changing the output voltage often requires a change to the inductor (L) and output capacitor (C_{OUT}) values. After the V_{OUT} value is selected, calculate and test the L and C_{OUT} values (see the Selecting the Inductor section and the Selecting the Output Capacitor section).

Selecting the Inductor

The required inductor value can be determined by the input and output voltages, the switching frequency, and the ripple current, as shown in Equation 1.

$$L = \frac{V_{IN} - V_{OUT}}{I_{RIPPLE}} \times \frac{1}{f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \quad (1)$$

where:
L is the inductor value.
f_{SW} is the switching frequency.
I_{RIPPLE} is a peak-to-peak value for the ripple current.

In general, the recommended ripple current is 30% of the maximum load current. Therefore, Equation 1 can be rewritten as follows:

$$L = \frac{V_{IN} - V_{OUT}}{0.3 \times I_{LOAD}} \times \frac{1}{f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \quad (2)$$

Note that ripple current varies with input voltage. The typical input voltage can be used to determine the inductor value. However, to avoid inductor saturation and current limit, also calculate the inductor value with the worst-case input voltage (V_{IN} max).

The maximum rated current of the selected inductor (both rms current and saturation current) must be greater than the peak inductor current (I_{PEAK}) at the maximum load current. If the rating of the inductor is not sufficient, the inductor may saturate due to inductor value degradation, causing it to reach the current limit, even in a lower load condition than expected.

The peak current can be estimated using Equation 3.

$$I_{PEAK} = I_{LOAD} + (I_{RIPPLE}/2) \quad (3)$$

If the 30% ripple guideline is followed, typical peak current is simplified as follows:

$$I_{PEAK} = (I_{LOAD} + 0.15) \times I_{LOAD} = 1.15 \times I_{LOAD} \quad (4)$$

Another important specification to consider is the parasitic series resistance in the inductor: dc resistance (DCR). A larger DCR decreases efficiency, but a larger size inductor typically has lower DCR. Therefore, the trade-off between available space on the PCB and device performance must be considered carefully.

Equation 1 to Equation 4 apply to the buck regulators. Although Channel 6 is a buck boost regulator, the inductor value can be determined using the buck regulator mode of operation given that the available step-up ratio in boost mode is relatively small (4 V at the PVIN6 pin to 5.5 V at the VOUT6 pin) compared to the available step-down ratio. Therefore, an inductor value selected for buck regulator mode typically works equally well in boost regulator mode.

Table 13 lists recommended inductor values for a range of voltages and frequencies. The values provided are based on a wide operating range and assume the maximum load current for each channel. In the actual application, larger or smaller values may be more appropriate. In general, the inductor value can be increased or decreased by one standard value from the recommended 30% ripple guideline. A larger inductance provides higher efficiency, whereas smaller values results in better transient response and a smaller footprint. Note that inductor values much smaller or larger than the ones recommended in Table 13 may cause control loop instability.

It is also important to note that because the current-limit protection monitors peak or valley current, the selected inductance affects the load current level at which current limit is triggered.

Table 13. Suggested Inductors

Channel	V_{OUT} (V)	Frequency (kHz)	Inductance (µH)	Part Number
1	<1.0	750 or 1000	1	Toko FDSD0420-H-1R0
		1500 or 2000	0.47	Toko FDSD0420-H-R47
	1.0 to 1.2	750 or 1000	1.5	Toko FDSD0420-H-1R5
		1500 or 2000	0.68	Toko FDSD0420-H-R68
2	<1.8	750 or 1000	4.7	Toko FDSD0420-H-4R7
		1500 or 2000	2.2	Toko FDSD0420-H-2R2
	1.8 to 3.3	750 or 1000	6.8	Taiyo Yuden NRS4018T6R8M
		1500 or 2000	3.3	Toko FDSD0420-H-3R3
3	<1.5	750 or 1000	3.3	Toko FDSD0420-H-3R3
		1500 or 2000	1.5	Toko FDSD0420-H-1R5
	1.5 to 1.8	750 or 1000	3.3	Toko FDSD0420-H-3R3
		1500 or 2000	1.5	Toko FDSD0420-H-1R5
4	<2.5	750 or 1000	6.8	Taiyo Yuden NRS4018T6R8M
		1500 or 2000	3.3	Toko FDSD0420-H-3R3
	2.5 to 3.55	750 or 1000	10	Taiyo Yuden NRS4018T100M
		1500 or 2000	4.7	Toko FDSD0420-H-4R7
5	<4	750 or 1000	3.3	Toko FDSD0420-H-3R3
		1500 or 2000	2.2	Toko FDSD0420-H-2R2
	4 to 5	750 or 1000	3.3	Toko FDSD0420-H-3R3
		1500 or 2000	1.5	Toko FDSD0420-H-1R5
6	<4.5	750 or 1000	4.7	Toko FDSD0420-H-4R7
		1500 or 2000	2.2	Toko FDSD0420-H-2R2
	4.5 to 5.5	750 or 1000	4.7	Toko FDSD0420-H-4R7
		1500 or 2000	3.3	Toko FDSD0420-H-3R3

Selecting the Input Capacitor

Step-down switching regulators draw current from the input supply in pulses that have very fast rise and fall times. Low ESR ceramic input capacitors are required to reduce the input voltage ripple and provide bypass for high frequency switching noise. If not well bypassed, the input noise can cause poor device performance, instability, and increased conducted and radiated emissions (EMI).

Each switching channel should have approximately 10 µF of input bypass capacitance. Place the input capacitors as close as possible to the PVINx and PGNDx pins. Place an additional ceramic input capacitor at VBATT. It is usually beneficial to use multiple capacitors in parallel instead of a single high value capacitor.

Note that ceramic capacitors have very strong dc bias characteristics and lose as much as 80% of their capacitance value at the rated voltage. Also, note that the rise in case temperature due to rms current in the input capacitor can be quite high on the input of a buck regulator. For these reasons, capacitors of X5R and X7R type or better are recommended. A good estimate for the rms current in the input capacitor of a single channel is

$$I_{RMS} = \frac{I_{LOAD} \times \sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

Selecting the Output Capacitor

The output capacitor is important for regulator operation because it affects the loop stability, output voltage ripple, and load transient response.

The ADP5080 is designed to operate with low ESR ceramic output capacitors. Higher output capacitor values reduce the output voltage ripple and improve load transient step response. When choosing an output capacitor value, it is also important to account for the loss of capacitance due to output voltage dc bias.

Table 14 lists the minimum recommended capacitor values for each channel. Note that the capacitor values shown in Table 14 are nominal values, not derated values. The capacitors listed work for the full range of operating frequency and load.

Lower values can be used at higher frequency or lighter load currents. However, exercise caution when using values smaller than the minimum recommended values; too small an output capacitor can result in unstable operation. Output capacitance can typically be increased with no practical limit without causing stability problems. Greater capacitance improves ripple and transient performance.

Table 14. Minimum Recommended Output Capacitors

Channel	Output Capacitor (µF)
1	44
2	44
3	44
4	33
5	44
6	44

Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric that is adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of at least 2 × V_{OUT} are recommended for best performance.

The peak-to-peak output voltage ripple for the selected output capacitor and inductor values is calculated using Equation 5.

$$V_{RIPPLE} = \frac{V_{IN}}{(2\pi \times f_{SW}) \times 2 \times L \times C_{OUT}} = \frac{I_{RIPPLE}}{8 \times f_{SW} \times C_{OUT}} \quad (5)$$

High ESR capacitors are not recommended because they increase output ripple and can cause loop instability. Equation 5 assumes ceramic capacitors and does not include ESR.

For optimal performance, place output capacitors to minimize PCB parasitics. Connect capacitor pads directly to the output and GND power paths, not via separate traces. For purposes of high frequency noise reduction, it can be beneficial to use multiple capacitors in parallel instead of a single high value capacitor.

Because Channel 6 operates in buck boost mode, the output capacitors see large switching currents. Therefore, placement of the output capacitors requires additional attention. Make sure to place the output capacitors as close as possible to the VOUT6 and PGND6 pins of Channel 6.

COMPONENT SELECTION FOR THE LDO REGULATORS

Selecting the Capacitors

Use low ESR capacitors for all LDO input and output capacitors. Lower ESR reduces the output impedance and ripple voltage. High ESR capacitors are not recommended due to ripple and stability of the LDO control loop. Therefore, it is recommended that surface-mount ceramic capacitors be used. The X5R and X7R type of capacitor is preferable for adequate performance.

Use an output capacitor with a value from 2.2 µF to 10 µF for VREG2. Values of 4.7 µF to 10 µF are recommended for VREG1; 4.7 µF is the minimum requirement for stability.

For the Channel 7 high voltage LDO regulator, the minimum required output capacitor value for the VOLDO7 pin is 1 µF. Because Channel 7 is a high voltage output, make sure to account for capacitor bias voltage derating. If the charge pump doubler circuit is used as the input supply to Channel 7, the maximum recommended value for the Channel 7 output capacitor is 3.3 µF. This is to prevent overloading the charge pump during startup.

PCB LAYOUT RECOMMENDATIONS

Proper printed circuit board (PCB) layout is essential for optimal device performance and thermal dissipation, and to minimize switching noise and electromagnetic interference (EMI). A few key layout guidelines are provided in the following sections.

Sensitive Signal Treatment

It is important to isolate sensitive signal traces from noisy switching traces. The FBx pins and the FREQ pin are sensitive to noise coupling and should be routed away from noise sources. Any node with high dV/dt—such as SWx, BSTx, and SCL—is considered a noise source.

Additional noisy circuit areas to avoid are the main areas of high switching current: primarily the input capacitors and PGNDx connections. Finally, do not route sensitive nodes below or near the inductors. If a sensitive signal trace must cross a noisy source, it is recommended that at least one PCB ground layer be placed between these signal traces as a shield.

Grounding

It is recommended that the analog ground (AGND) and power ground (PGND) planes be separated. The AGND plane is used for the device reference voltage; therefore, it should be as quiet as possible and not used as a current path. The PGND plane serves as the current return path for the regulators. PGND can be very noisy due to the flow of current, as well as the presence of switching noise. Therefore, care must be taken with the connection of the AGND and PGND planes so that currents flowing in the PGND plane do not intrude on the AGND region. Connect the AGND and PGND planes at a single point, preferably at the device.

The PGNDx nodes are part of the regulation loop for each switching regulator and carry fast switching currents. Therefore, it is critical that the PGNDx regions for each switching regulator be separated and connected to the PGND plane at the output capacitor ground. This prevents interference from adjacent channels and helps contain switching noise. Multiple vias are recommended for the connection between the PGNDx regions and the PGND plane.

To improve thermal performance and noise immunity, each AGND or PGND layer should have as much copper coverage as possible.

External Component Placement and Signal Routing

The majority of the critical switching regulator pins are located on the outer bumps of the device, making it easier to lay out and connect to the external components. In general, make traces that handle large current as wide and short as possible. This consideration applies to the traces for PVINx, SWxA, SWxB, SWx, PGNDx, and VOUT6.

Make traces that handle switching currents as short as possible. These critical areas are PVINx, SW6B, VOUT6, and PGNDx. Reducing the trace length on these nodes helps mitigate noise coupling. For these connections, avoid using vias because they add parasitic inductance in the current path. If vias are required due to routing restrictions, place multiple vias in parallel.

For the buck regulators, the input capacitor has placement priority. Place the input capacitor as close as possible to the PVINx and PGNDx pins with wide trace connections. For Channel 6, the critical component connections are the input capacitor and the output capacitor. Connect these components as close as possible to the PVIN6, VOUT6, and PGND6 pins.

For all channels, keep the SWx pin to inductor connection as short as possible to minimize capacitive coupling. Because the SWx nodes carry high current, the traces must be wide enough to handle it.

THERMAL CONSIDERATIONS

The ADP5080 is a high efficiency power converter. However, in applications with heavy loads at high ambient temperature (T_A), the heat dissipated on the device may exceed the maximum junction temperature of 125°C. If the junction temperature (T_J) exceeds 165°C, the ADP5080 enters thermal shutdown (TSD), and all outputs are disabled. When the junction temperature falls below approximately 150°C, TSD is cleared. After a TSD event, the ADP5080 does not restart automatically, but must be reenabled with the EN pin.

The junction temperature can be calculated using Equation 6.

$$T_J = T_A + T_R \quad (6)$$

where T_R is the rise in junction temperature of the device due to power dissipation.

The rise in junction temperature is directly proportional to the power dissipation in the device, as shown in Equation 7.

$$T_R = PD_{LOSS} \times \theta_{JA} \quad (7)$$

where:
PD_{LOSS} is the power dissipation in the ADP5080.
θ_{JA} is the junction-to-ambient thermal resistance of the package mounted on a PCB.

The θ_{JA} value provided in Table 7 is for a JEDEC standard board. However, this value is only a benchmark and does not necessarily correlate to the thermal performance of a real-world PCB.

The thermal performance of the WLCSP package itself is given by the θ_{JB} value (see Table 7). This value is the thermal resistance from junction to solder ball and varies little with PCB design.

To determine the junction temperature, it is recommended that the ADP5080 case temperature be measured under worst-case conditions. The case temperature (T_C) is defined as the temperature on the top surface of the device and can be calculated using Equation 8.

$$T_C = T_A + PD_{LOSS} \times (\theta_{JA} - \theta_{JC}) \quad (8)$$

where:
θ_{JC} is the junction-to-case thermal resistance of the package, which is 0.2°C/W.

Because θ_{JC} is very low, it can be seen from Equation 9 that the measured value of T_C is a good approximation of T_J.

$$T_J = T_C + T_R = T_C + PD_{LOSS} \times \theta_{JC} \approx T_C \quad (9)$$

The estimated junction temperature or measured case temperature in worst-case conditions must be less than the maximum junction temperature of 125°C.

I²C INTERFACE

The ADP5080 includes an I²C-compatible serial interface to control the power management blocks and to read back system status. The I²C serial interface provides access to the internal registers of the ADP5080. For detailed information about the registers, see the Control Register Information section.

All registers programmed by the I²C interface are cleared and reset to their default values by a power-on reset (see the Power-On Reset (POR) section). The CHx_ON bits in the PCTRL register (Register 48) are cleared by a power-on reset or by taking the EN pin low.

The I²C interface operates at clock frequencies of up to 400 kHz. The ADP5080 does not respond to general calls. The ADP5080 accepts multiple masters, but if the device is in read mode, access is limited to one master until the data transmission is completed.

SDA AND SCL PINS

The ADP5080 has two dedicated I²C pins: SDA and SCL. SDA is an open-drain line for receiving and transmitting data. SCL is an input line for receiving the clock signal. These buses must be externally pulled up to the VDDIO supply.

Serial data is transferred by the SCL rising edge. The read data is generated at the SDA pin in read mode. If the V_{VDDIO} voltage level is below the undervoltage threshold (typically 950 mV), the EN signal goes low, and the SDA and SCL pins are left high-Z. The internal level shifter is disabled to prevent corrupt data from being received.

Note that the SCL pin must be pulled high to VDDIO during power-up so that the programmed fuse settings are properly loaded into the I²C registers at power-on reset (POR). This restriction does not apply as long as VDDIO is low. If VDDIO is supplied by VREG2, SCL must be high impedance until VREG2 rises above the POR threshold. If VDDIO is supplied by an external I²C host, either SCL must be held high or the VDDIO supply must be off until the VREG2 voltage rises above the POR threshold.

I²C ADDRESS

The 7-bit I²C chip address for the ADP5080 is 0x30 (011 0000); the subaddress is used to select one of the user registers, through which the I²C master communicates with the ADP5080.

SELF-CLEARING REGISTER BITS

Register 26 and Register 27 are status registers that contain self-clearing register bits. These bit are cleared automatically when a 1 is written to the status bit. Therefore, it is not necessary to write a 0 to the status bit to clear it.

I²C INTERFACE TIMING DIAGRAMS

Figure 57 is a timing diagram for the I²C write operation. Figure 58 and Figure 59 are timing diagrams for the I²C read operation. Register 48 (PCTRL register) has a special status flag in Bit 7 that indicates the presence of valid data in this register (see Figure 59). If Bit 7 = 0, the data is not yet valid, and the read operation must be repeated until the status bit changes to 1.

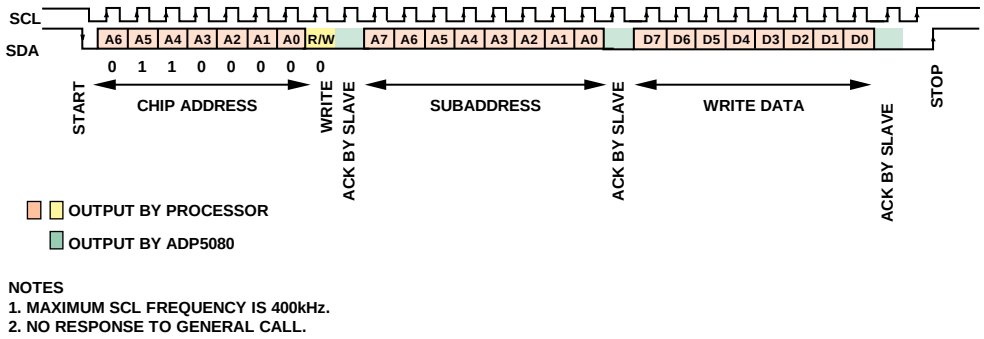

Figure 57. I²C Write to Registers

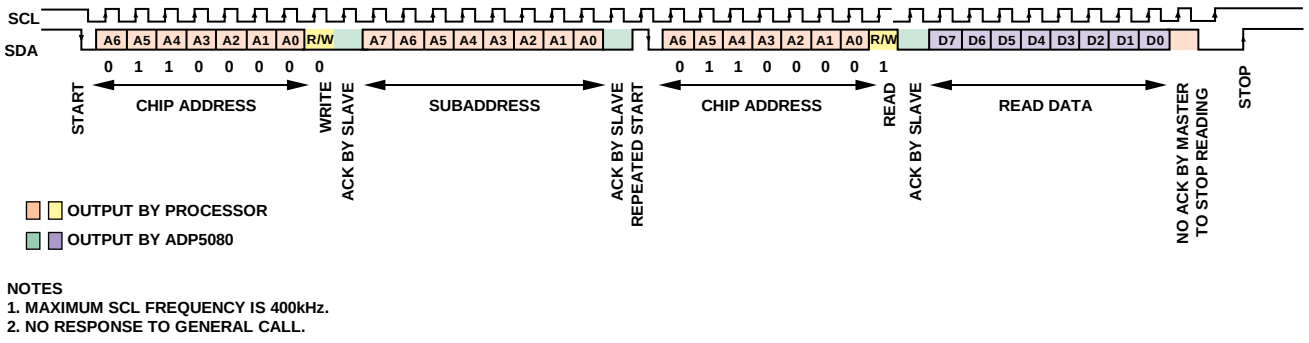

Figure 58. I²C Read from Registers with No Read Status Bit (All Registers Except PCTRL)

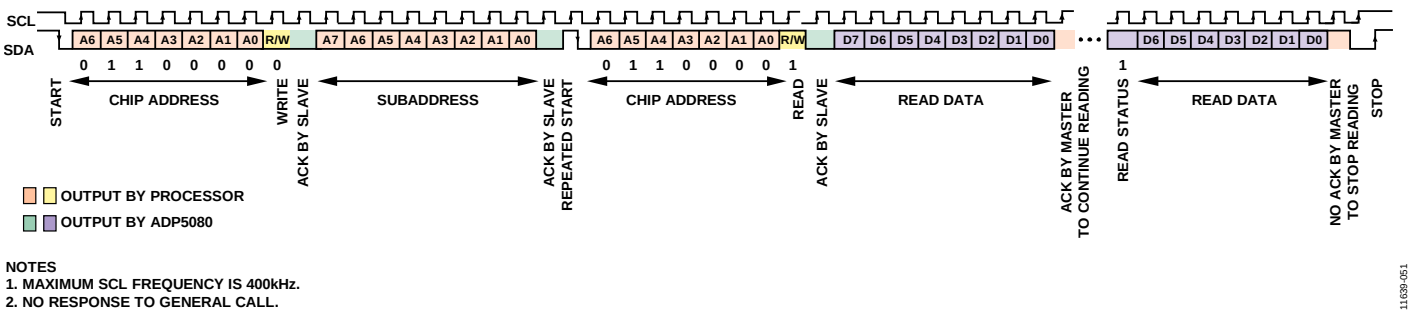

Figure 59. I²C Read from Register with Read Status Bit (PCTRL Register)

CONTROL REGISTER INFORMATION

CONTROL REGISTER MAP

Table 15 lists all control registers for the ADP5080. Any bits shown as blank are reserved.

Table 15. Control Register Map

Reg.	Register Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0x00	Reserved	Reserved							
1	0x01	DSCG		DSCG7_ON	DSCG6_ON	DSCG5_ON	DSCG4_ON	DSCG3_ON	DSCG2_ON	DSCG1_ON
2	0x02	SFTTIM1234	SS4[1:0]		SS3[1:0]		SS2[1:0]		SS1[1:0]	
3	0x03	SFTTIM567				SS7	SS6[1:0]		SS5[1:0]	
4	0x04	EN_DLY12		EN_DLY2[2:0]				EN_DLY1[2:0]		
5	0x05	EN_DLY34		EN_DLY4[2:0]				EN_DLY3[2:0]		
6	0x06	EN_DLY56		EN_DLY6[2:0]				EN_DLY5[2:0]		
7	0x07	EN_DLY7						EN_DLY7[2:0]		
8	0x08	DIS_DLY12		DIS_DLY2[2:0]				DIS_DLY1[2:0]		
9	0x09	DIS_DLY34		DIS_DLY4[2:0]				DIS_DLY3[2:0]		
10	0x0A	DIS_DLY56		DIS_DLY6[2:0]				DIS_DLY5[2:0]		
11	0x0B	DIS_DLY7						DIS_DLY7[2:0]		
12	0x0C	VID1				VID1[4:0]				
13	0x0D	VID23		VID3[2:0]			VID2[3:0]			
14	0x0E	VID45		VID5[2:0]				VID4[2:0]		
15	0x0F	VID6					VID6[3:0]			
16	0x10	VID7_LDO12		VID_LDO2[1:0]		VID_LDO1			VID7[1:0]	
17	0x11	DVS12			DVS2_INTVL	DVS1_INTVL			EN_DVS2	EN_DVS1
18	0x12	SEL_FREQ	SEL_FSW		FREQ6	FREQ5	FREQ4	FREQ3	FREQ2	FREQ1
19	0x13	SEL_FREQ_CP				EN_CLKO			FREQ_CP[1:0]	
20	0x14	SEL_PHASE			PHASE6	PHASE5	PHASE4	PHASE3	PHASE2	PHASE1
23	0x17	PROT_DLY			UV_DLY[1:0]				OV_DLY[1:0]	
24	0x18	PWRG	EN	PWRG7	PWRG6	PWRG5	PWRG4	PWRG3	PWRG2	PWRG1
25	0x19	MASK_PWRG		MASK_ PWRG7	MASK_ PWRG6	MASK_ PWRG5	MASK_ PWRG4	MASK_ PWRG3	MASK_ PWRG2	MASK_ PWRG1
26	0x1A	UVPST		UV7	UV6	UV5	UV4	UV3	UV2	UV1
27	0x1B	OVPST			OV6	OV5	OV4	OV3	OV2	OV1
28	0x1C	AUTO-PSM			AUTO-PSM6	AUTO-PSM5	AUTO-PSM4	AUTO-PSM3	AUTO-PSM2	AUTO-PSM1
29	0x1D	SEQ_MODE		MODE_EN7	MODE_EN6	MODE_EN5	MODE_EN4	MODE_EN3	MODE_EN2	MODE_EN1
30	0x1E	ADJ_BST_VTH6				BUCK6_ONLY			BOOST6_VTH[1:0]	
31	0x1F	OPT_SR_ADJ			ADJ_SR6	ADJ_SR5	ADJ_SR4	ADJ_SR3	ADJ_SR2	ADJ_SR1
32	0x20	DCM56_GSCAL1				DCM56				GATE_SCAL1
33	0x21	SEL_INP_LDO12				SEL_INP_ LDO2				SEL_INP_ LDO1
34	0x22	SEL_IND_UV5			UV_DLY5[1:0]					SEL_IND_ UV5
35	0x23	OPTION_SEL					REDUCE_ VOUT1	DIS_DLY_ EXTEND	DIS_EN34_ CH4	DIS_EN34_ CH3
48	0x30	PCTRL	RDST_PCTRL	CH7_ON	CH6_ON	CH5_ON	CH4_ON	CH3_ON	CH2_ON	CH1_ON

CONTROL REGISTER DETAILS

This section describes the bit functions of each register used by the ADP5080.

Register 1: DSCG (Discharge Switch Control), Address 0x01

Register 1 disables and enables the discharge switch for Channel 1 to Channel 7. The default values are defined by the fuse option.

Table 16. Register 1 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	DSCG7_ON	DSCG6_ON	DSCG5_ON	DSCG4_ON	DSCG3_ON	DSCG2_ON	DSCG1_ON

Table 17. DSCG Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
6	DSCG7_ON	R/W	0 = disable output discharge switch for Channel 7. 1 = enable output discharge switch for Channel 7.
5	DSCG6_ON	R/W	0 = disable output discharge switch for Channel 6. 1 = enable output discharge switch for Channel 6.
4	DSCG5_ON	R/W	0 = disable output discharge switch for Channel 5. 1 = enable output discharge switch for Channel 5.
3	DSCG4_ON	R/W	0 = disable output discharge switch for Channel 4. 1 = enable output discharge switch for Channel 4.
2	DSCG3_ON	R/W	0 = disable output discharge switch for Channel 3. 1 = enable output discharge switch for Channel 3.
1	DSCG2_ON	R/W	0 = disable output discharge switch for Channel 2. 1 = enable output discharge switch for Channel 2.
0	DSCG1_ON	R/W	0 = disable output discharge switch for Channel 1. 1 = enable output discharge switch for Channel 1.

Register 2: SFTTIM1234 (Soft Start Time for Channel 1, Channel 2, Channel 3, and Channel 4), Address 0x02

Register 2 sets the soft start time for Channel 1 to Channel 4. The default values are defined by the fuse option.

Table 18. Register 2 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SS4		SS3		SS2		SS1	

Table 19. SFTTIM1234 Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
[7:6]	SS4	R/W	Soft start time for Channel 4. 00 = 1 ms. 01 = 2 ms. 10 = 4 ms. 11 = 8 ms.
[5:4]	SS3	R/W	Soft start time for Channel 3. 00 = 1 ms. 01 = 2 ms. 10 = 4 ms. 11 = 8 ms.
[3:2]	SS2	R/W	Soft start time for Channel 2. 00 = 1 ms. 01 = 2 ms. 10 = 4 ms. 11 = 8 ms.
[1:0]	SS1	R/W	Soft start time for Channel 1. 00 = 1 ms. 01 = 2 ms. 10 = 4 ms. 11 = 8 ms.

Register 3: SFTTIM567 (Soft Start Time for Channel 5, Channel 6, and Channel 7), Address 0x03

Register 3 sets the soft start time for Channel 5 to Channel 7. The default values are defined by the fuse option.

Table 20. Register 3 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			SS7	SS6		SS5	

Table 21. SFTTIM567 Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
4	SS7	R/W	Soft start time for Channel 7. 0 = 2 ms. 1 = 4 ms.
[3:2]	SS6	R/W	Soft start time for Channel 6. 00 = 1 ms. 01 = 2 ms. 10 = 4 ms. 11 = 8 ms.
[1:0]	SS5	R/W	Soft start time for Channel 5. 00 = 1 ms. 01 = 2 ms. 10 = 4 ms. 11 = 8 ms.

Register 4: EN_DLY12 (Enable Delay Time for Channel 1 and Channel 2), Address 0x04

Register 4 sets the enable delay time for Channel 1 and Channel 2. The default values are defined by the fuse option.

Table 22. Register 4 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	EN_DLY2				EN_DLY1		

Table 23. EN_DLY12 Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
[6:4]	EN_DLY2	R/W	Enable delay time for Channel 2. 000 = 0 ms. 001 = 2 ms. 010 = 4 ms. 011 = 6 ms. 100 = 8 ms. 101 = 10 ms. 110 = 12 ms. 111 = 14 ms.
[2:0]	EN_DLY1	R/W	Enable delay time for Channel 1. 000 = 0 ms. 001 = 2 ms. 010 = 4 ms. 011 = 6 ms. 100 = 8 ms. 101 = 10 ms. 110 = 12 ms. 111 = 14 ms.

Register 5: EN_DLY34 (Enable Delay Time for Channel 3 and Channel 4), Address 0x05

Register 5 sets the enable delay time for Channel 3 and Channel 4. The default values are defined by the fuse option.

Table 24. Register 5 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	EN_DLY4				EN_DLY3		

Table 25. EN_DLY34 Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
[6:4]	EN_DLY4	R/W	Enable delay time for Channel 4. 000 = 0 ms. 001 = 2 ms. 010 = 4 ms. 011 = 6 ms. 100 = 8 ms. 101 = 10 ms. 110 = 12 ms. 111 = 14 ms.
[2:0]	EN_DLY3	R/W	Enable delay time for Channel 3. 000 = 0 ms. 001 = 2 ms. 010 = 4 ms. 011 = 6 ms. 100 = 8 ms. 101 = 10 ms. 110 = 12 ms. 111 = 14 ms.

Register 6: EN_DLY56 (Enable Delay Time for Channel 5 and Channel 6), Address 0x06

Register 6 sets the enable delay time for Channel 5 and Channel 6. The default values are defined by the fuse option.

Table 26. Register 6 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	EN_DLY6				EN_DLY5		

Table 27. EN_DLY56 Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
[6:4]	EN_DLY6	R/W	Enable delay time for Channel 6. 000 = 0 ms. 001 = 2 ms. 010 = 4 ms. 011 = 6 ms. 100 = 8 ms. 101 = 10 ms. 110 = 12 ms. 111 = 14 ms.
[2:0]	EN_DLY5	R/W	Enable delay time for Channel 5. 000 = 0 ms. 001 = 2 ms. 010 = 4 ms. 011 = 6 ms. 100 = 8 ms. 101 = 10 ms. 110 = 12 ms. 111 = 14 ms.

Register 7: EN_DLY7 (Enable Delay Time for Channel 7), Address 0x07

Register 7 sets the enable delay time for Channel 7. The default value is defined by the fuse option.

Table 28. Register 7 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
					EN_DLY7		

Table 29. EN_DLY7 Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
[2:0]	EN_DLY7	R/W	Enable delay time for Channel 7. 000 = 0 ms. 001 = 2 ms. 010 = 4 ms. 011 = 6 ms. 100 = 8 ms. 101 = 10 ms. 110 = 12 ms. 111 = 14 ms.

Register 8: DIS_DLY12 (Disable Delay Time for Channel 1 and Channel 2), Address 0x08

Register 8 sets the disable delay time for Channel 1 and Channel 2. The disable delay depends on the setting of the DIS_DLY_EXTEND bit in Register 35 (Bit 2 in Address 0x23). The default values are defined by the fuse option.

Table 30. Register 8 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	DIS_DLY2				DIS_DLY1		

Table 31. DIS_DLY12 Register, Bit Function Descriptions

Bits	Bit Name	R/W	Description		
[6:4]	DIS_DLY2	R/W	These bits set the disable delay time for Channel 2.		
			Bits[6:4]	**DIS_DLY_EXTEND = 0**	**DIS_DLY_EXTEND = 1**
			000	0 ms	0 ms
			001	4 ms	16 ms
			010	8 ms	32 ms
			011	12 ms	48 ms
			100	16 ms	64 ms
			101	20 ms	80 ms
			110	24 ms	96 ms
			111	28 ms	112 ms
[2:0]	DIS_DLY1	R/W	These bits set the disable delay time for Channel 1.		
			Bits[2:0]	**DIS_DLY_EXTEND = 0**	**DIS_DLY_EXTEND = 1**
			000	0 ms	0 ms
			001	4 ms	16 ms
			010	8 ms	32 ms
			011	12 ms	48 ms
			100	16 ms	64 ms
			101	20 ms	80 ms
			110	24 ms	96 ms
			111	28 ms	112 ms

Register 9: DIS_DLY34 (Disable Delay Time for Channel 3 and Channel 4), Address 0x09

Register 9 sets the disable delay time for Channel 3 and Channel 4. The disable delay depends on the setting of the DIS_DLY_EXTEND bit in Register 35 (Bit 2 in Address 0x23). The default values are defined by the fuse option.

Table 32. Register 9 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	DIS_DLY4				DIS_DLY3		

Table 33. DIS_DLY34 Register, Bit Function Descriptions

Bits	Bit Name	R/W	Description		
[6:4]	DIS_DLY4	R/W	These bits set the disable delay time for Channel 4.		
			Bits[6:4]	**DIS_DLY_EXTEND = 0**	**DIS_DLY_EXTEND = 1**
			000	0 ms	0 ms
			001	4 ms	16 ms
			010	8 ms	32 ms
			011	12 ms	48 ms
			100	16 ms	64 ms
			101	20 ms	80 ms
			110	24 ms	96 ms
			111	28 ms	112 ms
[2:0]	DIS_DLY3	R/W	These bits set the disable delay time for Channel 3.		
			Bits[2:0]	**DIS_DLY_EXTEND = 0**	**DIS_DLY_EXTEND = 1**
			000	0 ms	0 ms
			001	4 ms	16 ms
			010	8 ms	32 ms
			011	12 ms	48 ms
			100	16 ms	64 ms
			101	20 ms	80 ms
			110	24 ms	96 ms
			111	28 ms	112 ms

Register 10: DIS_DLY56 (Disable Delay Time for Channel 5 and Channel 6), Address 0x0A

Register 10 sets the disable delay time for Channel 5 and Channel 6. The disable delay depends on the setting of the DIS_DLY_EXTEND bit in Register 35 (Bit 2 in Address 0x23). The default values are defined by the fuse option.

Table 34. Register 10 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	DIS_DLY6				DIS_DLY5		

Table 35. DIS_DLY56 Register, Bit Function Descriptions

Bits	Bit Name	R/W	Description		
[6:4]	DIS_DLY6	R/W	These bits set the disable delay time for Channel 6.		
			Bits[6:4]	**DIS_DLY_EXTEND = 0**	**DIS_DLY_EXTEND = 1**
			000	0 ms	0 ms
			001	4 ms	16 ms
			010	8 ms	32 ms
			011	12 ms	48 ms
			100	16 ms	64 ms
			101	20 ms	80 ms
			110	24 ms	96 ms
			111	28 ms	112 ms
[2:0]	DIS_DLY5	R/W	These bits set the disable delay time for Channel 5.		
			Bits[2:0]	**DIS_DLY_EXTEND = 0**	**DIS_DLY_EXTEND = 1**
			000	0 ms	0 ms
			001	4 ms	16 ms
			010	8 ms	32 ms
			011	12 ms	48 ms
			100	16 ms	64 ms
			101	20 ms	80 ms
			110	24 ms	96 ms
			111	28 ms	112 ms

Register 11: DIS_DLY7 (Disable Delay Time for Channel 7), Address 0x0B

Register 11 sets the disable delay time for Channel 7. The disable delay depends on the setting of the DIS_DLY_EXTEND bit in Register 35 (Bit 2 in Address 0x23). The default value is defined by the fuse option.

Table 36. Register 11 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
					DIS_DLY7		

Table 37. DIS_DLY7 Register, Bit Function Descriptions

Bits	Bit Name	R/W	Description		
[2:0]	DIS_DLY7	R/W	These bits set the disable delay time for Channel 7.		
			Bits[2:0]	**DIS_DLY_EXTEND = 0**	**DIS_DLY_EXTEND = 1**
			000	0 ms	0 ms
			001	4 ms	16 ms
			010	8 ms	32 ms
			011	12 ms	48 ms
			100	16 ms	64 ms
			101	20 ms	80 ms
			110	24 ms	96 ms
			111	28 ms	112 ms

Register 12: VID1 (Output Voltage for Channel 1), Address 0x0C

Register 12 sets the output voltage for Channel 1. The output voltage depends on the setting of the REDUCE_VOUT1 bit in Register 35 (Bit 3 in Address 0x23). The default value is defined by the fuse option.

Table 38. Register 12 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			VID1				

Table 39. VID1 Register, Bit Function Descriptions

Bits	Bit Name	R/W	Description		
[4:0]	VID1	R/W	These bits set the output voltage for Channel 1.		
			Bits[4:0]	**REDUCE_VOUT1 = 0**	**REDUCE_VOUT1 = 1**
			00000	1.20 V	1.11 V
			00001	1.19 V	1.10 V
			00010	1.18 V	1.09 V
			00011	1.17 V	1.08 V
			00100	1.16 V	1.07 V
			00101	1.15 V	1.06 V
			00110	1.14 V	1.05 V
			00111	1.13 V	1.04 V
			01000	1.12 V	1.03 V
			01001	1.11 V	1.02 V
			01010	1.10 V	1.01 V
			01011	1.09 V	1.00 V
			01100	1.08 V	0.99 V
			01101	1.07 V	0.98 V
			01110	1.06 V	0.97 V
			01111	1.05 V	0.96 V
			10000	1.04 V	0.95 V
			10001	1.03 V	0.94 V
			10010	1.02 V	0.93 V
			10011	1.01 V	0.92 V
			10100	1.00 V	0.91 V
			10101	0.99 V	0.90 V
			10110	0.98 V	0.89 V
			10111	0.97 V	0.88 V
			11000	0.96 V	0.87 V
			11001	0.95 V	0.86 V
			11010	0.94 V	0.85 V
			11011	0.93 V	0.84 V
			11100	0.92 V	0.83 V
			11101	0.91 V	0.82 V
			11110	0.90 V	0.81 V
			11111	0.89 V	0.80 V

Register 13: VID23 (Output Voltage for Channel 2 and Channel 3), Address 0x0D

Register 13 sets the output voltage for Channel 2 and Channel 3. The default values are defined by the fuse option.

Table 40. Register 13 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	VID3			VID2			

Table 41. VID23 Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
[6:4]	VID3	R/W	These bits set the output voltage for Channel 3. 000 = 1.8 V. 001 = 1.5 V. 010 = 1.35 V. 011 = 1.3 V. 100 = 1.25 V. 101 = 1.225 V. 110 = 1.2 V. 111 = adjustable mode.
[3:0]	VID2	R/W	These bits set the output voltage for Channel 2. 0000 = 3.3 V. 0001 = 3.2 V. 0010 = 3.15 V. 0011 = 3.00 V. 0100 = 1.8 V. 0101 = 1.25 V. 0110 = 1.225 V. 0111 = 1.2 V. 1000 = 1.175 V. 1001 = 1.15 V. 1010 = 1.125 V. 1011 = 1.1 V. 1100 = 1.075 V. 1101 = 1.05 V. 1110 = 1.025 V. 1111 = 1.0 V.

Register 14: VID45 (Output Voltage for Channel 4 and Channel 5), Address 0x0E

Register 14 sets the output voltage for Channel 4 and Channel 5. The default values are defined by the fuse option.

Table 42. Register 14 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	VID5				VID4		

Table 43. VID45 Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
[6:4]	VID5	R/W	These bits set the output voltage for Channel 5. 000 = 5.00 V. 001 = 4.30 V. 010 = 4.25 V. 011 = 3.30 V. 100 = 3.20 V. 101 = 3.15 V. 110 = 3.10 V. 111 = 3.00 V.
[2:0]	VID4	R/W	These bits set the output voltage for Channel 4. 000 = 3.55 V. 001 = 3.30 V. 010 = 3.20 V. 011 = 3.15 V. 100 = 3.10 V. 101 = 2.80 V. 110 = 1.80 V. 111 = adjustable mode.

Register 15: VID6 (Output Voltage for Channel 6), Address 0x0F

Register 15 sets the output voltage for Channel 6. The default value is defined by the fuse option.

Table 44. Register 15 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				VID6			

Table 45. VID6 Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
[3:0]	VID6	R/W	These bits set the output voltage for Channel 6. 0000 = 5.5 V. 0001 = 5.4 V. 0010 = 5.3 V. 0011 = 5.2 V. 0100 = 5.15 V. 0101 = 5.1 V. 0110 = 5.0 V. 0111 = 4.9 V. 1000 = 4.8 V. 1001 = 4.7 V. 1010 = 4.6 V. 1011 = 4.5 V. 1100 = 4.4 V. 1101 = 3.8 V. 1110 = 3.5 V. 1111 = adjustable mode.

Register 16: VID7_LDO12 (Output Voltage for Channel 7, LDO1, and LDO2), Address 0x10

Register 16 sets the output voltage for Channel 7, LDO1, and LDO2. The default values are defined by the fuse option.

Table 46. Register 16 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	VID_LDO2		VID_LDO1			VID7	

Table 47. VID7_LDO12 Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
[6:5]	VID_LDO2	R/W	These bits set the output voltage for LDO2. 00 = 3.3 V. 01 = 3.2 V. 10 = 3.15 V. 11 = 3.0 V.
4	VID_LDO1	R/W	These bits set the output voltage for LDO1. 0 = 5.5 V. 1 = 5.0 V.
[1:0]	VID7	R/W	These bits set the output voltage for Channel 7. 00 = 12 V. 01 = 9 V. 10 = 6 V. 11 = 5 V.

Register 17: DVS12 (DVS Control for Channel 1 and Channel 2), Address 0x11

Register 17 configures the dynamic voltage scaling (DVS) function for Channel 1 and Channel 2. For more information, see the Dynamic Voltage Scaling (DVS) Function section.

Table 48. Register 17 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		DVS2_INTVAL	DVS1_INTVAL			EN_DVS2	EN_DVS1

Table 49. DVS12 Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
5	DVS2_INTVAL	R/W	This bit configures the DVS interval for Channel 2. 0 = 32 µs (default). 1 = 64 µs.
4	DVS1_INTVAL	R/W	This bit configures the DVS interval for Channel 1. 0 = 16 µs (default). 1 = 32 µs.
1	EN_DVS2	R/W	This bit enables or disables the DVS function for Channel 2. 0 = disable DVS function for Channel 2 (default). 1 = enable DVS function for Channel 2.
0	EN_DVS1	R/W	This bit enables or disables the DVS function for Channel 1. 0 = disable DVS function for Channel 1 (default). 1 = enable DVS function for Channel 1.

Register 18: SEL_FREQ (Switching Frequency for Channel 1 to Channel 6), Address 0x12

Register 18 sets the master switching frequency (f_{SW}) and the switching frequency for each channel. The default values are defined by the fuse option.

Table 50. Register 18 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SEL_FSW		FREQ6	FREQ5	FREQ4	FREQ3	FREQ2	FREQ1

Table 51. SEL_FREQ Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
7	SEL_FSW	R/W	This bit selects the master switching frequency (f_{SW}). 0 = f_{SW} is 2 MHz. 1 = f_{SW} is 1.5 MHz.
5	FREQ6	R/W	This bit sets the switching frequency for Channel 6. 0 = 1 × f_{SW}. 1 = 1/2 × f_{SW}.
4	FREQ5	R/W	This bit sets the switching frequency for Channel 5. 0 = 1 × f_{SW}. 1 = 1/2 × f_{SW}.
3	FREQ4	R/W	This bit sets the switching frequency for Channel 4. 0 = 1 × f_{SW}. 1 = 1/2 × f_{SW}.
2	FREQ3	R/W	This bit sets the switching frequency for Channel 3. 0 = 1 × f_{SW}. 1 = 1/2 × f_{SW}.
1	FREQ2	R/W	This bit sets the switching frequency for Channel 2. 0 = 1 × f_{SW}. 1 = 1/2 × f_{SW}.
0	FREQ1	R/W	This bit sets the switching frequency for Channel 1. 0 = 1 × f_{SW}. 1 = 1/2 × f_{SW}.

Register 19: SEL_FREQ_CP (Charge Pump Frequency), Address 0x13

Register 19 sets the switching frequency for the charge pump and configures the CLKO output. The switching frequency for the charge pump depends on whether the device is synchronized to the internal clock or to an external clock. The default values are defined by the fuse option.

Table 52. Register 19 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			EN_CLKO			FREQ_CP	

Table 53. SEL_FREQ_CP Register, Bit Function Descriptions

Bits	Bit Name	Access	Description		
4	EN_CLKO	R/W	This bit configures the clock output (CLKO) pin. The CLKO pin can output the internal switching clock used for Channel 1 when the device is configured to use the internal oscillator. 0 = no output from CLKO pin. 1 = output from CLKO pin.		
[1:0]	FREQ_CP	R/W	These bits set the charge pump switching frequency.		
			Bits[1:0]	**Internal Clock**	**External Clock**
			00	1/2 × f_{SW}	1/4 × f_{SW}
			01	1/4 × f_{SW}	1/8 × f_{SW}
			10	1/8 × f_{SW}	1/4 × f_{SW}
			11	1/16 × f_{SW}	1/8 × f_{SW}

Register 20: SEL_PHASE (Switching Phase for Channel 1 to Channel 6), Address 0x14

Register 20 is used to reverse the phase of the switching clock to spread switching energy over time. The default values for Channel 2 to Channel 6 are defined by the fuse option.

Table 54. Register 20 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		PHASE6	PHASE5	PHASE4	PHASE3	PHASE2	PHASE1

Table 55. SEL_PHASE Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
5	PHASE6	R/W	This bit sets the phase for Channel 6. 0 = switching pulse in phase. 1 = switching pulse reversed.
4	PHASE5	R/W	This bit sets the phase for Channel 5. 0 = switching pulse in phase. 1 = switching pulse reversed.
3	PHASE4	R/W	This bit sets the phase for Channel 4. 0 = switching pulse in phase. 1 = switching pulse reversed.
2	PHASE3	R/W	This bit sets the phase for Channel 3. 0 = switching pulse in phase. 1 = switching pulse reversed.
1	PHASE2	R/W	This bit sets the phase for Channel 2. 0 = switching pulse in phase. 1 = switching pulse reversed.
0	PHASE1	R/W	This bit sets the phase for Channel 1. 0 = switching pulse in phase (default). 1 = switching pulse reversed.

Register 23: PROT_DLY (Undervoltage/Overvoltage Protection Delay Times), Address 0x17

Register 23 sets the delay times to start undervoltage and overvoltage protection. The default values are defined by the fuse option.

Table 56. Register 23 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		UV_DLY				OV_DLY	

Table 57. PROT_DLY Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
[5:4]	UV_DLY	R/W	Undervoltage protection delay time. 00 = 0 ms. 01 = 21 ms. 10 = 45 ms. 11 = disable undervoltage protection.
[1:0]	OV_DLY	R/W	Overvoltage protection delay time. 00 = 0 ms. 01 = 1.3 ms. 10 = 3.4 ms. 11 = disable overvoltage protection.

Register 24: PWRG (Power-Good Status), Address 0x18

Register 24 is the read-only register for the power-good status of Channel 1 to Channel 7. A value of 1 for any PWRGx bit indicates that the power for that channel is good. The EN signal logic level can be monitored using Bit 7 of this register.

Table 58. Register 24 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EN	PWRG7	PWRG6	PWRG5	PWRG4	PWRG3	PWRG2	PWRG1

Table 59. PWRG Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
7	EN	R	This bit displays the state of the EN pin. 0 = EN pin low (default). 1 = EN pin high.
6	PWRG7	R	This bit displays the power-good status of Channel 7. 0 = power-good status low (default). 1 = power-good status high.
5	PWRG6	R	This bit displays the power-good status of Channel 6. 0 = power-good status low (default). 1 = power-good status high.
4	PWRG5	R	This bit displays the power-good status of Channel 5. 0 = power-good status low (default). 1 = power-good status high.
3	PWRG4	R	This bit displays the power-good status of Channel 4. 0 = power-good status low (default). 1 = power-good status high.
2	PWRG3	R	This bit displays the power-good status of Channel 3. 0 = power-good status low (default). 1 = power-good status high.
1	PWRG2	R	This bit displays the power-good status of Channel 2. 0 = power-good status low (default). 1 = power-good status high.
0	PWRG1	R	This bit displays the power-good status of Channel 1. 0 = power-good status low (default). 1 = power-good status high.

Register 25: MASK_PWRG (Power-Good Masked Channels), Address 0x19

Register 25 masks and unmasks the power-good status for Channel 1 to Channel 7. The default values are defined by the fuse option.

Table 60. Register 25 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	MASK_PWRG7	MASK_PWRG6	MASK_PWRG5	MASK_PWRG4	MASK_PWRG3	MASK_PWRG2	MASK_PWRG1

Table 61. MASK_PWRG Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
6	MASK_PWRG7	R/W	This bit masks or unmasks the power-good status of Channel 7. 0 = output power-good status of Channel 7 to the $\overline{\text{FAULT}}$ pin. 1 = mask power-good status of Channel 7.
5	MASK_PWRG6	R/W	This bit masks or unmasks the power-good status of Channel 6. 0 = output power-good status of Channel 6 to the $\overline{\text{FAULT}}$ pin. 1 = mask power-good status of Channel 6.
4	MASK_PWRG5	R/W	This bit masks or unmasks the power-good status of Channel 5. 0 = output power-good status of Channel 5 to the $\overline{\text{FAULT}}$ pin. 1 = mask power-good status of Channel 5.
3	MASK_PWRG4	R/W	This bit masks or unmasks the power-good status of Channel 4. 0 = output power-good status of Channel 4 to the $\overline{\text{FAULT}}$ pin. 1 = mask power-good status of Channel 4.
2	MASK_PWRG3	R/W	This bit masks or unmasks the power-good status of Channel 3. 0 = output power-good status of Channel 3 to the $\overline{\text{FAULT}}$ pin. 1 = mask power-good status of Channel 3.
1	MASK_PWRG2	R/W	This bit masks or unmasks the power-good status of Channel 2. 0 = output power-good status of Channel 2 to the $\overline{\text{FAULT}}$ pin. 1 = mask power-good status of Channel 2.
0	MASK_PWRG1	R/W	This bit masks or unmasks the power-good status of Channel 1. 0 = output power-good status of Channel 1 to the $\overline{\text{FAULT}}$ pin. 1 = mask power-good status of Channel 1.

Register 26: UVPST (Undervoltage Protection Status), Address 0x1A

Register 26 indicates the status of the undervoltage protection on Channel 1 to Channel 7. To clear any bit in this register, write a 1 to the bit.

Table 62. Register 26 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	UV7	UV6	UV5	UV4	UV3	UV2	UV1

Table 63. UVPST Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
6	UV7	Read/ self-clear	0 = no undervoltage condition detected on Channel 7 (default). 1 = undervoltage condition detected on Channel 7.
5	UV6	Read/ self-clear	0 = no undervoltage condition detected on Channel 6 (default). 1 = undervoltage condition detected on Channel 6.
4	UV5	Read/ self-clear	0 = no undervoltage condition detected on Channel 5 (default). 1 = undervoltage condition detected on Channel 5.
3	UV4	Read/ self-clear	0 = no undervoltage condition detected on Channel 4 (default). 1 = undervoltage condition detected on Channel 4.
2	UV3	Read/ self-clear	0 = no undervoltage condition detected on Channel 3 (default). 1 = undervoltage condition detected on Channel 3.
1	UV2	Read/ self-clear	0 = no undervoltage condition detected on Channel 2 (default). 1 = undervoltage condition detected on Channel 2.
0	UV1	Read/ self-clear	0 = no undervoltage condition detected on Channel 1 (default). 1 = undervoltage condition detected on Channel 1.

Register 27: OVPST (Overvoltage Protection Status), Address 0x1B

Register 27 indicates the status of the overvoltage protection on Channel 1 to Channel 6. To clear any bit in this register, write a 1 to the bit.

Table 64. Register 27 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		OV6	OV5	OV4	OV3	OV2	OV1

Table 65. OVPST Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
5	OV6	Read/ self-clear	0 = no overvoltage condition detected on Channel 6 (default). 1 = overvoltage condition detected on Channel 6.
4	OV5	Read/ self-clear	0 = no overvoltage condition detected on Channel 5 (default). 1 = overvoltage condition detected on Channel 5.
3	OV4	Read/ self-clear	0 = no overvoltage condition detected on Channel 4 (default). 1 = overvoltage condition detected on Channel 4.
2	OV3	Read/ self-clear	0 = no overvoltage condition detected on Channel 3 (default). 1 = overvoltage condition detected on Channel 3.
1	OV2	Read/ self-clear	0 = no overvoltage condition detected on Channel 2 (default). 1 = overvoltage condition detected on Channel 2.
0	OV1	Read/ self-clear	0 = no overvoltage condition detected on Channel 1 (default). 1 = overvoltage condition detected on Channel 1.

Register 28: AUTO-PSM (Auto PSM or Forced PWM Mode for Channel 1 to Channel 6), Address 0x1C

Register 28 configures Channel 1 to Channel 6 for either forced PWM operation or automatic PWM/PSM operation. The default values are defined by the fuse option.

Table 66. Register 28 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		AUTO-PSM6	AUTO-PSM5	AUTO-PSM4	AUTO-PSM3	AUTO-PSM2	AUTO-PSM1

Table 67. AUTO-PSM Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
5	AUTO-PSM6	R/W	0 = enable forced PWM mode for Channel 6. 1 = enable automatic PWM/PSM mode for Channel 6.
4	AUTO-PSM5	R/W	0 = enable forced PWM mode for Channel 5. 1 = enable automatic PWM/PSM mode for Channel 5.
3	AUTO-PSM4	R/W	0 = enable forced PWM mode for Channel 4. 1 = enable automatic PWM/PSM mode for Channel 4.
2	AUTO-PSM3	R/W	0 = enable forced PWM mode for Channel 3. 1 = enable automatic PWM/PSM mode for Channel 3.
1	AUTO-PSM2	R/W	0 = enable forced PWM mode for Channel 2. 1 = enable automatic PWM/PSM mode for Channel 2.
0	AUTO-PSM1	R/W	0 = enable forced PWM mode for Channel 1. 1 = enable automatic PWM/PSM mode for Channel 1.

Register 29: SEQ_MODE (Sequencer Mode), Address 0x1D

Register 29 selects the power-up/power-down control mode for Channel 1 to Channel 7: I²C control (manual) mode or sequencer mode (for more information, see the Enabling and Disabling the Output Channels section). The default values are defined by the fuse option.

Table 68. Register 29 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	MODE_EN7	MODE_EN6	MODE_EN5	MODE_EN4	MODE_EN3	MODE_EN2	MODE_EN1

Table 69. SEQ_MODE Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
6	MODE_EN7	R/W	This bit sets the power-up/power-down control mode for Channel 7. 0 = I²C control mode. 1 = sequencer mode.
5	MODE_EN6	R/W	This bit sets the power-up/power-down control mode for Channel 6. 0 = I²C control mode. 1 = sequencer mode.
4	MODE_EN5	R/W	This bit sets the power-up/power-down control mode for Channel 5. 0 = I²C control mode. 1 = sequencer mode.
3	MODE_EN4	R/W	This bit sets the power-up/power-down control mode for Channel 4. 0 = I²C control mode. 1 = sequencer mode.
2	MODE_EN3	R/W	This bit sets the power-up/power-down control mode for Channel 3. 0 = I²C control mode. 1 = sequencer mode.
1	MODE_EN2	R/W	This bit sets the power-up/power-down control mode for Channel 2. 0 = I²C control mode. 1 = sequencer mode.
0	MODE_EN1	R/W	This bit sets the power-up/power-down control mode for Channel 1. 0 = I²C control mode. 1 = sequencer mode.

Register 30: ADJ_BST_VTH6 (Adjust Boost Kick-In Threshold and Regulation Mode for Channel 6), Address 0x1E

Register 30 sets the regulation mode for Channel 6 (buck boost or buck only) and adjusts the threshold of the boost regulator kick-in point when Channel 6 is configured for buck boost regulation mode (for more information, see the Channel 6: Buck or Buck Boost Regulator section). The default values are defined by the fuse option.

Table 70. Register 30 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			BUCK6_ONLY			BOOST6_VTH	

Table 71. ADJ_BST_VTH6 Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
4	BUCK6_ONLY	R/W	This bit sets the regulation mode for Channel 6. 0 = buck boost mode. 1 = buck regulation only mode.
[1:0]	BOOST6_VTH	R/W	These bits set the input threshold voltage for the boost FETs. 00 = VOUT6/0.82. 01 = VOUT6/0.79. 10 = VOUT6/0.77. 11 = VOUT6/0.85.

Register 31: OPT_SR_ADJ (Slew Rate Adjustment for Channel 1 to Channel 6), Address 0x1F

Register 31 slows the switching slew rate of the specified channel, which reduces high frequency switching noise. The default value is 0 for all channels.

Table 72. Register 31 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		ADJ_SR6	ADJ_SR5	ADJ_SR4	ADJ_SR3	ADJ_SR2	ADJ_SR1

Table 73. OPT_SR_ADJ Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
5	ADJ_SR6	R/W	This bit sets the slew rate for Channel 6. 0 = normal slew rate (default). 1 = reduced slew rate.
4	ADJ_SR5	R/W	This bit sets the slew rate for Channel 5. 0 = normal slew rate (default). 1 = reduced slew rate.
3	ADJ_SR4	R/W	This bit sets the slew rate for Channel 4. 0 = normal slew rate (default). 1 = reduced slew rate.
2	ADJ_SR3	R/W	This bit sets the slew rate for Channel 3. 0 = normal slew rate (default). 1 = reduced slew rate.
1	ADJ_SR2	R/W	This bit sets the slew rate for Channel 2. 0 = normal slew rate (default). 1 = reduced slew rate.
0	ADJ_SR1	R/W	This bit sets the slew rate for Channel 1. 0 = normal slew rate (default). 1 = reduced slew rate.

Register 32: DCM56_GSCAL1 (Auto DCM for Channel 5 and Channel 6, Gate Scaling for Channel 1), Address 0x20

Register 32 is used to enable or disable automatic DCM mode on Channel 5 and Channel 6. Register 32 is also used to set the gate size for Channel 1: either full or half size (for more information, see the Gate Scaling (Channel 1 Only) section). The default values are defined by the fuse option.

Table 74. Register 32 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			DCM56				GATE_SCAL1

Table 75. DCM56_GSCAL1 Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
4	DCM56	R/W	This bit sets the operational mode for Channel 5 and Channel 6. This bit can be set to 1 only when the AUTO-PSM6 and AUTO-PSM5 bits in Register 28 are set to 1. 0 = enable automatic PWM/PSM operation for Channel 5 and Channel 6. 1 = enable automatic DCM operation for Channel 5 and Channel 6.
0	GATE_SCAL1	R/W	This bit enables or disables the gate scaling function for Channel 1. 0 = disable gate scaling on Channel 1. 1 = enable gate scaling on Channel 1 (gate size is halved).

Register 33: SEL_INP_LDO12 (Input Selection for LDO1 and LDO2), Address 0x21

Register 33 is used to set the input path for LDO1 and LDO2. The default values are defined by the fuse option.

Table 76. Register 33 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			SEL_INP_LDO2				SEL_INP_LDO1

Table 77. SEL_INP_LDO12 Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
4	SEL_INP_LDO2	R/W	This bit sets the input path for LDO2. 0 = VREG1. 1 = VISW2.
0	SEL_INP_LDO1	R/W	This bit sets the input path for LDO1. 0 = VBATT. 1 = VISW1.

Register 34: SEL_IND_UV5 (Independent UVP Control for Channel 5), Address 0x22

Register 34 configures independent UVP control for Channel 5. When Bit 0 is set to 1, UVP control on Channel 5 operates independently of UVP control on the other channels, and the UV_DLY5 bits can be used to set a delay time separate from the UV_DLY setting in Register 23. The default values are defined by the fuse option.

Table 78. Register 34 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		UV_DLY5					SEL_IND_UV5

Table 79. SEL_IND_UV5 Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
[5:4]	UV_DLY5	R/W	Undervoltage protection delay time for Channel 5. These bits are valid only when SEL_IND_UV5 = 1. 00 = 0 ms. 01 = 21 ms. 10 = 45 ms. 11 = disable standalone undervoltage protection on Channel 5.
0	SEL_IND_UV5	R/W	This bit enables or disables standalone UVP control for Channel 5. 0 = UVP control for Channel 5 synchronized with UVP control of other channels. 1 = standalone UVP control for Channel 5.

Register 35: OPTION_SEL (Channel 1 Output Voltage Reduction, Disable Delay Time Increase, EN34 Function), Address 0x23

Register 35 is used to set the following options: Channel 1 output voltage range, global disable delay time range, and independent enable function for Channel 3 and Channel 4 via the EN34 pin. The default values are defined by the fuse option.

Table 80. Register 35 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				REDUCE_VOUT1	DIS_DLY_EXTEND	DIS_EN34_CH4	DIS_EN34_CH3

Table 81. OPTION_SEL Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
3	REDUCE_VOUT1	R/W	This bit sets the output voltage range for Channel 1 (see Table 39). 0 = normal output range. 1 = reduced output range.
2	DIS_DLY_EXTEND	R/W	This bit sets the disable delay time (see Table 31, Table 33, Table 35, and Table 37). 0 = normal disable delay time. 1 = extended disable delay time (4× the normal time).
1	DIS_EN34_CH4	R/W	This bit specifies whether the EN34 pin controls the enabling and disabling of Channel 4. 0 = EN34 pin controls Channel 4. 1 = EN34 pin does not control Channel 4.
0	DIS_EN34_CH3	R/W	This bit specifies whether the EN34 pin controls the enabling and disabling of Channel 3. 0 = EN34 pin controls Channel 3. 1 = EN34 pin does not control Channel 3.

Register 48: PCTRL (Channel Enable Control), Address 0x30

Register 48 enables and disables the operation of individual channels (Channel 1 to Channel 7). This register is reset when the EN pin is taken low or when an internal power-on reset occurs. All channels that are not configured for sequencer mode in Register 29 (Address 0x1D) can be manually turned on and off using the CHx_ON bits in the PCTRL register. Writing 1 to the CHx_ON bit takes effect only when the EN pin is logic high. When the EN pin is logic low, all channels configured for manual mode turn off immediately, and the appropriate CHx_ON bits are reset. When the EN pin is low, any data written to or read from the PCTRL register is not valid.

Table 82. Register 48 Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RDST_PCTRL	CH7_ON	CH6_ON	CH5_ON	CH4_ON	CH3_ON	CH2_ON	CH1_ON

Table 83. PCTRL Register, Bit Function Descriptions

Bits	Bit Name	Access	Description
7	RDST_PCTRL	R	This bit indicates whether data is valid. Repeat the read operation until this bit changes to 1. At least two read operations are required before this bit changes to 1. 0 = data is not yet valid. 1 = data is valid.
6	CH7_ON	R/W	This bit enables or disables Channel 7. 0 = disable Channel 7 (default). 1 = enable Channel 7.
5	CH6_ON	R/W	This bit enables or disables Channel 6. 0 = disable Channel 6 (default). 1 = enable Channel 6.
4	CH5_ON	R/W	This bit enables or disables Channel 5. 0 = disable Channel 5 (default). 1 = enable Channel 5.
3	CH4_ON	R/W	This bit enables or disables Channel 4. This bit may be masked if the DIS_EN34_CH4 bit in Register 35 is set to 0. 0 = disable Channel 4 (default). 1 = enable Channel 4.
2	CH3_ON	R/W	This bit enables or disables Channel 3. This bit may be masked if the DIS_EN34_CH3 bit in Register 35 is set to 0. 0 = disable Channel 3 (default). 1 = enable Channel 3.
1	CH2_ON	R/W	This bit enables or disables Channel 2. 0 = disable Channel 2 (default). 1 = enable Channel 2.
0	CH1_ON	R/W	This bit enables or disables Channel 1. 0 = disable Channel 1 (default). 1 = enable Channel 1.

FACTORY DEFAULT OPTIONS

Table 84 lists the factory default options programmed into the ADP5080 when the device is ordered (see the Ordering Guide). To order the device with options other than the default options, contact your local Analog Devices sales or distribution representative. For information about all available configuration options, see the Control Register Details section.

Table 84. Factory Default Fuse Option Settings

Register	Register Addr (Hex)	Register Name	Bit	Bit Name	Default Setting	Binary Code	Description
1	0x01	DSCG	6	DSCG7_ON	On	1	Channel 7 output discharge
			5	DSCG6_ON	On	1	Channel 6 output discharge
			4	DSCG5_ON	On	1	Channel 5 output discharge
			3	DSCG4_ON	On	1	Channel 4 output discharge
			2	DSCG3_ON	On	1	Channel 3 output discharge
			1	DSCG2_ON	On	1	Channel 2 output discharge
			0	DSCG1_ON	On	1	Channel 1 output discharge
2	0x02	SFTTIM1234	[7:6]	SS4	8 ms	11	Channel 4 soft start time
			[5:4]	SS3	1 ms	00	Channel 3 soft start time
			[3:2]	SS2	1 ms	00	Channel 2 soft start time
			[1:0]	SS1	1 ms	00	Channel 1 soft start time
3	0x03	SFTTIM567	4	SS7	2 ms	0	Channel 7 soft start time
			[3:2]	SS6	2 ms	01	Channel 6 soft start time
			[1:0]	SS5	8 ms	11	Channel 5 soft start time
4	0x04	EN_DLY12	[6:4]	EN_DLY2	2 ms	001	Channel 2 enable delay time
			[2:0]	EN_DLY1	0 ms	000	Channel 1 enable delay time
5	0x05	EN_DLY34	[6:4]	EN_DLY4	0 ms	000	Channel 4 enable delay time
			[2:0]	EN_DLY3	0 ms	000	Channel 3 enable delay time
6	0x06	EN_DLY56	[6:4]	EN_DLY6	4 ms	010	Channel 6 enable delay time
			[2:0]	EN_DLY5	4 ms	010	Channel 5 enable delay time
7	0x07	EN_DLY7	[2:0]	EN_DLY7	6 ms	011	Channel 7 enable delay time
8	0x08	DIS_DLY12	[6:4]	DIS_DLY2	0 ms	000	Channel 2 disable delay time
			[2:0]	DIS_DLY1	12 ms	011	Channel 1 disable delay time
9	0x09	DIS_DLY34	[6:4]	DIS_DLY4	0 ms	000	Channel 4 disable delay time
			[2:0]	DIS_DLY3	0 ms	000	Channel 3 disable delay time
10	0x0A	DIS_DLY56	[6:4]	DIS_DLY6	0 ms	000	Channel 6 disable delay time
			[2:0]	DIS_DLY5	0 ms	000	Channel 5 disable delay time
11	0x0B	DIS_DLY7	[2:0]	DIS_DLY7	0 ms	000	Channel 7 disable delay time
12	0x0C	VID1	[4:0]	VID1	0.80 V	11111	Channel 1 output voltage
13	0x0D	VID23	[6:4]	VID3	Adjustable	111	Channel 3 output voltage
			[3:0]	VID2	1.8 V	0100	Channel 2 output voltage
14	0x0E	VID45	[6:4]	VID5	3.3 V	011	Channel 5 output voltage
			[2:0]	VID4	Adjustable	111	Channel 4 output voltage
15	0x0F	VID6	[3:0]	VID6	Adjustable	1111	Channel 6 output voltage
16	0x10	VID7_LDO12	[6:5]	VID_LDO2	3.3 V	00	LDO2 output voltage
			4	VID_LDO1	5.0 V	1	LDO1 output voltage
			[1:0]	VID7	5.0 V	11	Channel 7 output voltage
18	0x12	SEL_FREQ	7	SEL_FSW	2 MHz	0	Master clock frequency
			5	FREQ6	$1/2 \times f_{SW}$	1	Channel 6 switching frequency
			4	FREQ5	$1/2 \times f_{SW}$	1	Channel 5 switching frequency
			3	FREQ4	$1/2 \times f_{SW}$	1	Channel 4 switching frequency
			2	FREQ3	$1/2 \times f_{SW}$	1	Channel 3 switching frequency
			1	FREQ2	$1/2 \times f_{SW}$	1	Channel 2 switching frequency
			0	FREQ1	$1/2 \times f_{SW}$	1	Channel 1 switching frequency

Register	Register Addr (Hex)	Register Name	Bit	Bit Name	Default Setting	Binary Code	Description
19	0x13	SEL_FREQ_CP	4	EN_CLKO	Enabled	1	Enable clock output
			[1:0]	FREQ_CP	1/4 × f_{SW}	01	Charge pump frequency
20	0x14	SEL_PHASE	5	PHASE6	Reversed	1	Channel 6 switching phase
			4	PHASE5	In phase	0	Channel 5 switching phase
			3	PHASE4	Reversed	1	Channel 4 switching phase
			2	PHASE3	In phase	0	Channel 3 switching phase
			1	PHASE2	Reversed	1	Channel 2 switching phase
23	0x17	PROT_DLY	[5:4]	UV_DLY	21 ms	01	Undervoltage delay time
			[1:0]	OV_DLY	1.3 ms	01	Overvoltage delay time
25	0x19	MASK_PWRG	6	MASK_PWRG7	Masked	1	Channel 7 power-good mask
			5	MASK_PWRG6	Not masked	0	Channel 6 power-good mask
			4	MASK_PWRG5	Masked	1	Channel 5 power-good mask
			3	MASK_PWRG4	Not masked	0	Channel 4 power-good mask
			2	MASK_PWRG3	Not masked	0	Channel 3 power-good mask
			1	MASK_PWRG2	Not masked	0	Channel 2 power-good mask
			0	MASK_PWRG1	Not masked	0	Channel 1 power-good mask
28	0x1C	AUTO-PSM	5	AUTO-PSM6	Auto PSM	1	Channel 6 auto PSM enable
			4	AUTO-PSM5	Auto PSM	1	Channel 5 auto PSM enable
			3	AUTO-PSM4	Auto PSM	1	Channel 4 auto PSM enable
			2	AUTO-PSM3	Auto PSM	1	Channel 3 auto PSM enable
			1	AUTO-PSM2	Auto PSM	1	Channel 2 auto PSM enable
			0	AUTO-PSM1	Auto PSM	1	Channel 1 auto PSM enable
29	0x1D	SEQ_MODE	6	MODE_EN7	I^2C mode	0	Channel 7 sequencer enable
			5	MODE_EN6	Sequencer mode	1	Channel 6 sequencer enable
			4	MODE_EN5	I^2C mode	0	Channel 5 sequencer enable
			3	MODE_EN4	Sequencer mode	1	Channel 4 sequencer enable
			2	MODE_EN3	Sequencer mode	1	Channel 3 sequencer enable
			1	MODE_EN2	Sequencer mode	1	Channel 2 sequencer enable
			0	MODE_EN1	Sequencer mode	1	Channel 1 sequencer enable
30	0x1E	ADJ_BST_VTH6	4	BUCK6_ONLY	Buck boost	0	Channel 6 buck or buck boost
			[1:0]	BOOST6_VTH	VOUT6/0.82	00	Channel 6 buck boost threshold
32	0x20	DCM56_GSCAL1	4	DCM56	Auto PSM	0	Channel 5/Channel 6 enable DCM mode
			0	GATE_SCAL1	Disabled	0	Channel 1 enable gate scaling
33	0x21	SEL_INP_LDO12	4	SEL_INP_LDO2	VISW2	1	LDO2 input select
			0	SEL_INP_LDO1	VISW1	1	LDO1 input select
34	0x22	SEL_IND_UV5	[5:4]	UV_DLY5	45 ms	10	Channel 5 UVP delay time
			0	SEL_IND_UV5	Sync with UVP	0	Channel 5 independent UVP control
35	0x23	OPTION_SEL	3	REDUCE_VOUT1	Reduced VID1 range	1	Channel 1 output voltage range
			2	DIS_DLY_EXTEND	Normal disable delay time	0	Extend disable delay time
			1	DIS_EN34_CH4	EN34 control	0	Channel 4 enable control via EN34
			0	DIS_EN34_CH3	EN34 control	0	Channel 3 enable control via EN34

OUTLINE DIMENSIONS

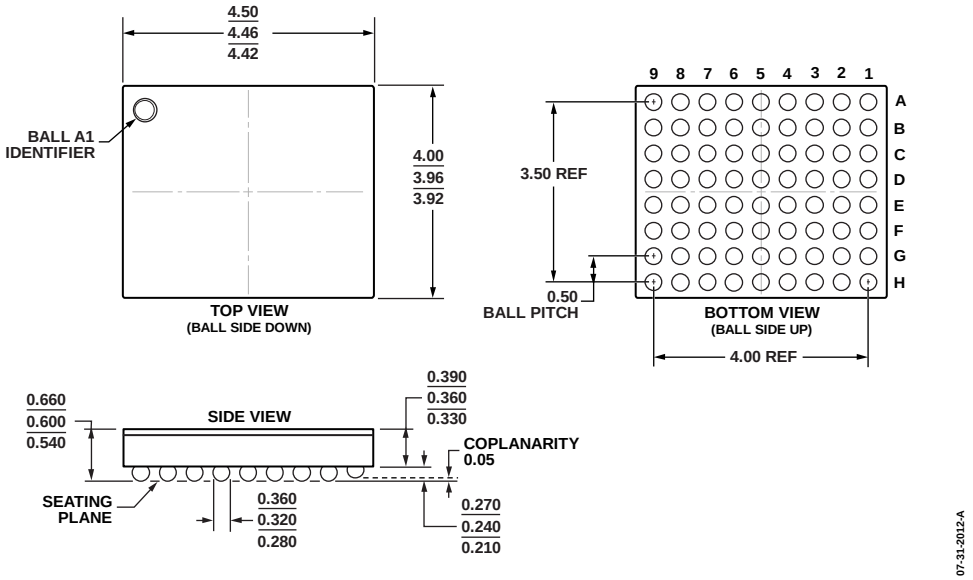

Figure 60. 72-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-72-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADP5080ACBZ-1-RL	−25°C to +85°C	72-Ball Wafer Level Chip Scale Package [WLCSP], 0.5 mm Pitch	CB-72-2

[1] Z = RoHS Compliant Part.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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