

# 512K x 32 Static RAM

## Features

- **High speed**
  - $t_{AA} = 8, 10, 12 \text{ ns}$
- **Low active power**
  - 1080 mW (max.)
- **Operating voltages of  $3.3 \pm 0.3V$**
- **2.0V data retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with  $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$  features**

## Functional Description

The CY7C1062AV33 is a high-performance CMOS Static RAM organized as 524,288 words by 32 bits.

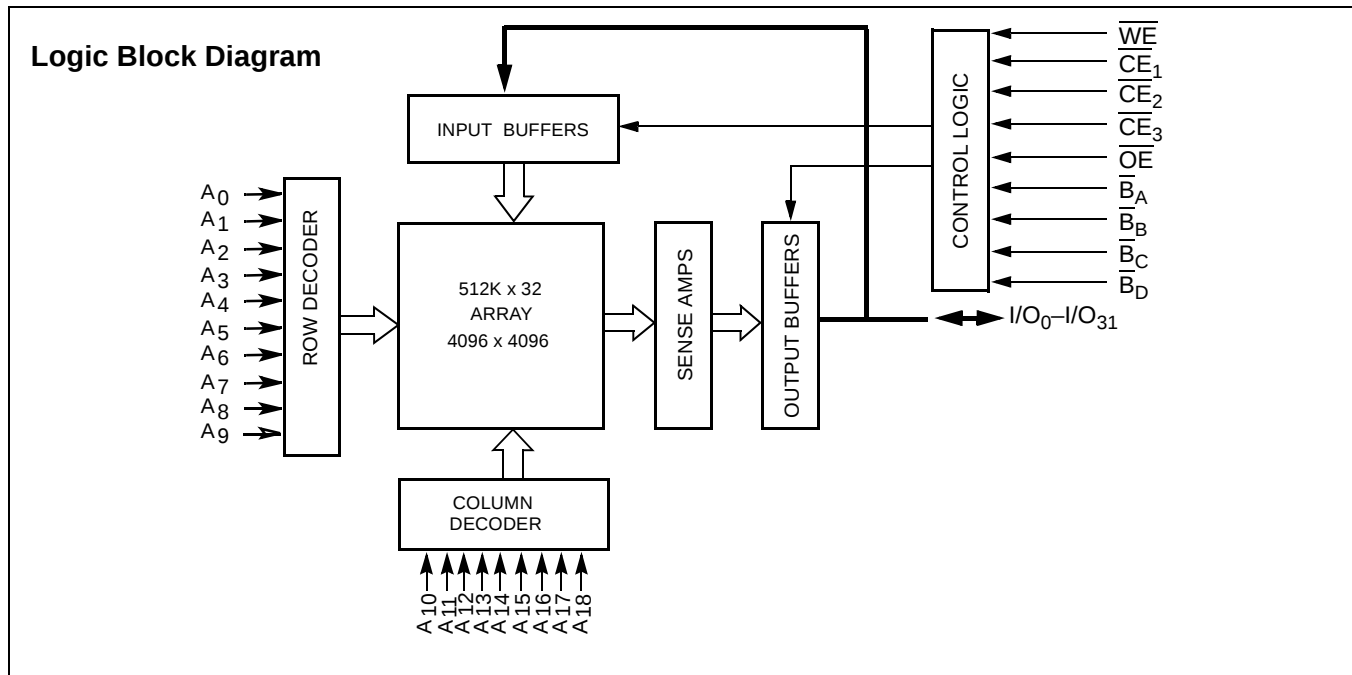
Writing to the device is accomplished by enabling the chip ( $\overline{CE}_1$ ,  $\overline{CE}_2$  and  $\overline{CE}_3$  LOW) and forcing the Write Enable (WE) input LOW. If Byte Enable A ( $\overline{B}_A$ ) is LOW, then data from I/O pins ( $I/O_0$  through  $I/O_7$ ), is written into the location specified on

the address pins ( $A_0$  through  $A_{18}$ ). If Byte Enable B ( $\overline{B}_B$ ) is LOW, then data from I/O pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ). Likewise,  $\overline{B}_C$  and  $\overline{B}_D$  correspond with the I/O pins  $I/O_{16}$  to  $I/O_{23}$  and  $I/O_{24}$  to  $I/O_{31}$ , respectively.

Reading from the device is accomplished by enabling the chip ( $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$  LOW) while forcing the Output Enable ( $\overline{OE}$ ) LOW and Write Enable (WE) HIGH. If the first Byte Enable ( $\overline{B}_A$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_0$  to  $I/O_7$ . If Byte Enable B ( $\overline{B}_B$ ) is LOW, then data from memory will appear on  $I/O_8$  to  $I/O_{15}$ . Similarly,  $\overline{B}_C$  and  $\overline{B}_D$  correspond to the third and fourth bytes. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins ( $I/O_0$  through  $I/O_{31}$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}_1$ ,  $\overline{CE}_2$  or  $\overline{CE}_3$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the byte selects are disabled ( $\overline{B}_{A-D}$  HIGH), or during a write operation ( $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$  LOW, and WE LOW).

The CY7C1062AV33 is available in a 119-ball pitch ball grid array (PBGA) package.



## Selection Guide

|                              |             | -8  | -10 | -12 | Unit |
|------------------------------|-------------|-----|-----|-----|------|
| Maximum Access Time          |             | 8   | 10  | 12  | ns   |
| Maximum Operating Current    | Com'I       | 300 | 275 | 260 | mA   |
|                              | Ind'I       | 300 | 275 | 260 |      |
| Maximum CMOS Standby Current | Com'I/Ind'I | 50  | 50  | 50  | mA   |

**Pin Configuration**
**119-ball PBGA**

(Top View)

|          | 1                 | 2                | 3                 | 4                 | 5                 | 6                | 7                 |
|----------|-------------------|------------------|-------------------|-------------------|-------------------|------------------|-------------------|
| <b>A</b> | I/O <sub>16</sub> | A                | A                 | A                 | A                 | A                | I/O <sub>0</sub>  |
| <b>B</b> | I/O <sub>17</sub> | A                | A                 | $\overline{CE}_1$ | A                 | A                | I/O <sub>1</sub>  |
| <b>C</b> | I/O <sub>18</sub> | $\overline{B}_c$ | $\overline{CE}_2$ | NC                | $\overline{CE}_3$ | $\overline{B}_a$ | I/O <sub>2</sub>  |
| <b>D</b> | I/O <sub>19</sub> | V <sub>DD</sub>  | V <sub>SS</sub>   | V <sub>SS</sub>   | V <sub>SS</sub>   | V <sub>DD</sub>  | I/O <sub>3</sub>  |
| <b>E</b> | I/O <sub>20</sub> | V <sub>SS</sub>  | V <sub>DD</sub>   | V <sub>SS</sub>   | V <sub>DD</sub>   | V <sub>SS</sub>  | I/O <sub>4</sub>  |
| <b>F</b> | I/O <sub>21</sub> | V <sub>DD</sub>  | V <sub>SS</sub>   | V <sub>SS</sub>   | V <sub>SS</sub>   | V <sub>DD</sub>  | I/O <sub>5</sub>  |
| <b>G</b> | I/O <sub>22</sub> | V <sub>SS</sub>  | V <sub>DD</sub>   | V <sub>SS</sub>   | V <sub>DD</sub>   | V <sub>SS</sub>  | I/O <sub>6</sub>  |
| <b>H</b> | I/O <sub>23</sub> | V <sub>DD</sub>  | V <sub>SS</sub>   | V <sub>SS</sub>   | V <sub>SS</sub>   | V <sub>DD</sub>  | I/O <sub>7</sub>  |
| <b>J</b> | NC                | V <sub>SS</sub>  | V <sub>DD</sub>   | V <sub>SS</sub>   | V <sub>DD</sub>   | V <sub>SS</sub>  | DNU               |
| <b>K</b> | I/O <sub>24</sub> | V <sub>DD</sub>  | V <sub>SS</sub>   | V <sub>SS</sub>   | V <sub>SS</sub>   | V <sub>DD</sub>  | I/O <sub>8</sub>  |
| <b>L</b> | I/O <sub>25</sub> | V <sub>SS</sub>  | V <sub>DD</sub>   | V <sub>SS</sub>   | V <sub>DD</sub>   | V <sub>SS</sub>  | I/O <sub>9</sub>  |
| <b>M</b> | I/O <sub>26</sub> | V <sub>DD</sub>  | V <sub>SS</sub>   | V <sub>SS</sub>   | V <sub>SS</sub>   | V <sub>DD</sub>  | I/O <sub>10</sub> |
| <b>N</b> | I/O <sub>27</sub> | V <sub>SS</sub>  | V <sub>DD</sub>   | V <sub>SS</sub>   | V <sub>DD</sub>   | V <sub>SS</sub>  | I/O <sub>11</sub> |
| <b>P</b> | I/O <sub>28</sub> | V <sub>DD</sub>  | V <sub>SS</sub>   | V <sub>SS</sub>   | V <sub>SS</sub>   | V <sub>DD</sub>  | I/O <sub>12</sub> |
| <b>R</b> | I/O <sub>29</sub> | A                | $\overline{B}_d$  | NC                | $\overline{B}_b$  | A                | I/O <sub>13</sub> |
| <b>T</b> | I/O <sub>30</sub> | A                | A                 | $\overline{WE}$   | A                 | A                | I/O <sub>14</sub> |
| <b>U</b> | I/O <sub>31</sub> | A                | A                 | $\overline{OE}$   | A                 | A                | I/O <sub>15</sub> |

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with  
Power Applied ..... -55°C to +125°C

Supply Voltage on  $V_{CC}$  to Relative GND<sup>[1]</sup> .... -0.5V to +4.6V

DC Voltage Applied to Outputs  
in High-Z State<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

Current into Outputs (LOW) ..... 20 mA

### Operating Range

| Range      | Ambient Temperature | $V_{CC}$    |
|------------|---------------------|-------------|
| Commercial | 0°C to +70°C        | 3.3V ± 0.3V |
| Industrial | -40°C to +85°C      |             |

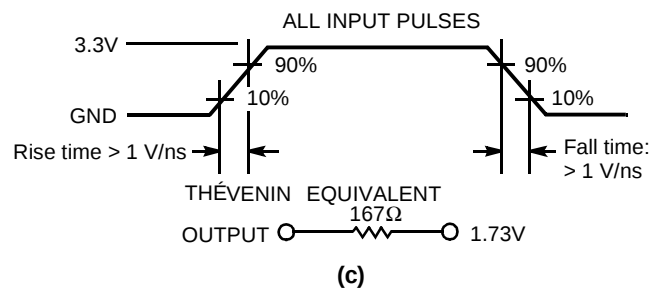
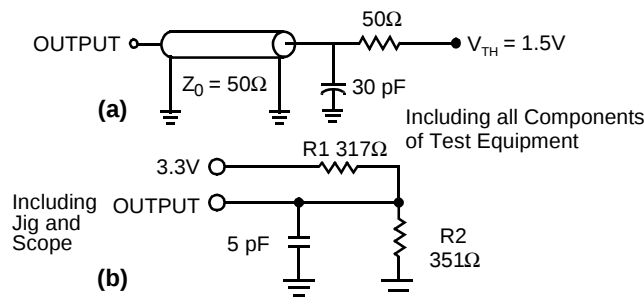
### DC Electrical Characteristics Over the Operating Range

| Parameter        | Description                                  | Test Conditions                                                                                                                                 | -8          |                       | -10  |                       | -12  |                       | Unit |     |    |
|------------------|----------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|-------------|-----------------------|------|-----------------------|------|-----------------------|------|-----|----|
|                  |                                              |                                                                                                                                                 | Min.        | Max.                  | Min. | Max.                  | Min. | Max.                  |      |     |    |
| V <sub>OH</sub>  | Output HIGH Voltage                          | V <sub>CC</sub> = Min.,<br>I <sub>OH</sub> = −4.0 mA                                                                                            | 2.4         |                       | 2.4  |                       | 2.4  |                       | V    |     |    |
| V <sub>OL</sub>  | Output LOW Voltage                           | V <sub>CC</sub> = Min.,<br>I <sub>OL</sub> = 8.0 mA                                                                                             |             | 0.4                   |      | 0.4                   |      | 0.4                   | V    |     |    |
| V <sub>IH</sub>  | Input HIGH Voltage                           |                                                                                                                                                 | 2.0         | V <sub>CC</sub> + 0.3 | 2.0  | V <sub>CC</sub> + 0.3 | 2.0  | V <sub>CC</sub> + 0.3 | V    |     |    |
| V <sub>IL</sub>  | Input LOW Voltage <sup>[1]</sup>             |                                                                                                                                                 | −0.3        | 0.8                   | −0.3 | 0.8                   | −0.3 | 0.8                   | V    |     |    |
| I <sub>IX</sub>  | Input Load Current                           | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                                                                                                          | −1          | +1                    | −1   | +1                    | −1   | +1                    | μA   |     |    |
| I <sub>OZ</sub>  | Output Leakage Current                       | GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled                                                                                      | −1          | +1                    | −1   | +1                    | −1   | +1                    | μA   |     |    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current     | V <sub>CC</sub> = Max., f = f <sub>MAX</sub><br>= 1/t <sub>RC</sub>                                                                             | Com'l       |                       |      | 300                   |      | 275                   |      | 260 | mA |
|                  |                                              |                                                                                                                                                 | Ind'l       |                       |      | 300                   |      | 275                   |      | 260 | mA |
| I <sub>SB1</sub> | Automatic CE Power-down Current —TTL Inputs  | Max. V <sub>CC</sub> , CE ≥ V <sub>IH</sub><br>V <sub>IN</sub> ≥ V <sub>IH</sub> or<br>V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub> |             | 70                    |      | 70                    |      | 70                    |      | mA  |    |
| I <sub>SB2</sub> | Automatic CE Power-down Current —CMOS Inputs | Max. V <sub>CC</sub> ,<br>CE ≥ V <sub>CC</sub> − 0.3V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.3V,<br>or V <sub>IN</sub> ≤ 0.3V, f = 0         | Com'l/Ind'l |                       |      | 50                    |      | 50                    |      | 50  | mA |

### Capacitance<sup>[2]</sup>

| Parameter | Description       | Test Conditions                                                  | Max. | Unit |
|-----------|-------------------|------------------------------------------------------------------|------|------|
| $C_{IN}$  | Input Capacitance | $T_A = 25^\circ\text{C}$ , $f = 1 \text{ MHz}$ , $V_{CC} = 3.3V$ | 8    | pF   |
| $C_{OUT}$ | I/O Capacitance   |                                                                  | 10   | pF   |

### AC Test Loads and Waveforms<sup>[3]</sup>

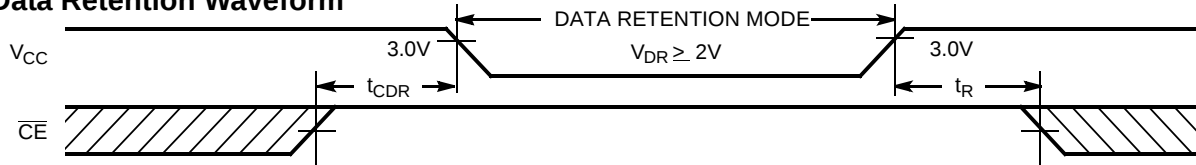


#### Notes:

- $V_{IL} (\text{min.}) = -2.0V$  for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.
- Valid SRAM operation does not occur until the power supplies have reached the minimum operating  $V_{DD}$  (3.0V). As soon as 1ms ( $T_{power}$ ) after reaching the minimum operating  $V_{DD}$ , normal SRAM operation can begin including reduction in  $V_{DD}$  to the data retention ( $V_{CCDR}$ , 2.0V) voltage.

**AC Switching Characteristics** Over the Operating Range<sup>[4]</sup>

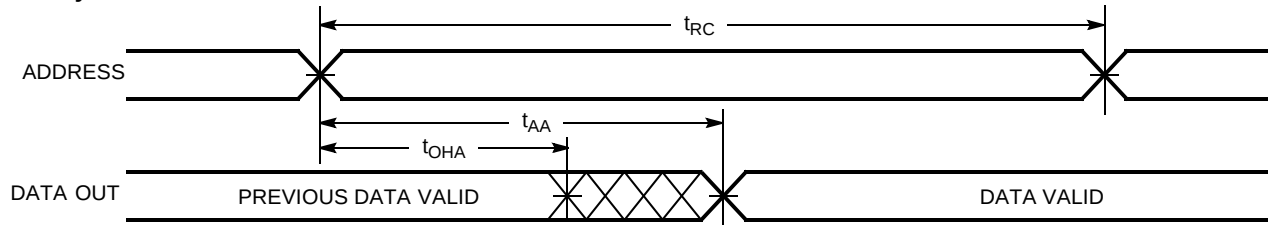
| Parameter                     | Description                                                                              | -8   |      | -10  |      | -12  |      | Unit |
|-------------------------------|------------------------------------------------------------------------------------------|------|------|------|------|------|------|------|
|                               |                                                                                          | Min. | Max. | Min. | Max. | Min. | Max. |      |
| Read Cycle                    |                                                                                          |      |      |      |      |      |      |      |
| t <sub>power</sub>            | V <sub>CC</sub> (typical) to the first access <sup>[5]</sup>                             | 1    |      | 1    |      | 1    |      | ms   |
| t <sub>RC</sub>               | Read Cycle Time                                                                          | 8    |      | 10   |      | 12   |      | ns   |
| t <sub>AA</sub>               | Address to Data Valid                                                                    |      | 8    |      | 10   |      | 12   | ns   |
| t <sub>OHA</sub>              | Data Hold from Address Change                                                            | 3    |      | 3    |      | 3    |      | ns   |
| t <sub>ACE</sub>              | CE <sub>1</sub> , CE <sub>2</sub> , or CE <sub>3</sub> LOW to Data Valid                 |      | 8    |      | 10   |      | 12   | ns   |
| t <sub>DOE</sub>              | OE LOW to Data Valid                                                                     |      | 5    |      | 5    |      | 6    | ns   |
| t <sub>LZOE</sub>             | OE LOW to Low-Z <sup>[6]</sup>                                                           | 1    |      | 1    |      | 1    |      | ns   |
| t <sub>HZOE</sub>             | OE HIGH to High-Z <sup>[6]</sup>                                                         |      | 5    |      | 5    |      | 6    | ns   |
| t <sub>LZCE</sub>             | CE <sub>1</sub> , CE <sub>2</sub> , or CE <sub>3</sub> LOW to Low-Z <sup>[6]</sup>       | 3    |      | 3    |      | 3    |      | ns   |
| t <sub>HZCE</sub>             | CE <sub>1</sub> , CE <sub>2</sub> , or CE <sub>3</sub> HIGH to High-Z <sup>[6]</sup>     |      | 5    |      | 5    |      | 6    | ns   |
| t <sub>PU</sub>               | CE <sub>1</sub> , CE <sub>2</sub> , or CE <sub>3</sub> LOW to Power-up <sup>[7]</sup>    | 0    |      | 0    |      | 0    |      | ns   |
| t <sub>PD</sub>               | CE <sub>1</sub> , CE <sub>2</sub> , or CE <sub>3</sub> HIGH to Power-down <sup>[7]</sup> |      | 8    |      | 10   |      | 12   | ns   |
| t <sub>DBE</sub>              | Byte Enable to Data Valid                                                                |      | 5    |      | 5    |      | 6    | ns   |
| t <sub>LZBE</sub>             | Byte Enable to Low-Z <sup>[6]</sup>                                                      | 1    |      | 1    |      | 1    |      | ns   |
| t <sub>HZBE</sub>             | Byte Disable to High-Z <sup>[6]</sup>                                                    |      | 5    |      | 5    |      | 6    | ns   |
| Write Cycle <sup>[8, 9]</sup> |                                                                                          |      |      |      |      |      |      |      |
| t <sub>WC</sub>               | Write Cycle Time                                                                         | 8    |      | 10   |      | 12   |      | ns   |
| t <sub>SCE</sub>              | CE <sub>1</sub> , CE <sub>2</sub> , or CE <sub>3</sub> LOW to Write End                  | 6    |      | 7    |      | 8    |      | ns   |
| t <sub>AW</sub>               | Address Set-up to Write End                                                              | 6    |      | 7    |      | 8    |      | ns   |
| t <sub>HA</sub>               | Address Hold from Write End                                                              | 0    |      | 0    |      | 0    |      | ns   |
| t <sub>SA</sub>               | Address Set-up to Write Start                                                            | 0    |      | 0    |      | 0    |      | ns   |
| t <sub>PWE</sub>              | WE Pulse Width                                                                           | 6    |      | 7    |      | 8    |      | ns   |
| t <sub>SD</sub>               | Data Set-up to Write End                                                                 | 5    |      | 5.5  |      | 6    |      | ns   |
| t <sub>HD</sub>               | Data Hold from Write End                                                                 | 0    |      | 0    |      | 0    |      | ns   |
| t <sub>LZWE</sub>             | WE HIGH to Low-Z <sup>[6]</sup>                                                          | 3    |      | 3    |      | 3    |      | ns   |
| t <sub>HZWE</sub>             | WE LOW to High-Z <sup>[6]</sup>                                                          |      | 5    |      | 5    |      | 6    | ns   |
| t <sub>BW</sub>               | Byte Enable to End of Write                                                              | 6    |      | 7    |      | 8    |      | ns   |

**Data Retention Waveform**

**Notes:**

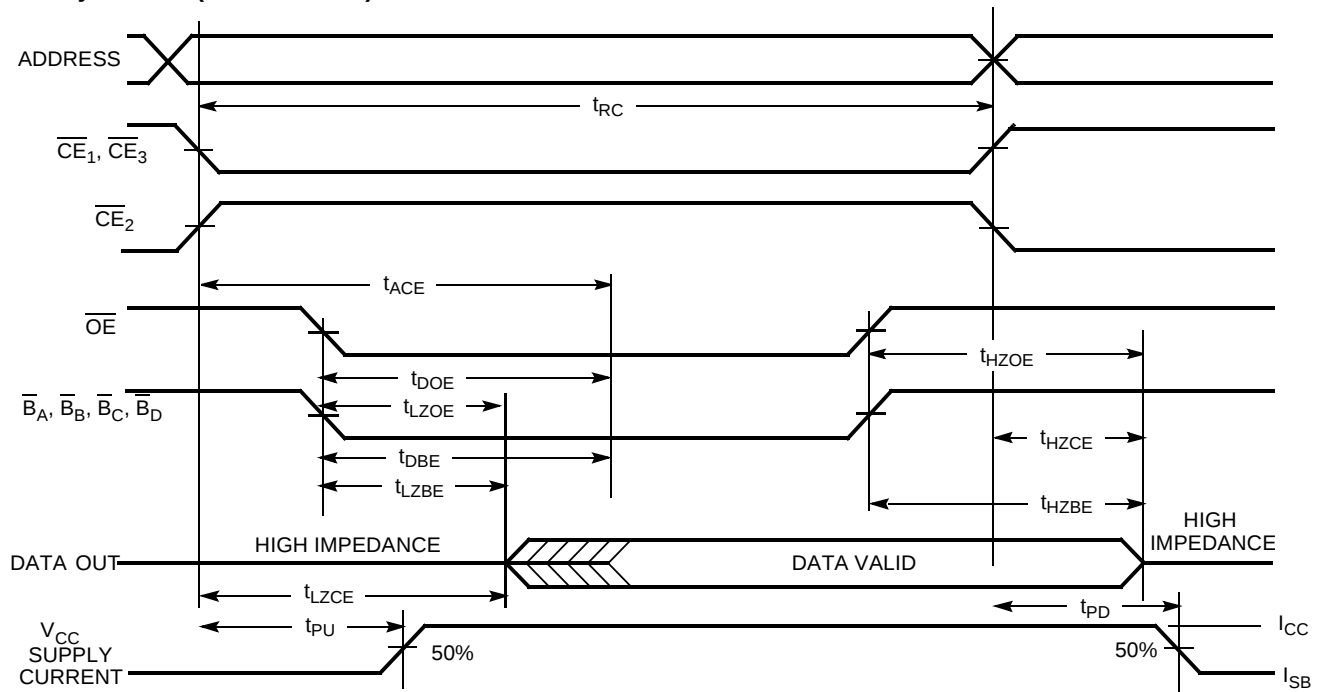
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{\text{OL}}/I_{\text{OH}}$  and transmission line loads. Test conditions for the read cycle use output loading as shown in (a) of AC Test Loads, unless specified otherwise.
- This part has a voltage regulator that steps down the voltage from 3V to 2V internally.  $t_{\text{power}}$  time has to be provided initially before a read/write operation is started.
- $t_{\text{HZOE}}$ ,  $t_{\text{HZCE}}$ ,  $t_{\text{HZWE}}$ ,  $t_{\text{HZBE}}$ , and  $t_{\text{LZOE}}$ ,  $t_{\text{LZCE}}$ ,  $t_{\text{LZWE}}$ , and  $t_{\text{LZBE}}$  are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured  $\pm 200$  mV from steady-state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}_1$  LOW,  $\overline{\text{CE}}_2$  HIGH,  $\overline{\text{CE}}_3$  LOW, and  $\overline{\text{WE}}$  LOW. The chip enables must be active and  $\overline{\text{WE}}$  must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

## Switching Waveforms

**Read Cycle No. 1** [10, 11]

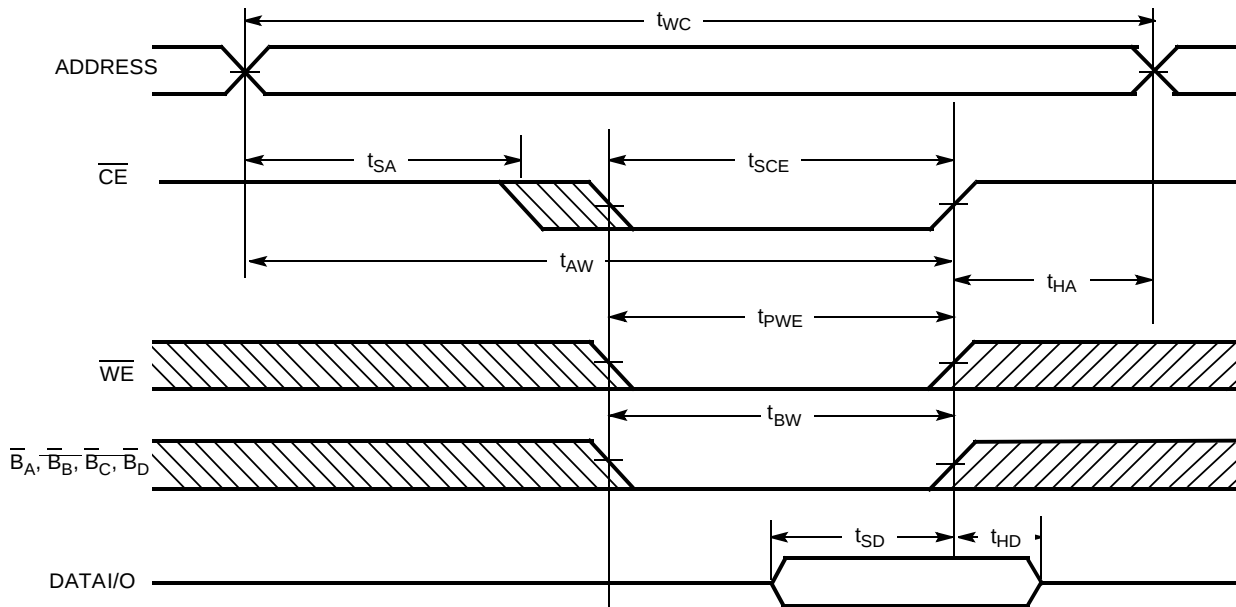
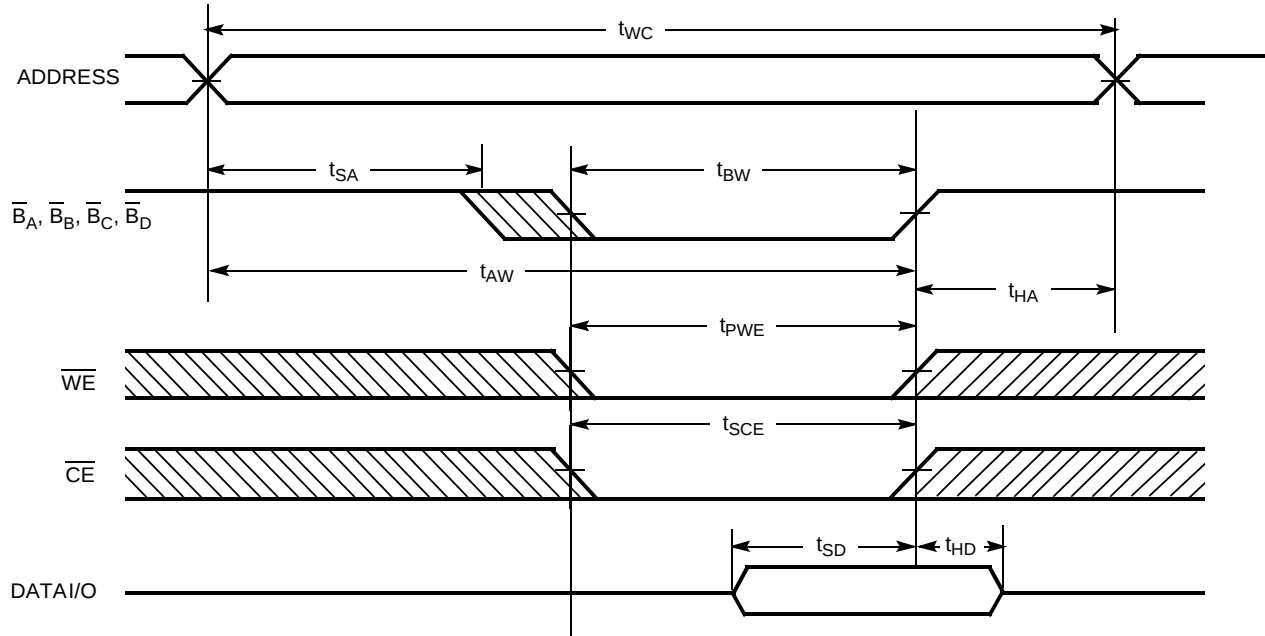


**Read Cycle No. 2 ( $\overline{OE}$  Controlled)** [11, 12]

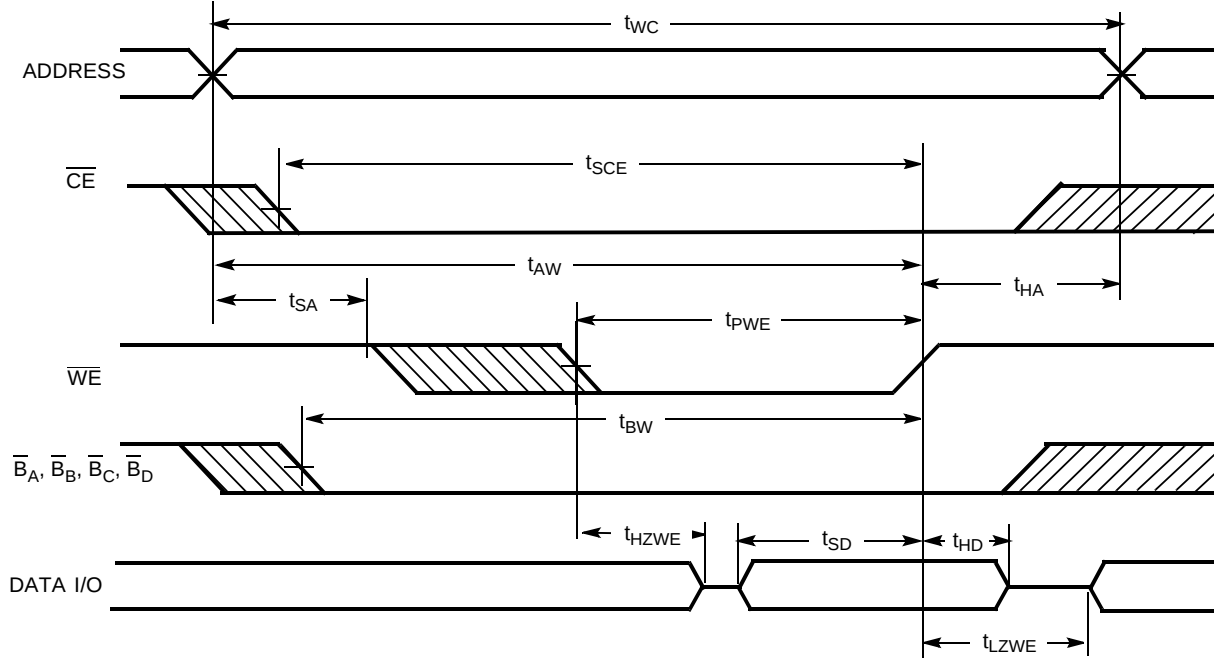


**Notes:**

10. Device is continuously selected.  $\overline{OE}, \overline{CE}, \overline{B}_A, \overline{B}_B, \overline{B}_C, \overline{B}_D = V_{IL}$ .
11.  $\overline{WE}$  is HIGH for read cycle.
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)<sup>[13, 14, 15]</sup>**

**Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)<sup>[13, 14, 15]</sup>**

**Notes:**

13.  $\overline{\text{CE}}$  indicates a combination of all three chip enables. When ACTIVE LOW,  $\overline{\text{CE}}$  indicates the  $\overline{\text{CE}}_1$ ,  $\overline{\text{CE}}_2$  and  $\overline{\text{CE}}_3$  are LOW.
14. Data I/O is high-impedance if  $\overline{\text{OE}}$  or  $\overline{\text{B}}_{\text{A}}, \overline{\text{B}}_{\text{B}}, \overline{\text{B}}_{\text{C}}, \overline{\text{B}}_{\text{D}} = V_{\text{IH}}$ .
15. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.

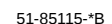
**Switching Waveforms (continued)**
**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)**

**Truth Table**

| $\overline{CE}_1$ | $\overline{CE}_2$ | $\overline{CE}_3$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{B_A}$ | $\overline{B_B}$ | $\overline{B_C}$ | $\overline{B_D}$ | I/O <sub>0-7</sub> | I/O <sub>8-15</sub> | I/O <sub>16-23</sub> | I/O <sub>24-31</sub> | Mode                       | Power        |
|-------------------|-------------------|-------------------|-----------------|-----------------|------------------|------------------|------------------|------------------|--------------------|---------------------|----------------------|----------------------|----------------------------|--------------|
| H                 | L                 | H                 | X               | X               | X                | X                | X                | X                | High-Z             | High-Z              | High-Z               | High-Z               | Power Down                 | ( $I_{SB}$ ) |
| L                 | H                 | L                 | X               | X               | X                | X                | X                | X                | High-Z             | High-Z              | High-Z               | High-Z               | Power Down                 | ( $I_{SB}$ ) |
| L                 | L                 | L                 | L               | H               | L                | L                | L                | L                | Data Out           | Data Out            | Data Out             | Data Out             | Read All Bits              | ( $I_{CC}$ ) |
| L                 | L                 | L                 | L               | H               | L                | H                | H                | H                | Data Out           | High-Z              | High-Z               | High-Z               | Read Byte A Bits Only      | ( $I_{CC}$ ) |
| L                 | L                 | L                 | L               | H               | H                | L                | H                | H                | High-Z             | Data Out            | High-Z               | High-Z               | Read Byte B Bits Only      | ( $I_{CC}$ ) |
| L                 | L                 | L                 | L               | H               | H                | H                | L                | H                | High-Z             | High-Z              | Data Out             | High-Z               | Read Byte C Bits Only      | ( $I_{CC}$ ) |
| L                 | L                 | L                 | L               | H               | H                | H                | H                | L                | High-Z             | High-Z              | High-Z               | Data Out             | Read Byte D Bits Only      | ( $I_{CC}$ ) |
| L                 | L                 | L                 | X               | L               | L                | L                | L                | L                | Data In            | Data In             | Data In              | Data In              | Write All Bits             | ( $I_{CC}$ ) |
| L                 | L                 | L                 | X               | L               | L                | H                | H                | H                | Data In            | High-Z              | High-Z               | High-Z               | Write Byte A Bits Only     | ( $I_{CC}$ ) |
| L                 | L                 | L                 | X               | L               | H                | L                | H                | H                | High-Z             | Data In             | High-Z               | High-Z               | Write Byte B Bits Only     | ( $I_{CC}$ ) |
| L                 | L                 | L                 | X               | L               | H                | H                | L                | H                | High-Z             | High-Z              | Data In              | High-Z               | Write Byte C Bits Only     | ( $I_{CC}$ ) |
| L                 | L                 | L                 | X               | L               | H                | H                | H                | L                | High-Z             | High-Z              | High-Z               | Data In              | Write Byte D Bits Only     | ( $I_{CC}$ ) |
| L                 | L                 | L                 | H               | H               | X                | X                | X                | X                | High-Z             | High-Z              | High-Z               | High-Z               | Selected, Outputs Disabled | ( $I_{CC}$ ) |



| Speed (ns) | Ordering Code      | Package Name | Package Type             | Operating Range |
|------------|--------------------|--------------|--------------------------|-----------------|
| 8          | CY7C1062AV33-8BGC  | BG119        | 14 x 22 mm 119-ball PBGA | Commercial      |
|            | CY7C1062AV33-8BGI  |              |                          | Industrial      |
| 10         | CY7C1062AV33-10BGC |              |                          | Commercial      |
|            | CY7C1062AV33-10BGI |              |                          | Industrial      |
| 12         | CY7C1062AV33-12BGC |              |                          | Commercial      |
|            | CY7C1062AV33-12BGI |              |                          | Industrial      |

### 119-ball PBGA (14 x 22 x 2.4 mm) BG119



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**Document History Page**

| Document Title: CY7C1062AV33 512K x 32 Static RAM<br>Document Number: 38-05137 |         |            |                 |                                                                                                                                                                                                                                  |
|--------------------------------------------------------------------------------|---------|------------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| REV.                                                                           | ECN NO. | Issue Date | Orig. of Change | Description of Change                                                                                                                                                                                                            |
| **                                                                             | 109752  | 02/27/02   | HGK             | New Data Sheet                                                                                                                                                                                                                   |
| *A                                                                             | 117059  | 09/19/02   | DFP             | Removed 15-ns bin and added 8-ns bin.<br>Changed CE <sub>2</sub> TO CE <sub>2</sub> .<br>Changed C <sub>IN</sub> – input capacitance – from 6 pF to 8 pF.<br>Changed C <sub>OUT</sub> – output capacitance – from 8 pF to 10 pF. |
| *B                                                                             | 119389  | 10/07/02   | DFP             | Updated I <sub>CC</sub> , T <sub>sd</sub> , and T <sub>doe</sub> parameters.<br>Removed note 7 (I <sub>Z</sub> /h <sub>Z</sub> comment).                                                                                         |
| *C                                                                             | 120384  | 11/13/02   | DFP             | Final Data Sheet.<br>Removed note 2.<br>Added note 3 to “AC Test Loads and Waveforms” and note 7 to t <sub>pu</sub> and t <sub>pd</sub> .                                                                                        |
| *D                                                                             | 124440  | 2/25/03    | MEG             | Changed ISB1 from 100 mA to 70 mA                                                                                                                                                                                                |