BLF3G21-30

UHF power LDMOS transistor

Rev. 01 — 14 February 2007 | Product data sheet

1. Product profile

1.1 General description

30 W LDMOS power transistor for base station applications at frequencies from HF to 2200 MHz.

Table 1. Typical class-AB RF performance
I_{Dq} = 450 mA; T_h = 25 °C in a common source test circuit.

Mode of operation	f (MHz)	P_L (W)	G_p (dB)	η_D (%)	IMD3 (dB)	$P_{L(1dB)}$ (W)
CW	2000	36	12.5	43	-	36
Two-tone	2000	30	13.5	35	–26	-
		0.1 to 10	13.8	-	< –50	-

Table 2. Typical class-A RF performance
I_{Dq} = 1 A; T_h = 25 °C in a modified PHS test fixture.

Mode of operation	f (MHz)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	$ACPR_{600}$ (dBc)
PHS	1880 to 1920	9	16	20	–75

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

- Excellent back-off linearity
- Typical PHS performance at a supply voltage of 26 V and I_{Dq} of 1 A:
  - Average output power = 9 W
  - Gain = 16 dB (typ)
  - Efficiency = 20 %
  - $ACPR_{600}$ = –75 dBc
- Easy power control
- Excellent ruggedness
- High power gain
- Excellent thermal stability
- Designed for broadband operation (HF to 2200 MHz)

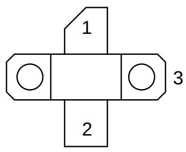
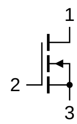
- No internal matching for broadband operation
- ESD protection

1.3 Applications

- RF power amplifiers for GSM, PHS, EDGE, CDMA and W-CDMA base stations and multicarrier applications in the HF to 2200 MHz frequency range
- Broadcast drivers

2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Symbol
1	drain		 sym112
2	gate		
3	source [1]		

[1] Connected to flange

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
BLF3G21-30	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT467C

4. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-	±15	V
I_D	drain current		-	4.5	A
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_h = 25 °C; $P_{L(AV)}$ = 15 W	[1]	1.6	K/W
$R_{th(j-h)}$	thermal resistance from junction to heatsink	T_h = 25 °C; $P_{L(AV)}$ = 15 W	[2]	2.1	K/W

[1] Thermal resistance is determined under specified RF operating conditions

[2] Depending on mounting condition in application

6. Characteristics

Table 7. Characteristics
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.7 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 70 mA	2.0	-	3.0	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	5	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 9 V; V_{DS} = 10 V	9	-	-	A
I_{GSS}	gate leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	-	11	nA
g_{fs}	transfer conductance	V_{DS} = 10 V; I_D = 2.5 A	-	3	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 9 V; I_D = 2.5 A	-	0.3	-	Ω
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 28 V; f = 1 MHz	-	1.7	-	pF

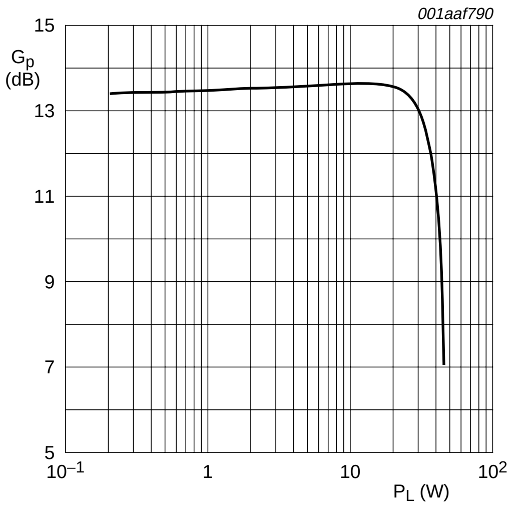
7. Application information

Table 8. Application information
V_{DS} = 26 V; T_h = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Mode of operation: Two-tone CW (100 kHz tone spacing); f = 2000 MHz; I_{Dq} = 450 mA						
G_p	power gain	$P_{L(PEP)}$ = 30 W	12.5	13.5	-	dB
RL_{in}	input return loss	$P_{L(PEP)}$ = 30 W	-	–16	–11	dB
η_D	drain efficiency	$P_{L(PEP)}$ = 30 W	32	35.0	-	%
IMD3	third order intermodulation distortion	$P_{L(PEP)}$ = 30 W	-	–26	–23	dBc
		$P_{L(PEP)}$ < 10 W	-	< –50	-	dBc
Mode of operation: one-tone CW; f = 2000 MHz; I_{Dq} = 450 mA						
G_p	power gain	P_L = $P_{L(1dB)}$ = 36 W	-	12.5	-	dB
η_D	drain efficiency	P_L = $P_{L(1dB)}$ = 36 W	-	43	-	%
Mode of operation: PHS; f = 1900 MHz; I_{Dq} = 1 A						
G_p	power gain	$P_{L(AV)}$ = 9 W	-	16	-	dB
η_D	drain efficiency	$P_{L(AV)}$ = 9 W	-	20	-	%

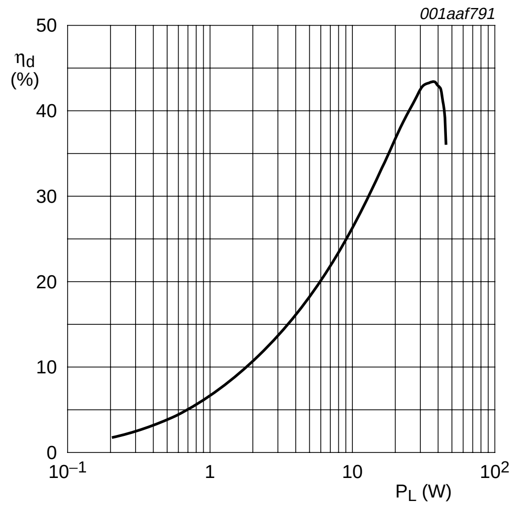
7.1 Ruggedness in class-AB operation

The BLF3G21-30 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 26 V; f = 2200 MHz at rated load power.



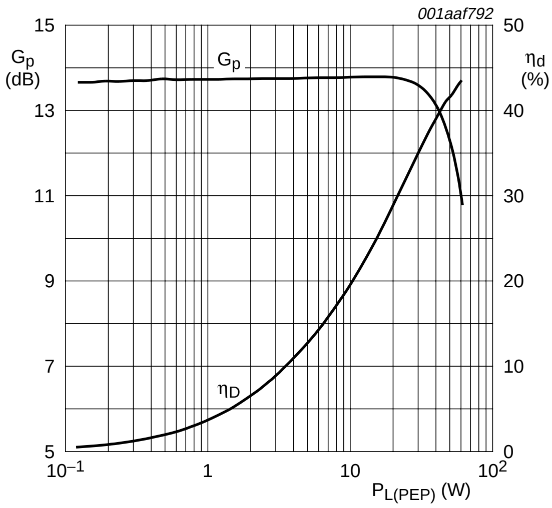
V_{DS} = 26 V; I_{Dq} = 450 mA; T_h = 25 °C; f = 2000 MHz

Fig 1. Power gain as function of CW load power; typical values



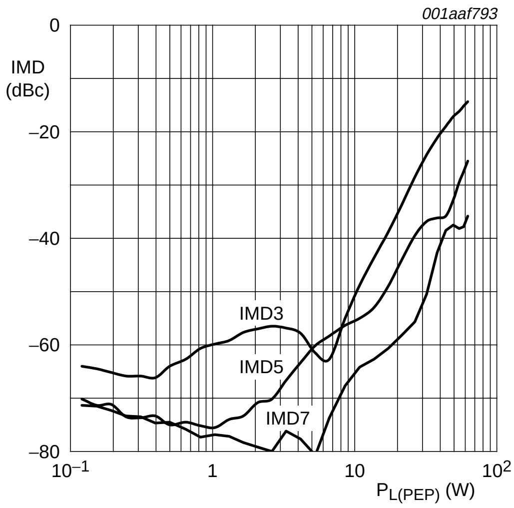
V_{DS} = 26 V; I_{Dq} = 450 mA; T_h = 25 °C; f = 2000 MHz

Fig 2. Drain efficiency as function of CW load power; typical values



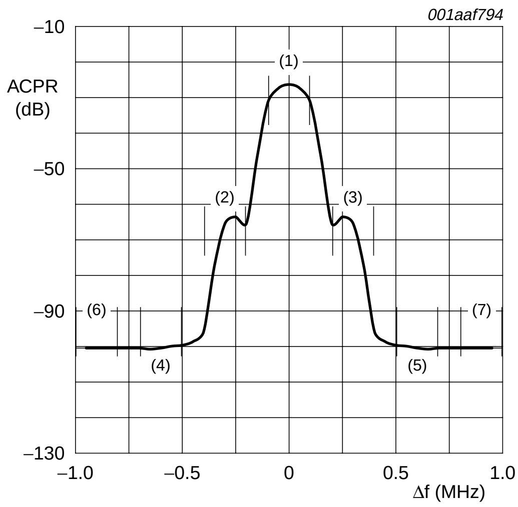
V_{DS} = 26 V; I_{Dq} = 450 mA; T_h ≤ 25 °C;
f_1 = 2000 MHz; f_2 = 2000.1 MHz

Fig 3. Two-tone power gain and drain efficiency as functions of peak envelope load power; typical values



V_{DS} = 26 V; I_{Dq} = 450 mA; T_h ≤ 25 °C;
f_1 = 2000 MHz; f_2 = 2000.1 MHz

Fig 4. Two-tone intermodulation distortion as function of peak envelope load power; typical values



(1) 192 kHz channel bandwidth

(2) $-ACPR_{300}$ at 192 kHz bandwidth

(3) $+ACPR_{300}$ at 192 kHz bandwidth

(4) $-ACPR_{600}$ at 192 kHz bandwidth

(5) $+ACPR_{600}$ at 192 kHz bandwidth

(6) $-ACPR_{900}$ at 192 kHz bandwidth

(7) $+ACPR_{900}$ at 192 kHz bandwidth

V_{DS} = 26 V; I_{Dq} = 1000 mA; $T_h \leq 25$ °C;
f_c = 1900 MHz; $P_{L(AV)}$ = 9 W

Fig 5. ACPR performance under PHS conditions, measured in application board

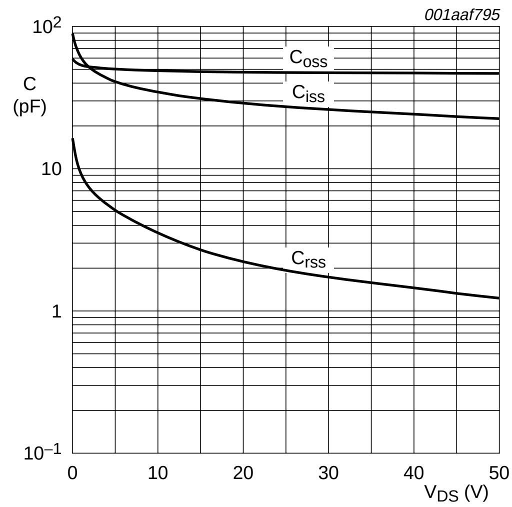
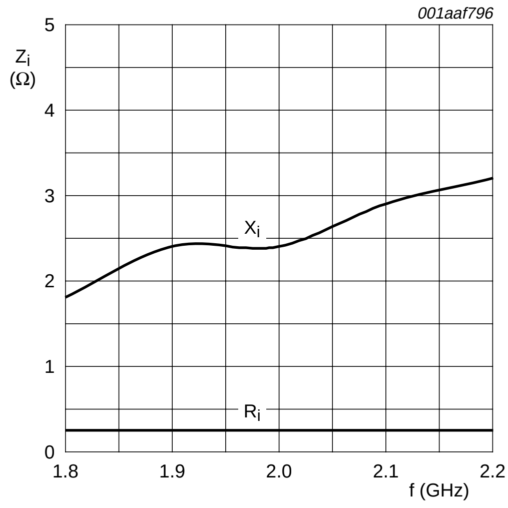
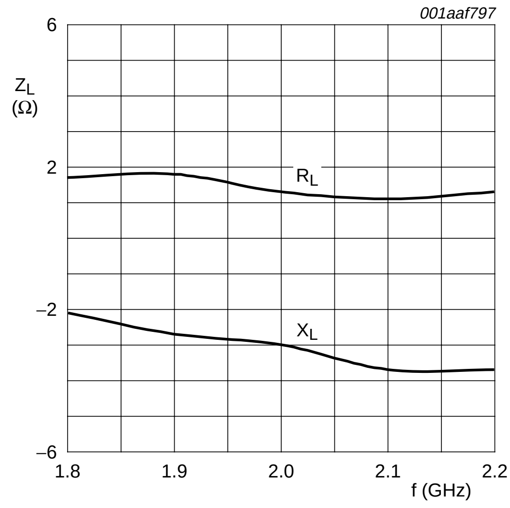


Fig 6. C_{iss}, C_{rss} and C_{oss} as functions of drain supply voltage; typical values



V_{DS} = 26 V; I_{Dq} = 450 mA; P_L = 45 W; $T_h \leq 25$ °C

Fig 7. Input impedance as function of frequency (series components); typical values



V_{DS} = 26 V; I_{Dq} = 450 mA; P_L = 45 W; $T_h \leq 25$ °C

Fig 8. Load impedance as function of frequency (series components); typical values

8. Test information

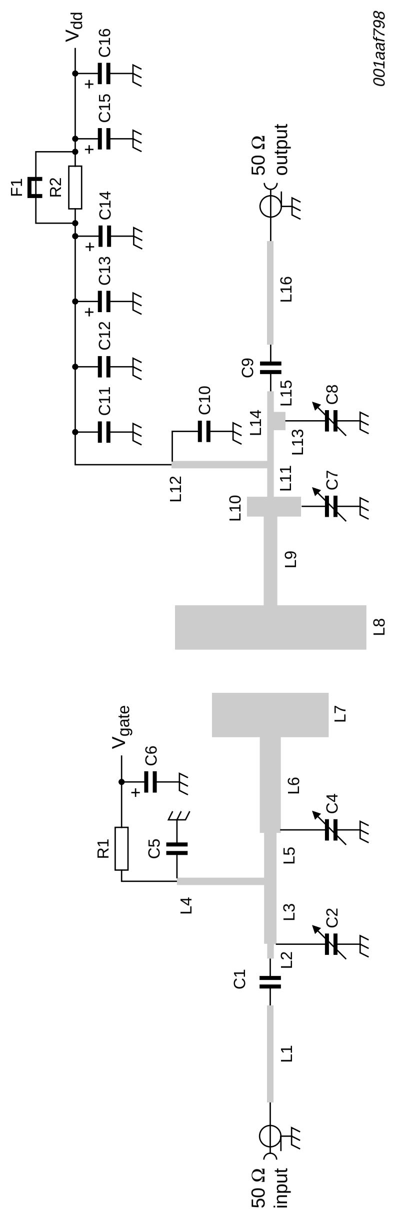
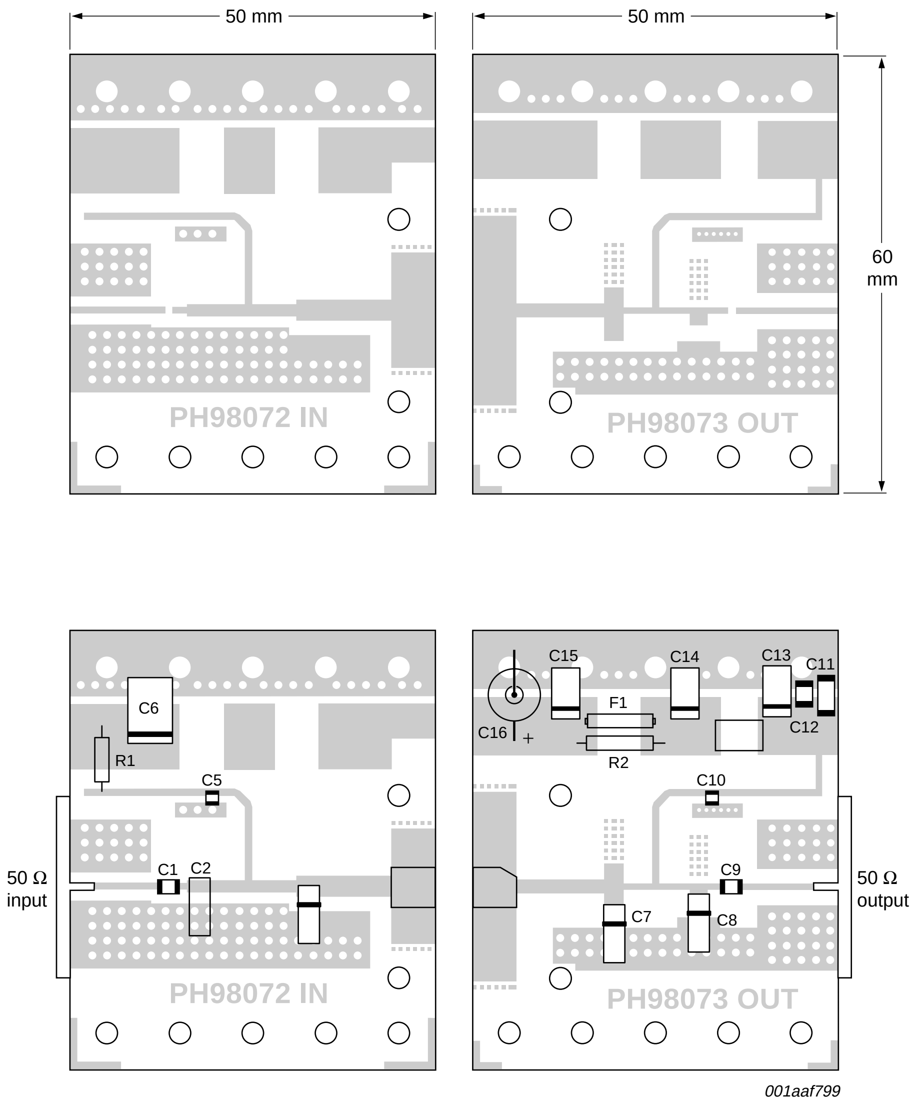


Fig 9. Class-AB test circuit for 2 GHz



The components are situated on one side of the copper-clad Printed-Circuit Board (PCB) with Teflon dielectric (ε_r = 6.15); thickness = 0.64 mm. The other side is unetched and serves as a ground plane.

See Table 9 for a list of components.

Fig 10. Component layout for 2 GHz class-AB test circuit

Table 9. List of components (see Figure 9 and Figure 10)

Component	Description		Value	Dimensions	Catalogue No.
C1, C9	multilayer ceramic chip capacitor	[2]	11 pF		
C2, C4, C7, C8	Tekelec variable capacitor; type 37271		0.6 pF to 4.5 pF		
C5, C10	multilayer ceramic chip capacitor	[1]	12 pF		
C6, C13, C14, C15	tantalum SMD capacitor		4.5 μF; 50 V		
C11	multilayer ceramic chip capacitor	[2]	1 nF		
C12	multilayer ceramic chip capacitor		100 nF		2222 581 16641
C16	electrolytic capacitor		100 μF; 63 V		2222 037 58101
F1	ferrite SMD bead			8DS3/3/8/9-4S2	4330 030 36301
L1	stripline	[3]	50 Ω	13 mm × 0.9 mm	
L2	stripline	[3]	50 Ω	2 mm × 0.9 mm	
L3	stripline	[3]	34.3 Ω	15 mm × 1.7 mm	
L4, L12	stripline	[3]	50 Ω	37 mm × 0.9 mm	
L5	stripline	[3]	34.3 Ω	6 mm × 1.7 mm	
L6	stripline	[3]	23.6 Ω	13 mm × 2.9 mm	
L7	stripline	[3]	5.6 Ω	6 mm × 15.8 mm	
L8	stripline	[3]	3.5 Ω	6 mm × 26 mm	
L9	stripline	[3]	31.9 Ω	12 mm × 1.9 mm	
L10	stripline	[3]	24.9 Ω	7.4 mm × 2.7 mm	
L11	stripline	[3]	50 Ω	3 mm × 0.9 mm	
L13	stripline	[3]	50 Ω	4.15 mm × 0.9 mm	
L14	stripline	[3]	26.3 Ω	2.5 mm × 2.5 mm	
L15	stripline	[3]	50 Ω	2.8 mm × 0.9 mm	
L16	stripline	[3]	50 Ω	14 mm × 0.9 mm	
R1, R2	metal film resistor		10 Ω; 0.6 W		2322 156 11009

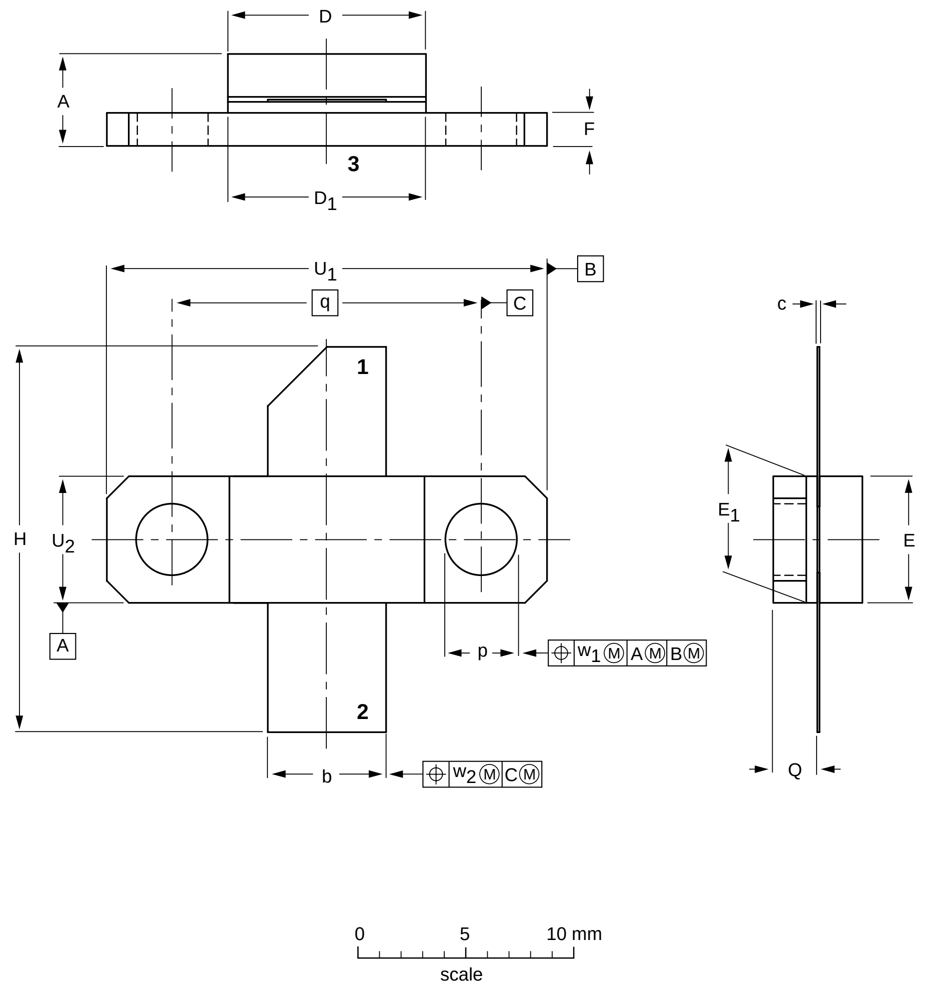
[1] American Technical Ceramics type 100B or capacitor of same quality

[2] American Technical Ceramics type 100A or capacitor of same quality

[3] The striplines are on a double copper-clad Printed-Circuit Board (PCB) with Teflon dielectric (ε_r = 6.15); thickness = 0.64 mm

9. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads **SOT467C**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	4.67 3.94	5.59 5.33	0.15 0.10	9.25 9.04	9.27 9.02	5.92 5.77	5.97 5.72	1.65 1.40	18.54 17.02	3.43 3.18	2.21 1.96	14.27	20.45 20.19	5.97 5.72	0.25	0.51
inch	0.184 0.155	0.220 0.210	0.006 0.004	0.364 0.356	0.365 0.355	0.233 0.227	0.235 0.225	0.065 0.055	0.73 0.67	0.135 0.125	0.087 0.077	0.562	0.805 0.795	0.235 0.225	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT467C						~~99-12-06~~ 99-12-28

Fig 11. Package outline SOT467C

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDMA	Code Division Multiple Access
EDGE	Enhanced Data rates for the GSM Evolution
GSM	Global System for Mobile communications
HF	High Frequency
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
PHS	Personal HandyPhone System
RF	Radio Frequency
SMD	Surface-Mount Device
UHF	Ultra High Frequency
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF3G21-30_1	20070214	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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