BUK7226-75A

N-channel TrenchMOS standard level FET

Rev. 02 — 22 February 2008 **Product data sheet**

1. Product profile

1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using NXP General Purpose Automotive (GPA) TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features

- 175 °C rated
- Q101 compliant
- Low on-state resistance
- Standard level compatible

1.3 Applications

- 12 V, 24 V and 42 V loads
- General purpose power switching
- Automotive systems
- Motors, lamps and solenoids

1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	-	75	V
I_D	drain current	$V_{GS} = 10$ V; $T_{mb} = 25$ °C; see Figure 1 and 4	[1]	-	-	45	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2		-	-	158	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 25$ A; $T_j = 25$ °C; see Figure 12 and 13		-	22	26	mΩ
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 45$ A; $V_{sup} \leq 75$ V; $R_{GS} = 50$ Ω; $V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; unclamped inductive load		-	-	215	mJ

[1] Capped at 45 A due to bondwire.

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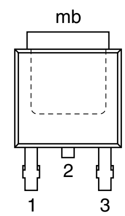
2. Pinning information

Table 2. Pinning

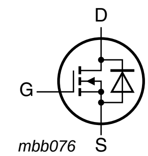
Pin	Symbol	Description
1	G	gate
2	D	drain
3	S	source
mb	D	mounting base; connected to drain

Simplified outline



SOT428 (DPAK)

Graphic symbol



3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7226-75A	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

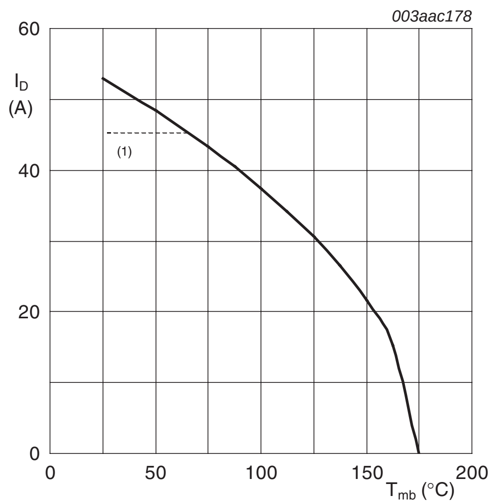
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	75	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20$ kΩ		-	75	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$T_{mb} = 25$ °C; $V_{GS} = 10$ V; see Figure 1 and 4	[1]	-	45	A
		$T_{mb} = 100$ °C; $V_{GS} = 10$ V; see Figure 1		-	38	A
I_{DM}	peak drain current	$T_{mb} = 25$ °C; $t_p \leq 10$ µs; pulsed; see Figure 4		-	215	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2		-	158	W
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 45$ A; $V_{sup} \leq 75$ V; $R_{GS} = 50$ Ω; $V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; unclamped inductive load		-	215	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	see Figure 3	[2][3][4]	-	-	J
Source-drain diode						
I_S	source current	$T_{mb} = 25$ °C	[1]	-	45	A
I_{SM}	peak source current	$t_p \leq 10$ µs; pulsed; $T_{mb} = 25$ °C		-	215	A

[1] Capped at 45 A due to bondwire.

[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

[3] Repetitive avalanche rating limited by an average junction temperature of 170 °C.

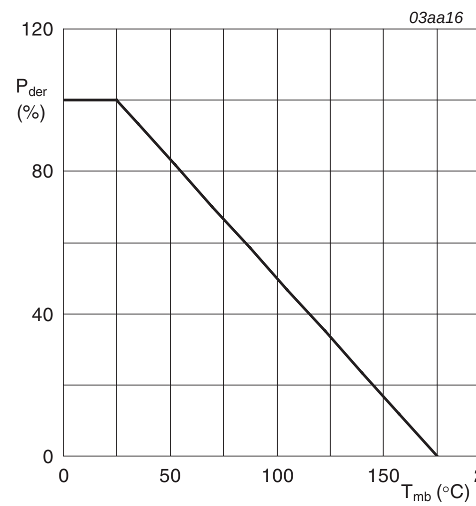
[4] Refer to application note AN10273 for further information.



$V_{GS} \geq 10 V$

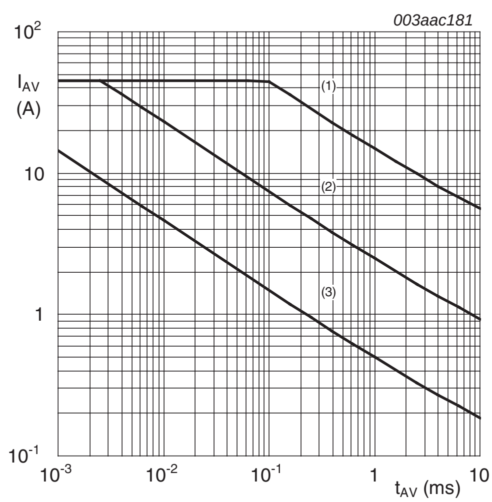
(1) Capped at 45 A due to bondwire.

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature

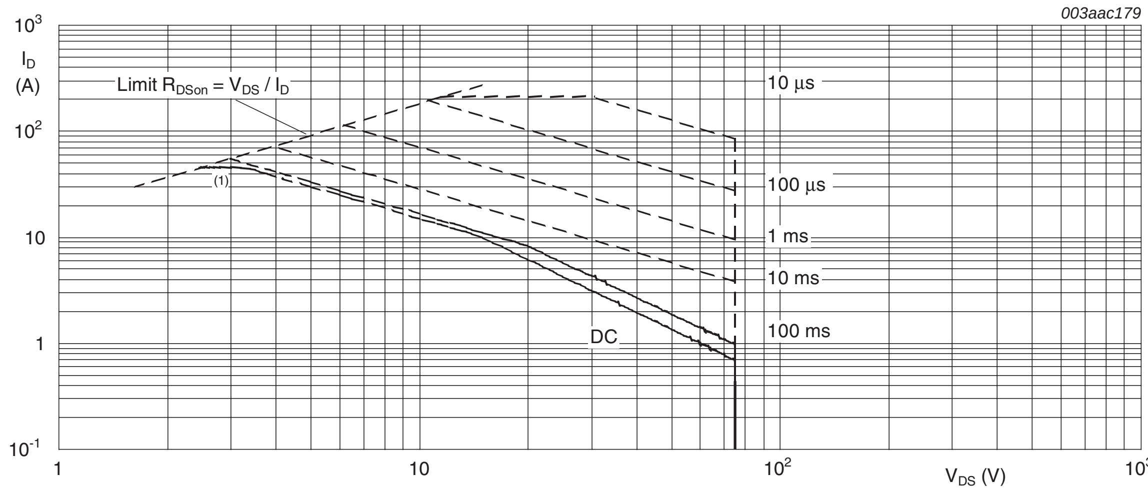


(1) Single−pulse; $T_j = 25\ °C$.

(2) Single−pulse; $T_j = 150\ °C$.

(3) Repetitive.

Fig 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time



T_{mb} = 25 °C; I_{DM} is single pulse

(1) Capped at 45 A due to bondwire.

Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; FR4 board	-	70	-	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	-	1	K/W

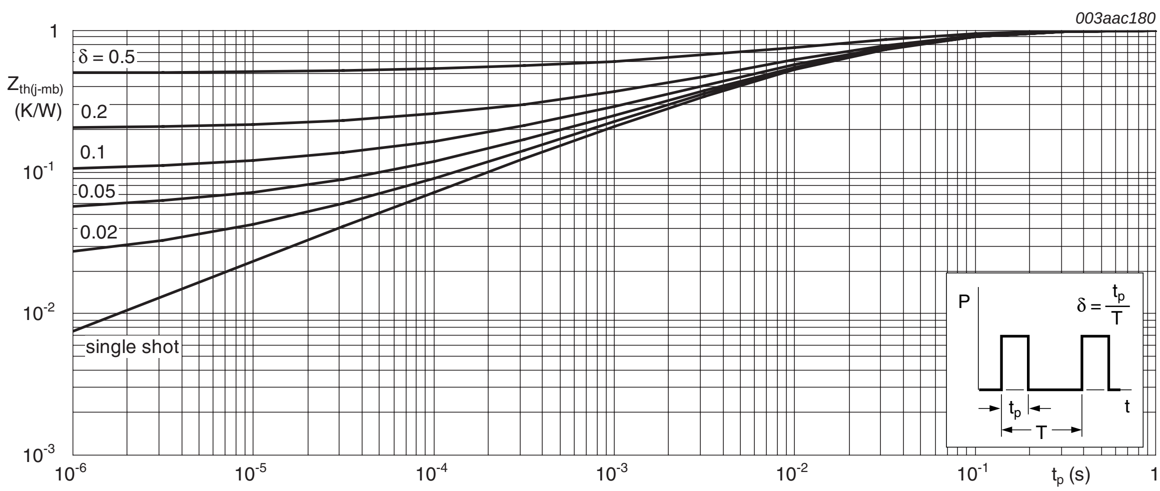


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

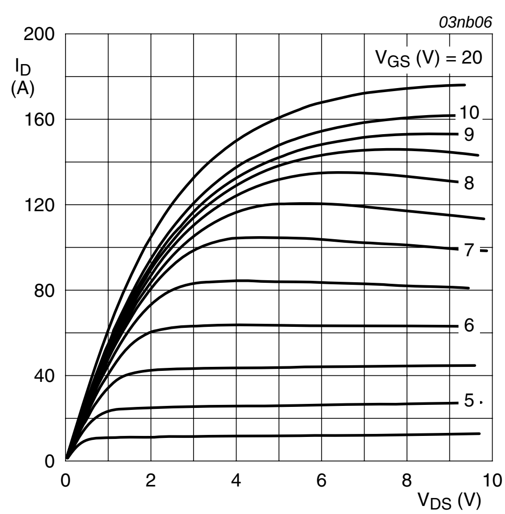
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V; T_j = -55 °C	70	-	-	V
		I_D = 0.25 mA; V_{GS} = 0 V; T_j = 25 °C	75	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; see Figure 11	1	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 11	2	3	4	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 11	-	-	4.4	V
I_{DSS}	drain leakage current	V_{DS} = 75 V; V_{GS} = 0 V; T_j = 25 °C	-	0.05	10	µA
		V_{DS} = 75 V; V_{GS} = 0 V; T_j = 175 °C	-	-	500	µA
I_{GSS}	gate leakage current	V_{DS} = 0 V; V_{GS} = 20 V; T_j = 25 °C	-	2	100	nA
		V_{DS} = 0 V; V_{GS} = -20 V; T_j = 25 °C	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; see Figure 12 and 13	-	-	54	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see Figure 12 and 13	-	22	26	mΩ
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 16	-	0.85	1.2	V

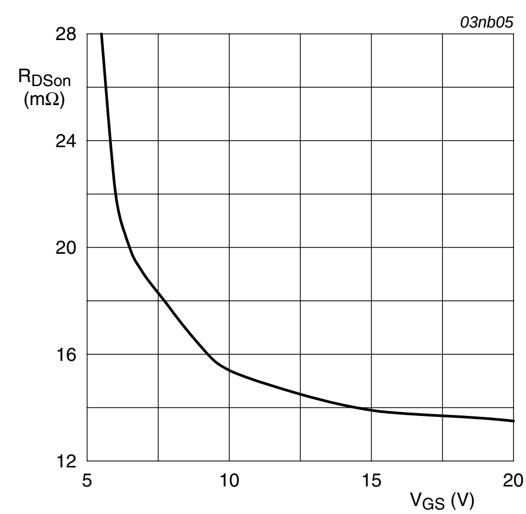
Table 6. Characteristics *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = -10 V; V_{DS} = 30 V; T_j = 25 °C	-	53	-	ns
Q_r	recovered charge		-	144	-	nC
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 60 V; V_{GS} = 10 V; see Figure 14	-	48	-	nC
Q_{GS}	gate-source charge		-	7.5	-	nC
Q_{GD}	gate-drain charge		-	17	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; see Figure 15	-	1789	2385	pF
C_{oss}	output capacitance		-	382	458	pF
C_{rss}	reverse transfer capacitance		-	219	300	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 10 Ω; T_j = 25 °C	-	14	-	ns
t_r	rise time		-	66	-	ns
$t_{d(off)}$	turn-off delay time		-	61	-	ns
t_f	fall time		-	41	-	ns
L_D	internal drain inductance	measured from drain lead from package to center of die; T_j = 25 °C	-	2.5	-	nH
L_S	internal source inductance	measured from source lead from package to source bond pad; T_j = 25 °C	-	7.5	-	nH



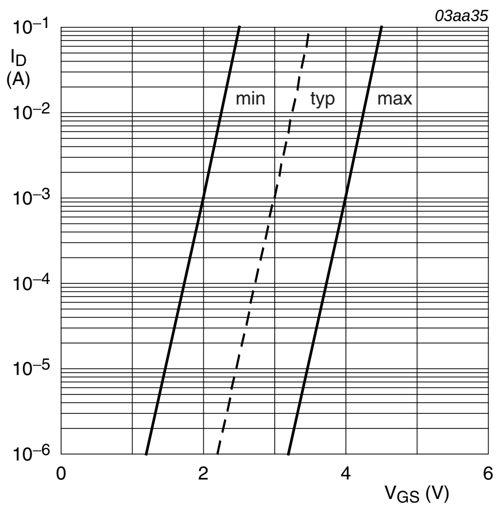
T_j = 25 °C; t_p = 300 µs

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



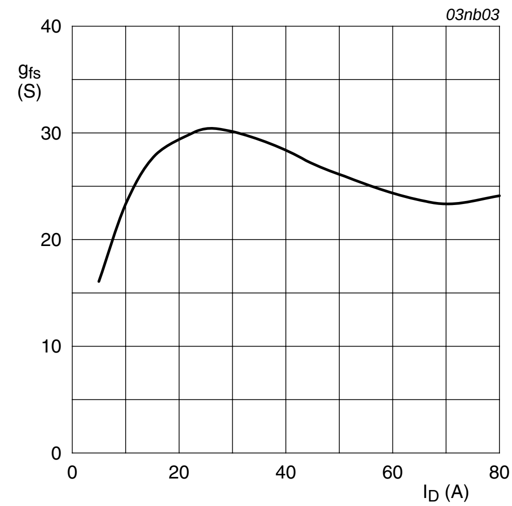
T_j = 25 °C; I_D = 25 A

Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



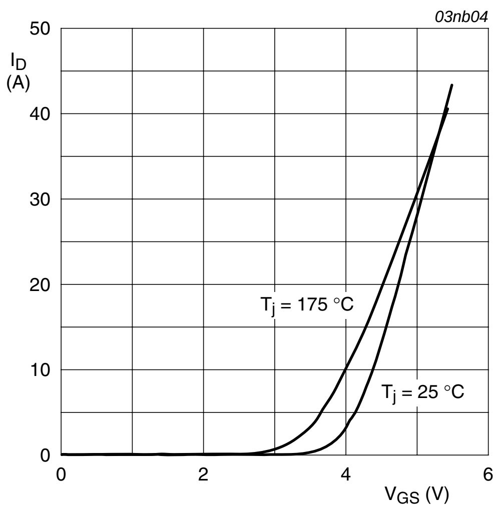
$T_j = 25\ °C; V_{DS} = V_{GS}$

Fig 8. Sub-threshold drain current as a function of gate-source voltage



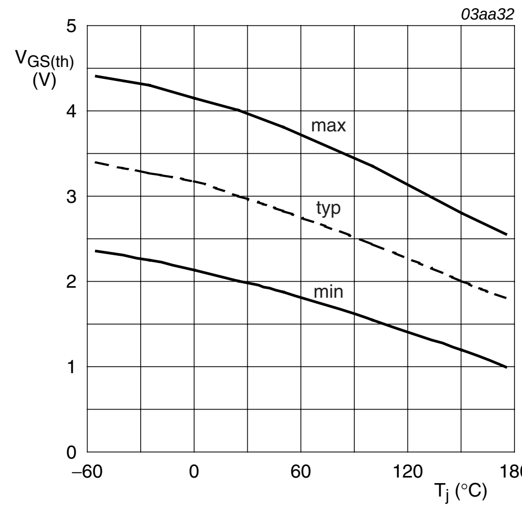
$T_j = 25\ °C; V_{DS} = 25\ V$

Fig 9. Forward transconductance as a function of drain current; typical values



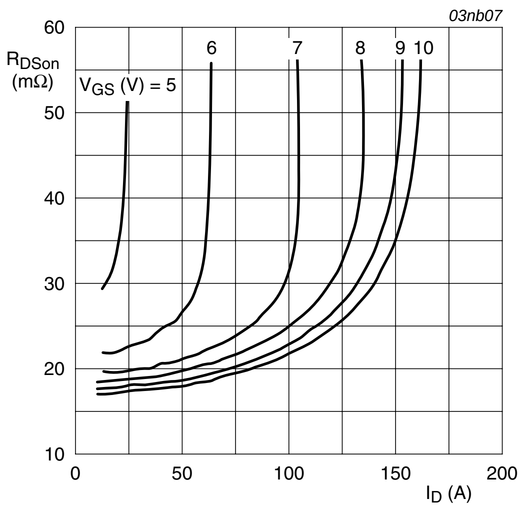
$V_{DS} = 25\ V$

Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



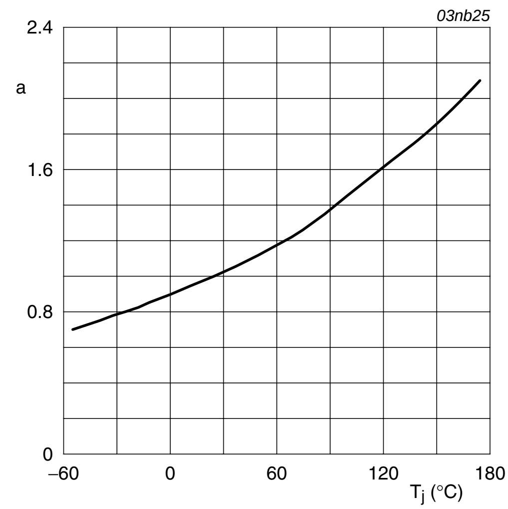
$I_D = 1\ mA; V_{DS} = V_{GS}$

Fig 11. Gate-source threshold voltage as a function of junction temperature



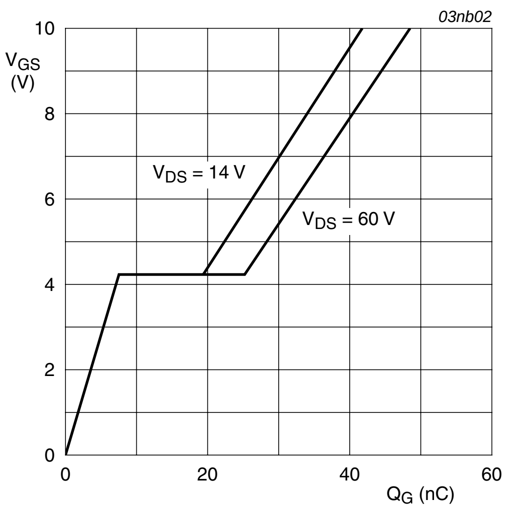
$T_j = 25\,°C$

Fig 12. Drain-source on-state resistance as a function of drain current; typical values



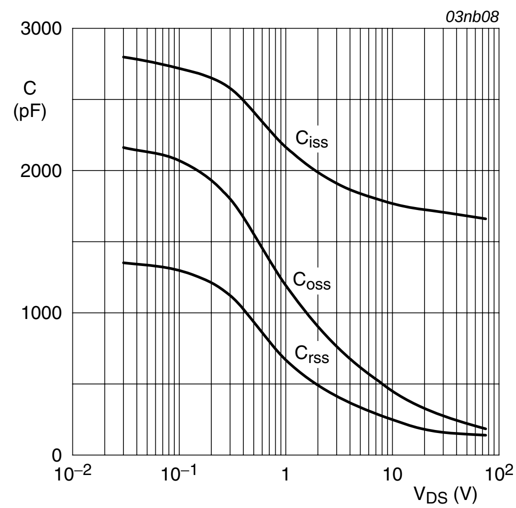
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature



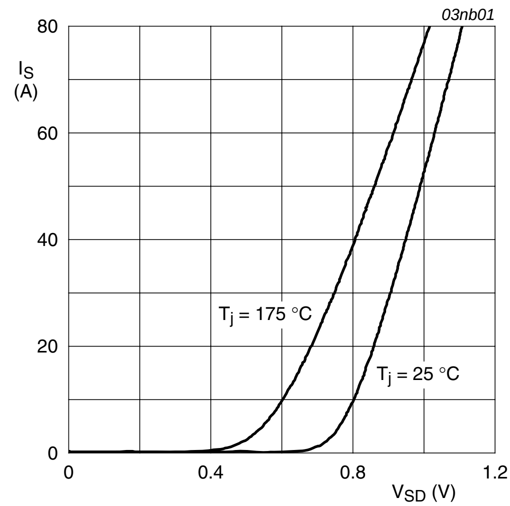
$T_j = 25\,°C;\ I_D = 25\,A$

Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values



$V_{GS} = 0\,V;\ f = 1\,MHz$

Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

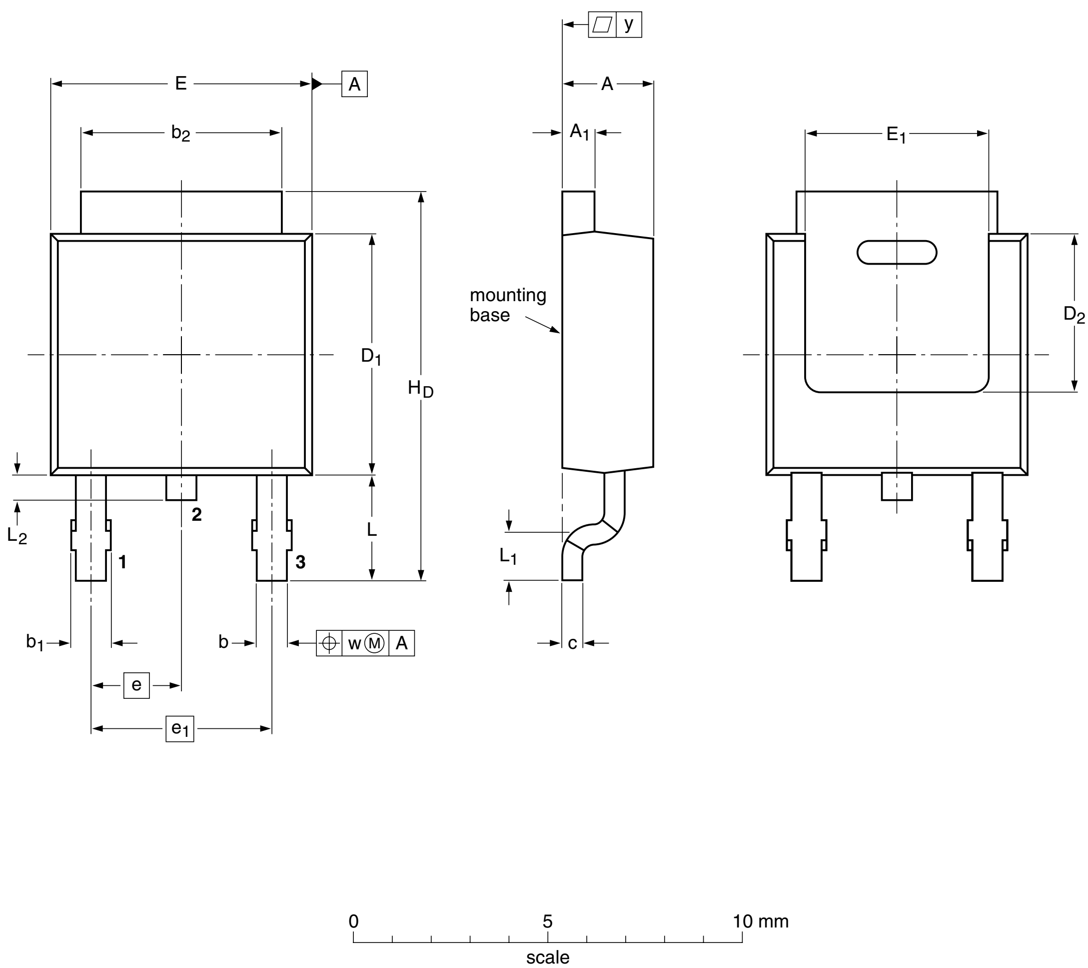


$V_{GS} = 0\,V$

Fig 16. Reverse diode current; typical values

7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) **SOT428**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D_1	D_2 min	E	E_1 min	e	e_1	H_D	L	L_1 min	L_2	w	y max
mm	2.38 2.22	0.93 0.46	0.89 0.71	1.1 0.9	5.46 5.00	0.56 0.20	6.22 5.98	4.0	6.73 6.47	4.45	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.9 0.5	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT428		TO-252	SC-63			~~06-02-14~~ 06-03-16

Fig 17. Package outline SOT428 (DPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK7226-75A_2	20080222	Product data sheet	-	BUK7226_75A-01
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
BUK7226_75A-01	20001009	Product specification; initial version		-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Date of release: 22 February 2008
Document identifier: BUK7226-75A_2