



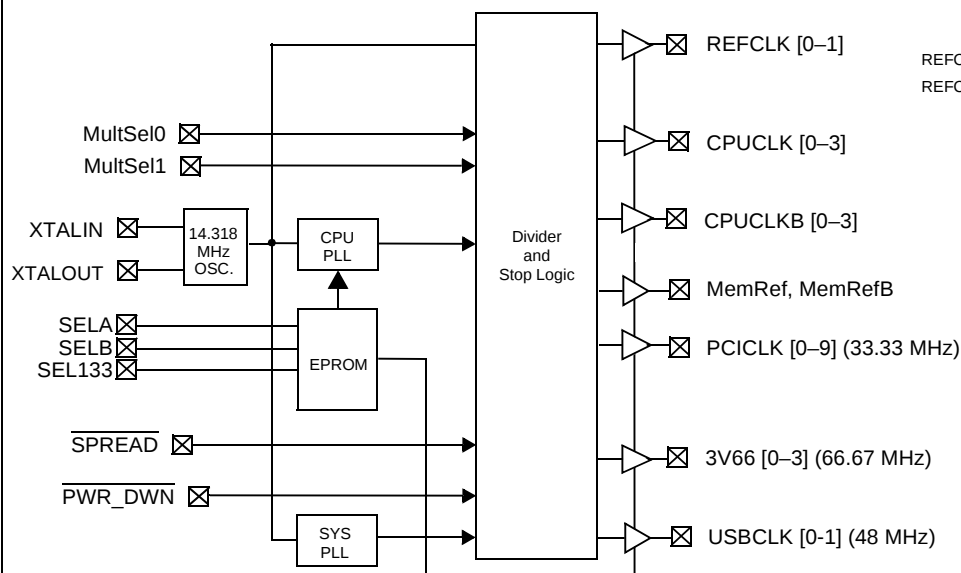
CYPRESS

CY2220

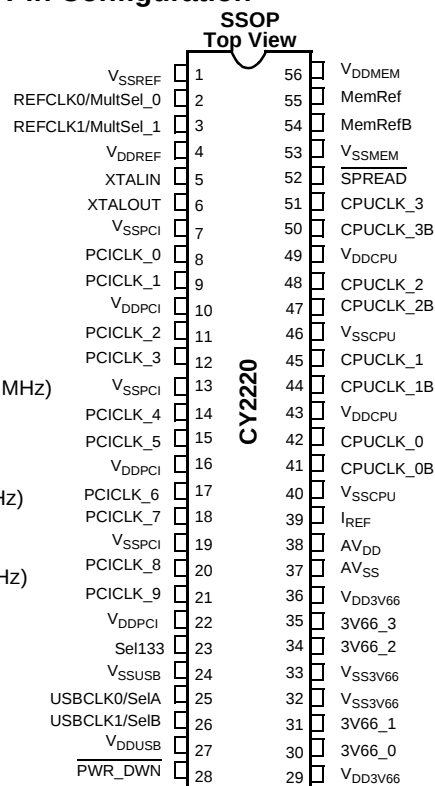
133-MHz Spread Spectrum Clock Synthesizer/Driver with Differential CPU Outputs

Features	Benefits
• Compliant to Intel® CK00 Clock Synthesizer/Driver Specifications	Supports next generation Pentium® processors using differential clock drivers
• Multiple output clocks at different frequencies — Four pairs of differential CPU outputs, up to 133 MHz — Ten synchronous PCI clocks — Two Memory Reference clocks, 180 degrees out of phase — Four AGP and Hub Link clocks at 66 MHz — Two 48-MHz clocks — Two reference clocks at 14.318 MHz	Motherboard clock generator — Support Multiple CPUs and a chipset — Support for PCI slots and chipset — Drives up to two Direct Rambus™ Clock Generators (DRCG) — Supports USB host controller and SuperI/O chip — Supports ISA slots and I/O chip
• Spread Spectrum clocking — 31 kHz modulation frequency — Default is -0.6%, which is recommended by Intel	Enables reduction of EMI and overall system cost
• Power-down features	Enables ACPI compliant designs
• Three Select inputs	Supports up to eight CPU clock frequencies
• Low-skew and low-jitter outputs	Meets tight system timing requirements at high frequency
• OE and Test Mode support	Enables ATE and “bed of nails” testing
• 56-pin SSOP package	Widely available, standard package enables lower cost

Logic Block Diagram



Pin Configuration



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Pin Summary

Name	Pins	Description
V _{SSREF}	1	3.3V Reference ground
V _{DDREF}	4	3.3V Reference voltage supply
V _{SSPCI}	7, 13, 19	3.3V PCI ground
V _{DDPCI}	10, 16, 22	3.3V PCI voltage supply
V _{SS3V66}	32, 33	3.3V AGP and Hub Link ground
V _{DD3V66}	29, 36	3.3V AGP and Hub Link voltage supply
V _{SSUSB}	24	3.3V USB ground
V _{DDUSB}	27	3.3V USB voltage supply
V _{SSCPU}	40, 46	3.3V CPU ground
V _{DDCPU}	43, 49	3.3V CPU voltage supply
V _{SSMEM}	53	3.3V Memory ground
V _{DDMEM}	56	3.3V Memory voltage supply
AV _{SS}	37	Analog ground for PLL and Core
AV _{DD}	38	Analog voltage supply to PLL and Core
I _{REF}	39	Reference current for external biasing
XTALIN ^[1]	5	Reference crystal input
XTALOUT ^[1]	6	Reference crystal feedback
CPUCLK [0–3]	42, 45, 48, 51	CPU clock outputs
CPUCLK [0–3]B	41, 44, 47, 50	Inverse CPU clock outputs
PCICLK [0–9]	8, 9, 11, 12, 14, 15, 17, 18, 20, 21	PCI clock outputs, synchronously running at 33.33 MHz
MemRef	55	MemRef clock output, drives memory clock generator
MemRefB	54	MemRefB clock output 180 degrees out of phase with MemRef
3V66_ [0–3]	30, 31, 34, 35	AGP and Hub Link clock outputs, running at 66 MHz
USBCLK [0–1]/Sel[A–B]	25, 26	Sel [A–B] inputs are sensed then internally latched on power-up before the pins are used for 48-MHz USB clock outputs
REFCLK[0–1]/MultSel[0–1]	2, 3	MultSel[0–1] inputs are sensed then internally latched on power-up before the pins are Reference clock outputs, 14.318 MHz
PWR_DWN	28	Active LOW input, powers down part when asserted
SPREAD ^[2]	52	Active LOW input, enables spread spectrum when asserted
SEL133	23	CPU frequency select input (See Function Table)

Notes:

- For best accuracy, use a parallel-resonant crystal, C_{LOAD} = 18 pF. For crystals with different C_{LOAD}, please refer to the application note, "Crystal Oscillator Topics."
- Input is static HIGH or LOW. Frequency of toggling cannot exceed 30 MHz.

Function Table^[3]

SEL133	SELA	SELB	CPUCLK (MHz)	MemRef (MHz)	3V66CLK (MHz)	PCICLK (MHz)	USBCLK (MHz)	REFCLK (MHz)
0	0	0	100	50	66	33	48	14.318
0	0	1	N/A	N/A	N/A	N/A	N/A	N/A
0	1	0	N/A	N/A	N/A	N/A	N/A	N/A
0	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1	0	0	133	66	66	33	48	14.318
1	0	1	N/A	N/A	N/A	N/A	N/A	N/A
1	1	0	N/A	N/A	N/A	N/A	N/A	N/A
1	1	1	TCLK/2	TCLK/4	TCLK/4	TCLK/8	TCLK/2	TCLK

Actual Clock Frequency Values

Clock Output	Target Frequency (MHz)	CY2220-1		CY2220-2	
		Actual Frequency (MHz)	PPM	Actual Frequency (MHz)	PPM
CPUCLK	100	99.126	-8741	100.227	+2270
CPUCLK	133	132.769	-1740	133.269	+2022
USBCLK	48	48.008	167	48.008	167

Swing Select Functions

MultSel0	MultSel1	Board Target	Reference R, I _{REF} =	Output Current	V _{OH} @ Z, I _{ref} = 2.32 mA
0	0	60Ω	R _r = 475 ± 1%, I _{ref} = 2.32 mA	I _{OH} = 5*I _{ref}	0.71 @ 60
0	0	50Ω	R _r = 475 ± 1%, I _{ref} = 2.32 mA	I _{OH} = 5*I _{ref}	0.59 @ 50
0	1	60Ω	R _r = 475 ± 1%, I _{ref} = 2.32 mA	I _{OH} = 6*I _{ref}	0.85 @ 60
0	1	50Ω	R _r = 475 ± 1%, I _{ref} = 2.32 mA	I _{OH} = 6*I _{ref}	0.71 @ 50
1	0	60Ω	R _r = 475 ± 1%, I _{ref} = 2.32 mA	I _{OH} = 4*I _{ref}	0.56 @ 60
1	0	50Ω	R _r = 475 ± 1%, I _{ref} = 2.32 mA	I _{OH} = 4*I _{ref}	0.47 @ 50
1	1	60Ω	R _r = 475 ± 1%, I _{ref} = 2.32 mA	I _{OH} = 7*I _{ref}	0.99 @ 60
1	1	50Ω	R _r = 475 ± 1%, I _{ref} = 2.32 mA	I _{OH} = 7*I _{ref}	0.82 @ 50

Clock Driver Impedances

Buffer Name	V _{DD} Range	Buffer Type	Impedance		
			Minimum Ω	Typical Ω	Maximum Ω
CPUCLK, CPUCLKB		Type X1			
USB, REF	3.135–3.465	Type 3	20	40	60
PCI, 3V66	3.135–3.465	Type 5	12	30	55
MemRef, MemRefB	3.135–3.465	Type 5	12	30	55

Note:

3. TCLK is a test clock driven in on the XTALIN input in test mode.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage.....–0.5 to +7.0V
 Input Voltage.....–0.5V to $V_{DD} + 0.5$

Storage Temperature (Non-Condensing).....–65°C to +150°C

Junction Temperature.....
 +150°C

Package Power Dissipation.....1W

Static Discharge Voltage
 (per JEDEC EIA/JESD22-A114-A).....2000V

Operating Conditions Over which Electrical Parameters are Guaranteed

Parameter	Description	Min.	Max.	Unit
V_{DDREF} , V_{DDPCI} , AV_{DD} , V_{DD3V66} , V_{DDUSB} , V_{DDCPU} , V_{DDMEM}	3.3V Supply Voltages	3.135	3.465	V
T_A	Operating Temperature, Ambient	0	70	°C
C_{in}	Input Pin Capacitance Nominal Value	18 pF	18 pF	pF
C_{XTAL}	XTAL Pin Capacitance		22.5	pF
C_L	Max. Capacitive Load on MemRef, USBCLK, REF PCICLK, 3V66		20 30	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz
t_{PU}	Power-up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Pads. Threshold voltage for crystal pads = $V_{DD}/2$		2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Pads			0.8	V
V_{OH}	High-level Output Voltage	MemRef, USB, REF, 3V66	$I_{OH} = -1$ mA	2.4		V
		PCI	$I_{OH} = -1$ mA	2.4		V
V_{OL}	Low-level Output Voltage	MemRef, USB, REF, 3V66	$I_{OL} = 1$ mA		0.4	V
		PCI	$I_{OL} = 1$ mA		0.55	V
I_{IH}	Input High Current	$0 \leq V_{IN} \leq V_{DD}$		–5	5	μA
I_{IL}	Input Low Current	$0 \leq V_{IN} \leq V_{DD}$		–5	5	μA
I_{OH}	High-level Output Current	CPU For $I_{OH} = 6 \cdot I_{Ref}$ Configuration	Type X1, $V_{OH} = 0.65V$	–12.9	–14.9	mA
		USB, REF	Type 3, $V_{OH} = 2.4V$	–15	–51	
		3V66, PCI, MemRef, MemRefB	Type 5, $V_{OH} = 2.4V$	–30	–100	
I_{OL}	Low-level Output Current	USB, REF	Type 3, $V_{OL} = 0.4V$	10	24	mA
		3V66, PCI, MemRef, MemRefB	Type 5, $V_{OL} = 0.4V$	20	49	
I_{OZ}	Output Leakage Current	Three-state			10	μA
I_{DD3}	3.3V Power Supply Current	$AV_{DD}/V_{DD33} = 3.465V$, $F_{CPU} = 133$ MHz			250	mA
I_{DDPD3}	3.3V Shutdown Current	$AV_{DD}/V_{DDQ3} = 3.465V$			60	mA

Switching Characteristics^[4] Over the Operating Range

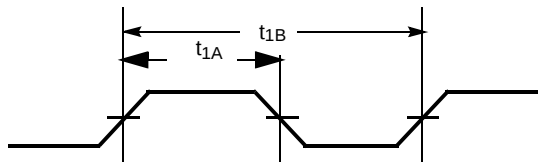
Parameter	Output	Description	Test Conditions	Min.	Max.	Unit
t_1	All	Output Duty Cycle ^[5]	$t_{1A}/(t_{1B})$	45	55	%
t_2	CPU	Rise Time	Measured at 20% to 80% of V_{OH}	175	700	ps
t_2	USB, REF	Rising Edge Rate	Between 0.4V and 2.4V	0.5	2.0	V/ns
t_2	PCI, 3V66, MemRef	Rising Edge Rate	Between 0.4V and 2.4V	1.0	4.0	V/ns
t_3	CPU	Fall Time	Measured at 80% to 20% of V_{OH}	175	700	ps
t_3	USB, REF	Falling Edge Rate	Between 2.4V and 0.4V	0.5	2.0	V/ns
t_3	PCI, 3V66, MemRef	Falling Edge Rate	Between 2.4V and 0.4V	1.0	4.0	V/ns
t_4	CPU	CPU-CPU Skew	Measured at Crossover		150	ps
t_5	3V66	3V66-3V66 Skew	Measured at 1.5V		250	ps
t_6	PCI	PCI-PCI Skew	Measured at 1.5V		500	ps
t_7	3V66, PCI	3V66-PCI Clock Skew	3V66 leads. Measured at 1.5V	1.5	3.5	ns
t_8	CPU	Cycle-Cycle Clock Jitter	Measured at Crossover $t_8 = t_{8A} - t_{8B}$ With all outputs running		200	ps
t_9	Mref	Cycle-Cycle Clock Jitter	Measured at 1.5V $t_9 = t_{9A} - t_{9B}$		250	ps
t_9	3V66	Cycle-Cycle Clock Jitter	Measured at 1.5V $t_9 = t_{9A} - t_{9B}$		300	ps
t_9	USB	Cycle-Cycle Clock Jitter	Measured at 1.5V $t_9 = t_{9A} - t_{9B}$		350	ps
t_9	PCI	Cycle-Cycle Clock Jitter	Measured at 1.5V $t_9 = t_{9A} - t_{9B}$		500	ps
t_9	REF	Cycle-Cycle Clock Jitter	Measured at 1.5V $t_9 = t_{9A} - t_{9B}$		1000	ps
	CPU, PCI	Settle Time	CPU and PCI clock stabilization from power-up		3	ms
	CPU	Rise/Fall Matching	Measured with test loads ^[6, 7]		20%	
	CPU	Overshoot	Measured with test loads ^[7]		$V_{OH} + 0.2$	V
	CPU	Undershoot	Measured with test loads ^[7]	-0.2		V
V_{oh}	CPU	High-level Output Voltage	Measured with test loads ^[7]	0.65	0.74	V
V_{ol}	CPU	Low-level Output Voltage	Measured with test loads ^[7]	0.0	0.05	V
$V_{crossover}$	CPU	Crossover Voltage	Measured with test loads ^[7]	45% of V_{OH}	55% of V_{OH}	V

Notes:

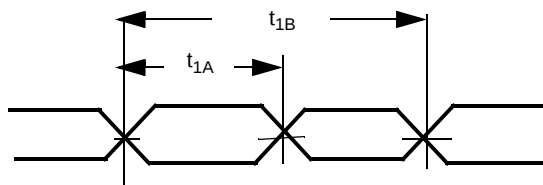
4. All parameters specified with loaded outputs. Parameters not tested in production, but are guaranteed by design characterization.
5. Duty cycle is measured at 1.5V with V_{DD} at 3.3V on all output except CPU. Duty Cycle on CPU is measured at $V_{crossover}$.
6. Determined as a fraction of $2*(t_{RP} - t_{RN})/(t_{RP} + t_{RN})$ Where t_{RP} is a rising edge and t_{RN} is an intersecting falling edge.
7. The test load is specified in test circuit.

Switching Waveforms

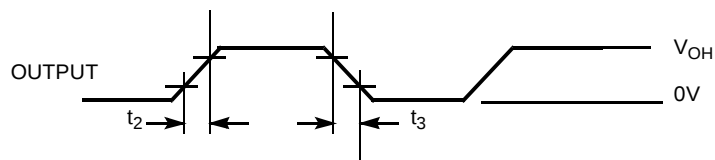
Duty Cycle Timing (Single Ended Output)



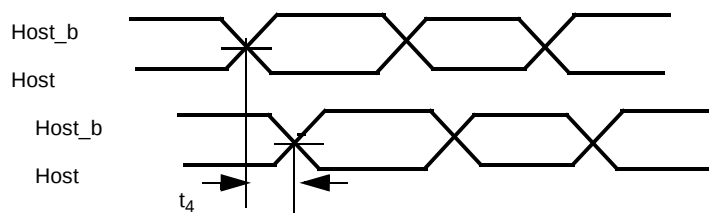
Duty Cycle Timing (CPU Differential Output)



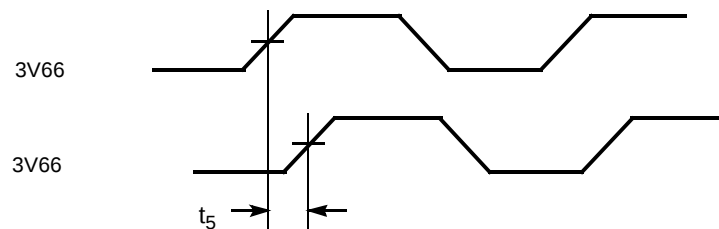
All Outputs Rise/Fall Time



CPU-CPU Clock Skew

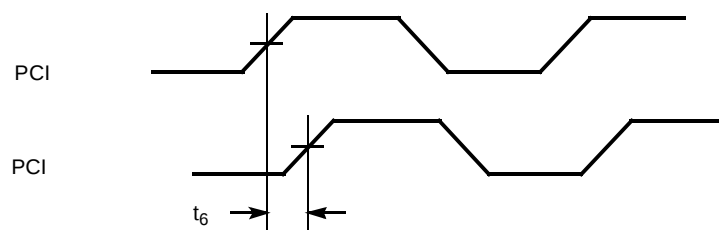


3V66-3V66 Clock Skew

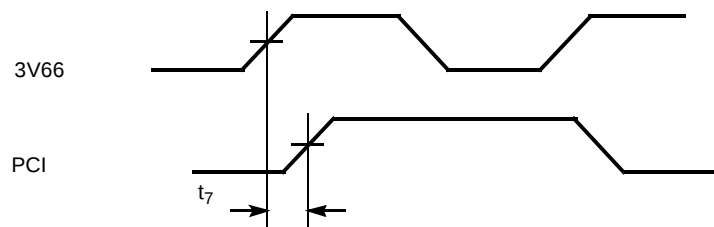


Switching Waveforms (continued)

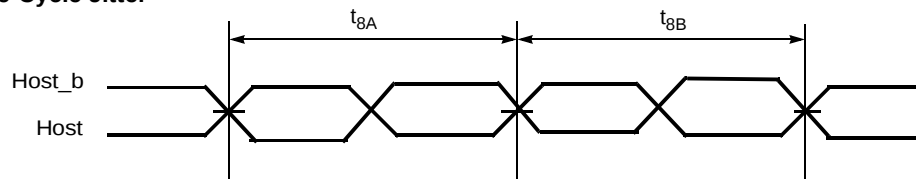
PCI-PCI Clock Skew



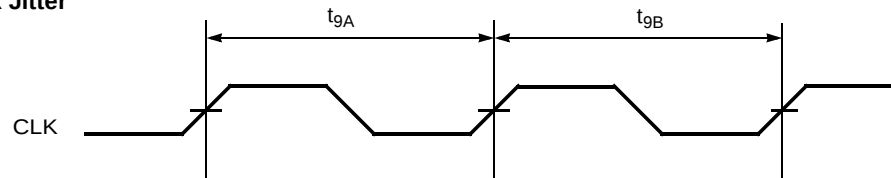
3V66-PCI Clock Skew



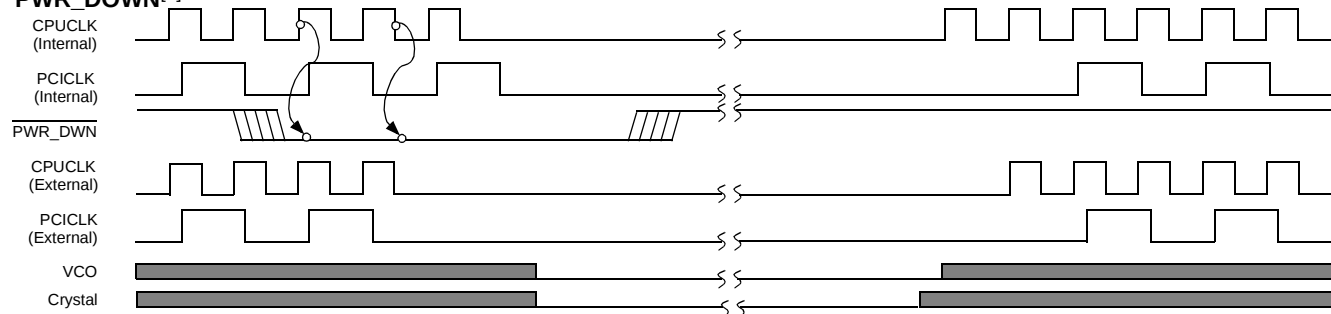
CPU Clock Cycle-Cycle Jitter



Cycle-Cycle Clock Jitter

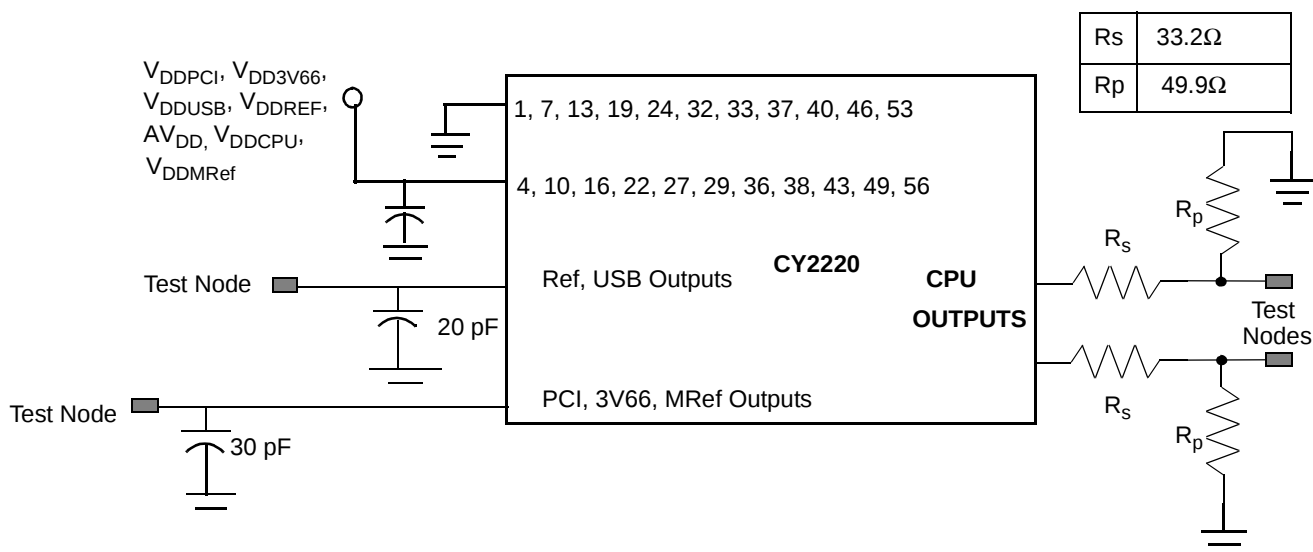


PWR_DOWN^[8]



Note:

8. Shaded section on the VCO and Crystal waveforms indicates that the VCO and crystal oscillator are active, and there is a valid clock.

Test Circuit^[9, 10]

Ordering Information

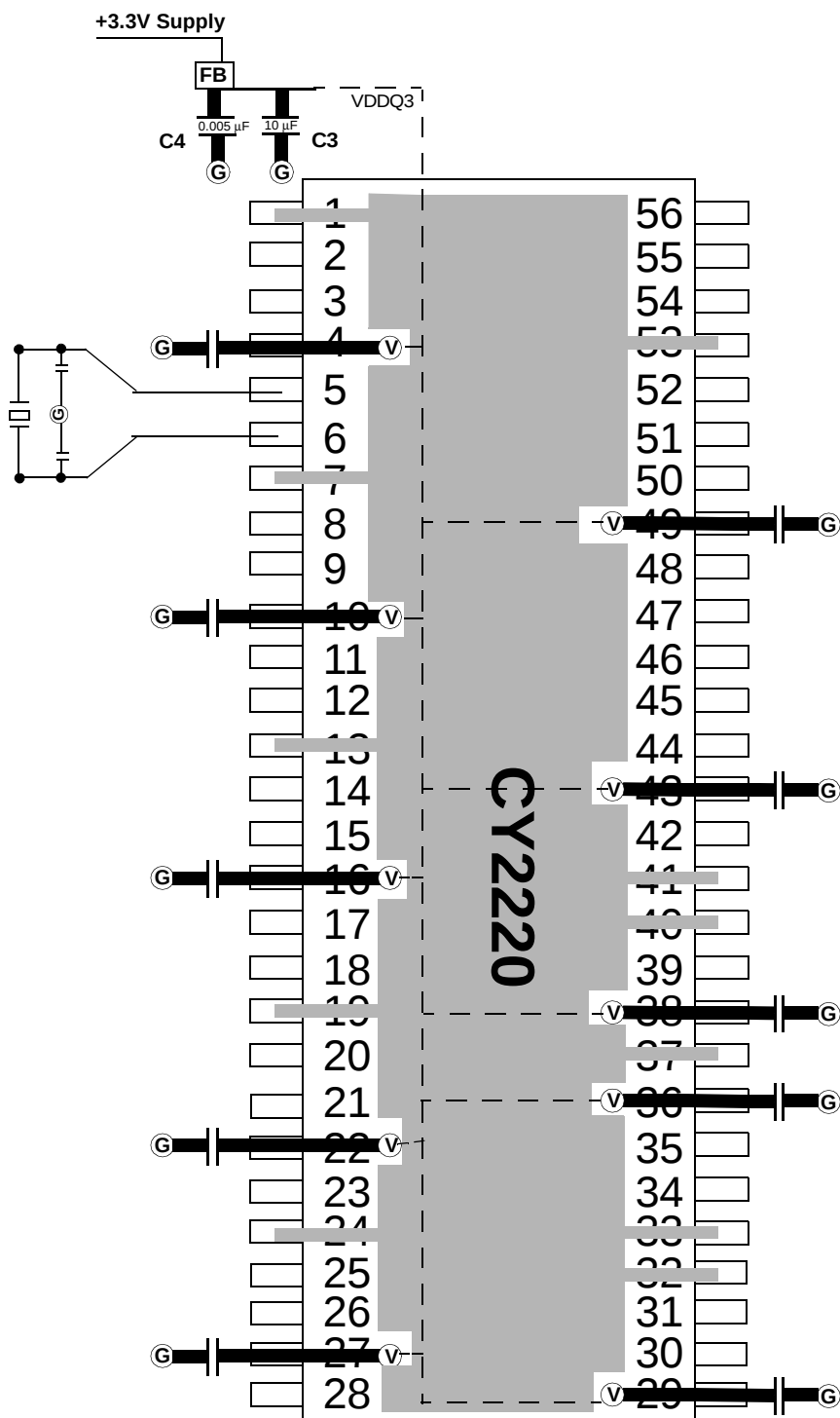
Ordering Code	Package Name	Package Type	Operating Range
CY2220PVC-1	O56	56-Pin SSOP	Commercial
CY2220PVC-2	O56	56-Pin SSOP	Commercial

Notes:

9. Each supply pin must have an individual decoupling capacitor.

10. All capacitors must be placed as close to the pins as is physically possible.

Layout Example



FB = Dale ILB1206 - 300 (30Ω @ 100 MHz)

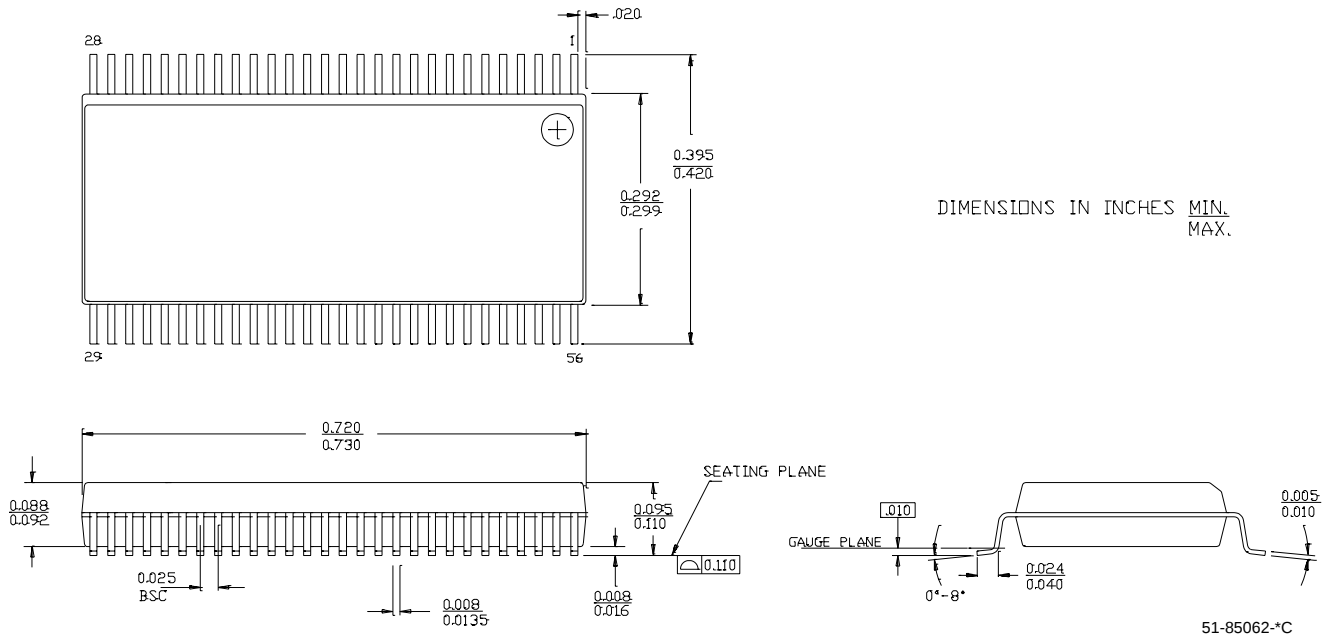
Ceramic Caps C3 = 10–22 µF C4 = 0.005 µF

⊗ = VIA to GND plane layer ⊕ = VIA to respective supply plane layer

Note: Each supply plane or strip should have a ferrite bead and capacitors
All bypass caps = 0.01 µF ceramic

Package Diagram

56-Lead Shrink Small Outline Package O56



Document Title: CY2220 133-MHz Spread Spectrum Clock Synthesizer/Driver with Differential CPU Outputs Document Number: 38-07206				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	111730	01/17/02	DSG	Change from Spec number: 38-00813 to 38-07206
*A	121841	12/30/02	RBI	Power up requirements added to Operating Conditions Information