

DC Brushless Motor Drivers for Cooling Fans

Two-Phase Half-Wave Pre Driver Fan Motor Driver


BA6506F
General description

BA6506F is two-phase half-wave fan motor pre-driver. This driver incorporates lock protection, automatic restart circuit and Rotation speed pulse signal (FG) output.

Package

SOP8

W (Typ.) x D (Typ.) x H (Max.)

5.00mm x 6.20mm x 1.71mm

Features

- Pre-driver
- Incorporates lock protection and automatic restart circuit
- Rotation speed pulse signal (FG) output



SOP8

Application

- For desktop PC, server, general consumer equipment, communication equipment and industrial equipment.

Absolute maximum ratings

Parameter	Symbol	Limit	Unit
Supply voltage	V _{cc}	30	V
Power dissipation	P _d	624 ^{*1}	mW
Operating temperature range	T _{opr}	-40 to +100	°C
Storage temperature range	T _{stg}	-55 to +125	°C
Output current	I _{omax}	70	mA
Rotation speed pulse signal (FG) output voltage	I _{FG}	8	mA
Rotation speed pulse signal (FG) output current	V _{FG}	30	V
Junction temperature	T _{jmax}	125	°C

*1 Reduce by 6.24mW/°C over T_a=25°C. (On 70.0mm×70.0mm×1.6mm glass epoxy board)

Recommended operating conditions

Parameter	Symbol	Limit	Unit
Operating supply voltage range	V _{cc}	4.0 to 28.0	V
Hall input voltage range	V _H	1.0 ~ V _{cc} -0.5	V

BA6506F

Pin configuration

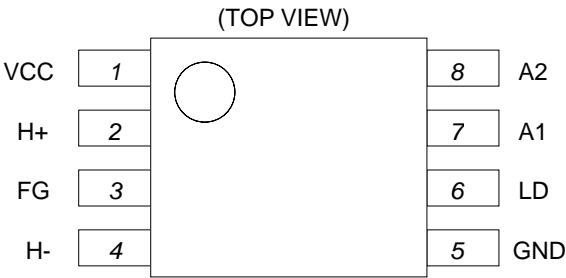


Fig.1 Pin configuration

Pin description

P/No.	T/Name	Function
1	Vcc	Power terminal
2	H+	Hall input terminal +
3	FG	Rotating speed pulse signal output terminal
4	H-	Hall input terminal -
5	GND	GND terminal
6	LD	Lock detection and automatic restart capacitor connecting terminal
7	A1	Output terminal 1
8	A2	Output terminal 2

Block diagram

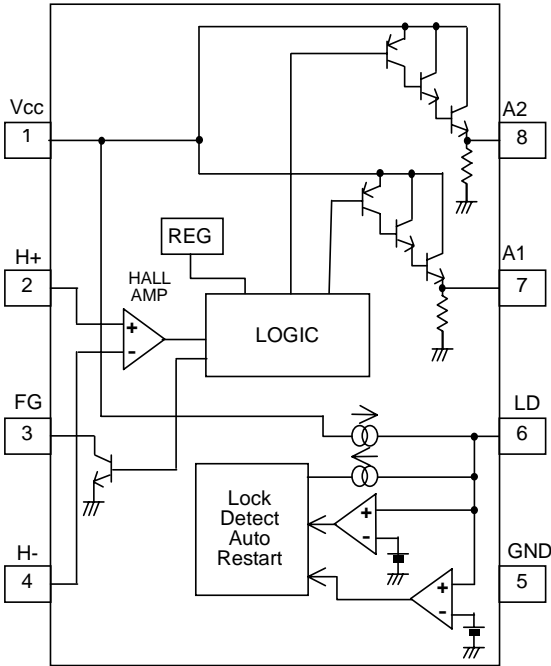


Fig.2 Block diagram

I/O truth table

H+	H-	A1	A2	FG
H	L	H (Output Tr ON)	L (Output Tr OFF)	H (Output Tr OFF)
L	H	L (Output Tr OFF)	H (Output Tr ON)	L (Output Tr ON)

H; High, L; Low, Hi-Z; High impedance
FG output is open-drain type.

Electrical characteristics(Unless otherwise specified Ta=25°C, Vcc=12V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Circuit current	Icc	-	3.2	5.0	mA	At output OFF
Hall input hysteresis	Vhys	± 3	-	±15	mV	
FG output L voltage	VFG	-	-	0.5	V	IFG=5mA
FG current capacity	IFG	8.0	-	-	mA	VFG=2V
Charge current of capacitor for lock detection	ILDC	2.0	3.45	5.25	μ A	VLD=1.5V
Discharge current of capacitor for lock detection	ILDD	0.35	0.80	1.45	μ A	VLD=1.5V
Charge-discharge current ratio of capacitor for lock detection	rCD	3	4.5	8	-	rCD=ILDC/ILDD
Clamp voltage of capacitor for lock detection	VLDCL	2.2	2.6	3.0	V	
Comparison voltage of capacitor for lock detection	VLDCL	0.4	0.6	0.8	V	
Output H voltage	VOH	10	10.5	-	V	I _o =10mA

Typical performance curves(Reference data)

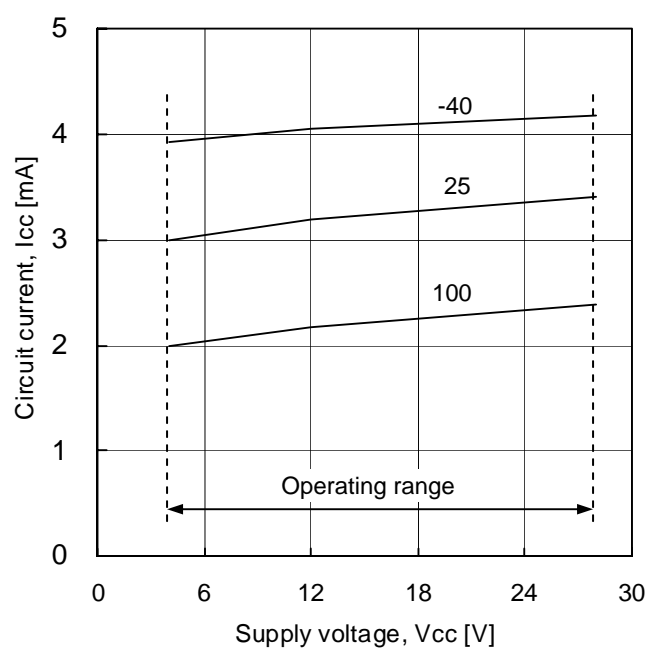


Fig.3 Circuit current

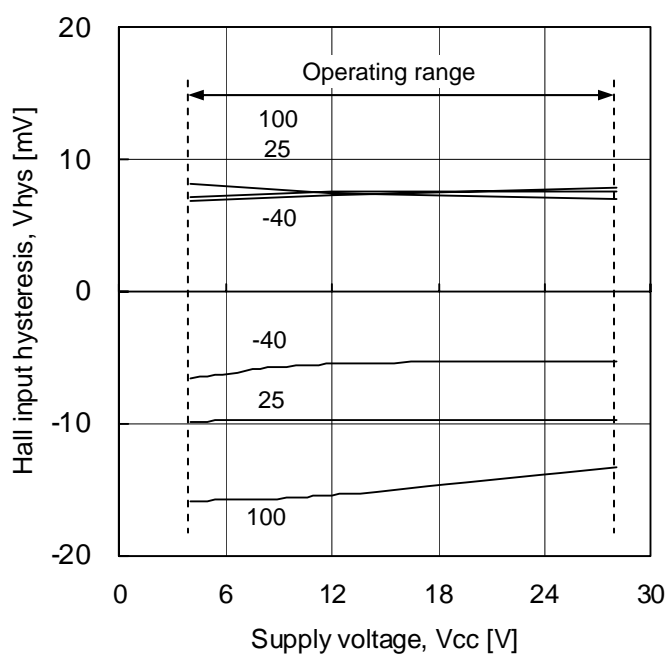


Fig.4 Hall input hysteresis

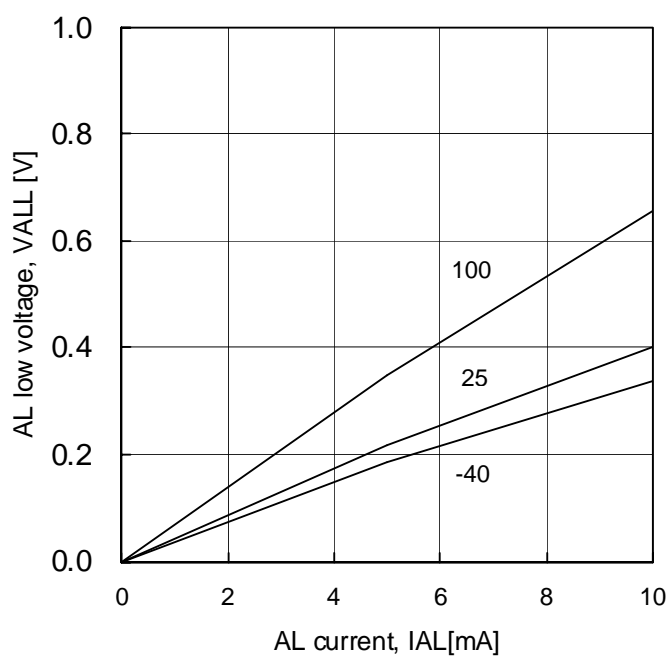


Fig.5 AL output L voltage

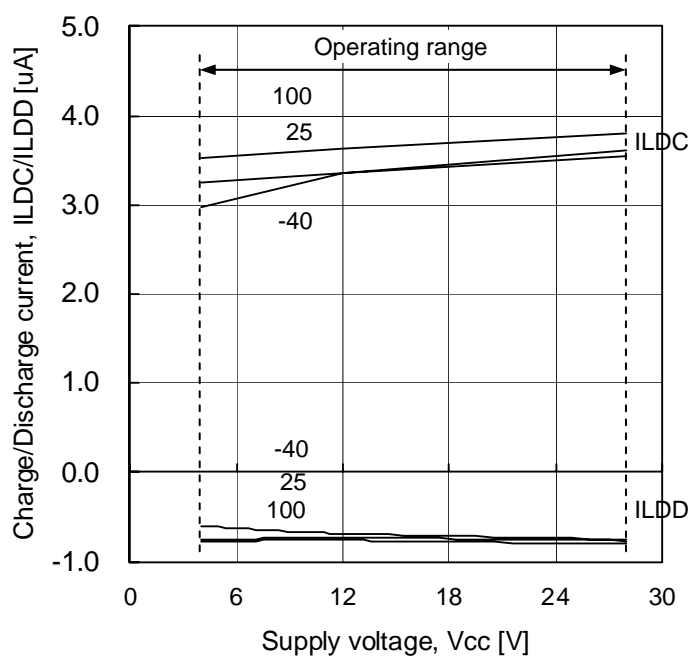


Fig.6 Charge-discharge current of capacitor for lock detection

Typical performance curves(Reference data)

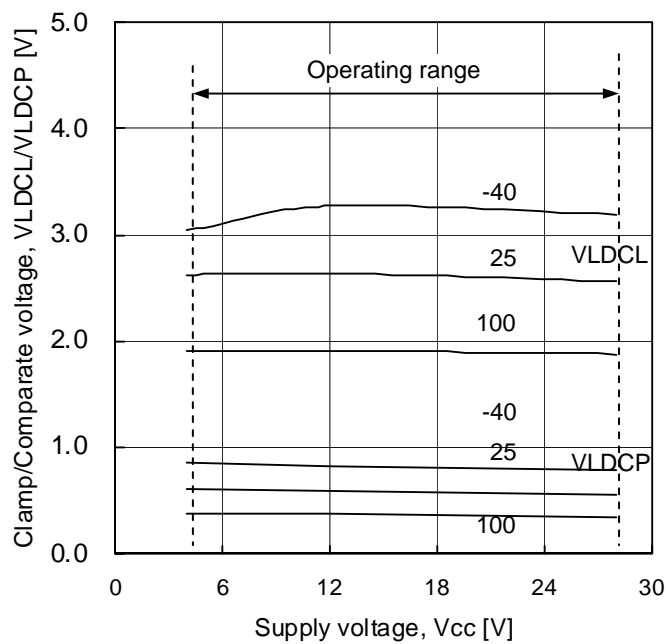


Fig.7 Clamp-compare voltage of capacitor for lock detection

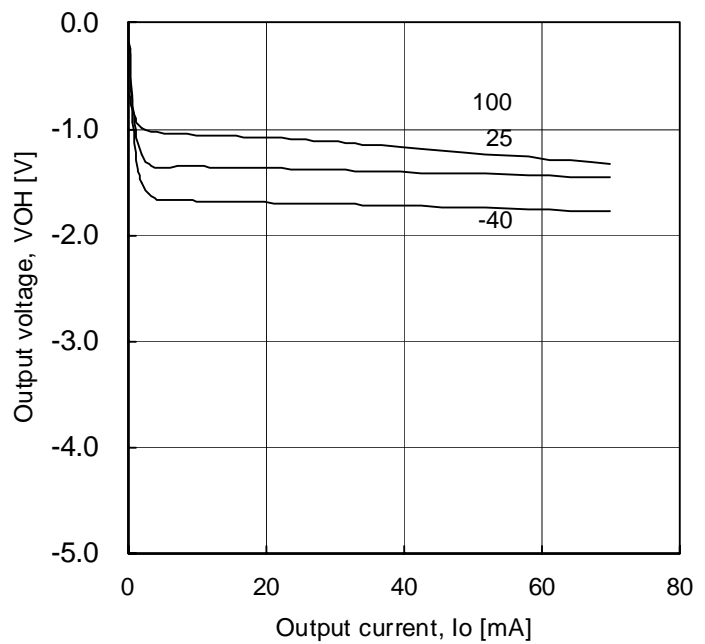


Fig.8 Output H voltage

Application circuit example(Constant values are for reference)

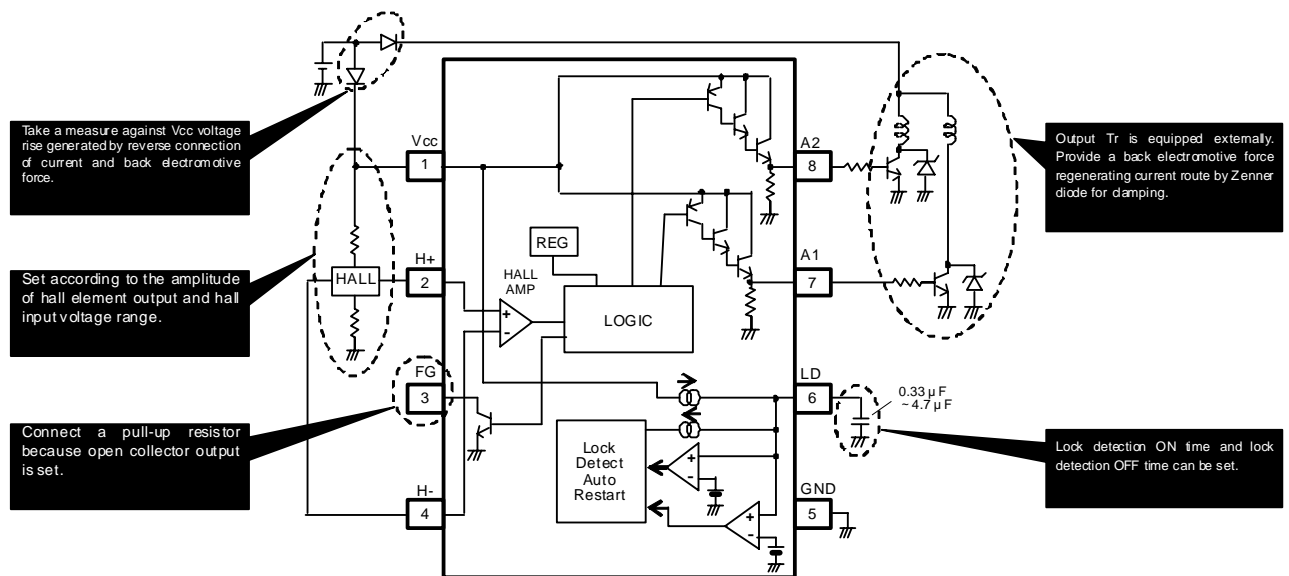


Fig.9 application circuit

Substrate design note

- IC power, motor outputs, and motor ground lines are made as fat as possible.
- IC ground (signal ground) line is common with the application ground except motor ground (i.e. hall ground etc.), and arranged near to (-) land.
- The bypass capacitor and/or Zenner diode are arrangement near to Vcc terminal.
- H+ and H- lines are arranged side by side and made from the hall element to IC as shorter as possible, because it is easy for the noise to influence the hall lines.

Description of operations

1) Lock protection and automatic restart

CR timer system

Charging and discharging time at LD terminal depends on the capacitor equipped externally on LD terminal. Charging and discharging time is determined as follows:

$$\begin{aligned} \text{TON(charging time)} &= \frac{C \times (\text{VLDCL} - \text{VLDCLP})}{\text{ILDC}} \\ \text{TOFF(discharging time)} &= \frac{C \times (\text{VLDCL} - \text{VLDCLP})}{\text{ILDD}} \end{aligned}$$

C : Capacity of capacitor equipped externally on LD terminal
VLDCL : LD terminal clamping voltage
VLDCLP : LD terminal comparator voltage
ILDC : LD terminal charging current
ILDD : LD terminal discharging current

Timing chart of LD terminal is shown in Fig.10.

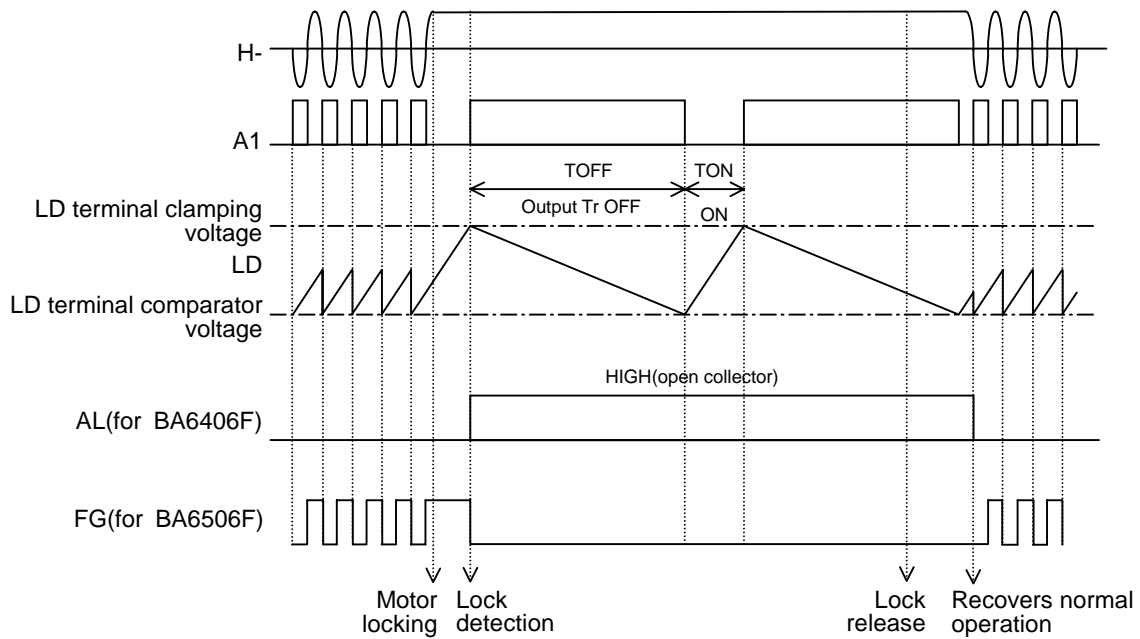


Fig.10 Lock protection (CR timer system) timing chart

Thermal derating curve

Power dissipation (total loss) indicates the power that can be consumed by IC at Ta = 25°C (normal temperature). IC is heated when it consumes power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, etc, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip (maximum junction temperature) and thermal resistance of package (heat dissipation capability). The maximum junction temperature is in general equal to the maximum value in the storage temperature range.

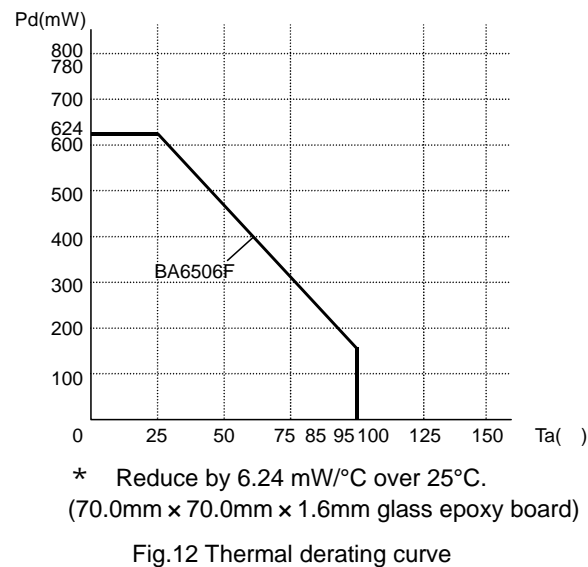
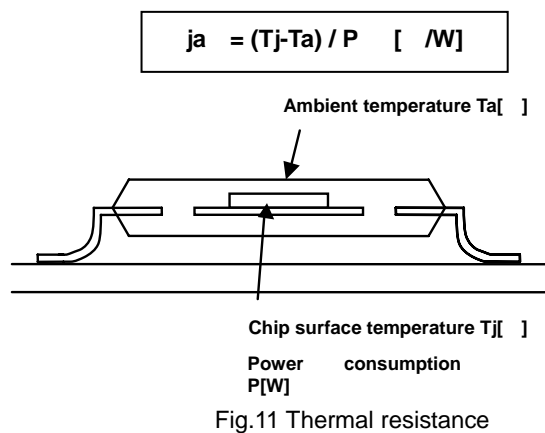
Heat generated by consumed power of IC is radiated from the mold resin or lead frame of package. The parameter which indicates this heat dissipation capability (hardness of heat release) is called heat resistance, represented by the symbol θ_{ja} [$^{\circ}\text{C}/\text{W}$]. The temperature of IC inside the package can be estimated by this heat resistance. Fig.11 shows the model of heat resistance of the package.

Heat resistance θ_{ja} , ambient temperature Ta, junction temperature Tj, and power consumption P can be calculated by the equation below:

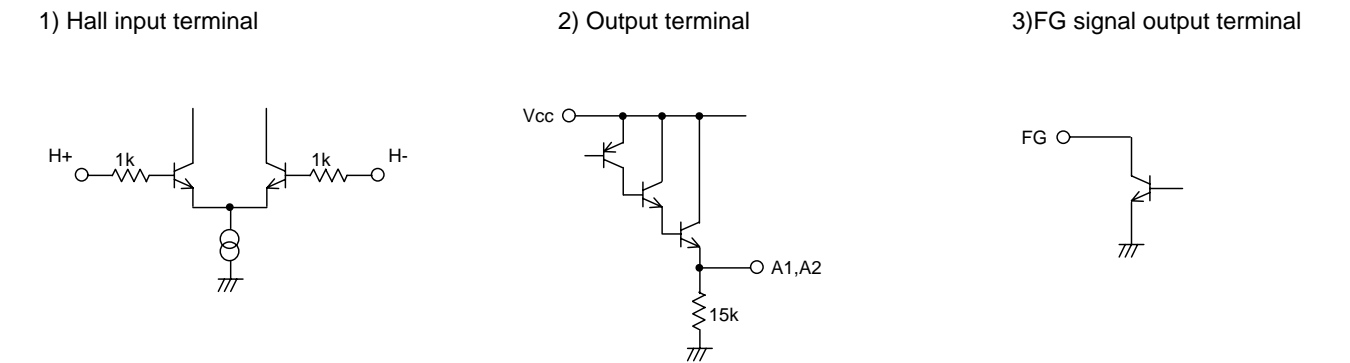
$$\theta_{ja} = (T_j - T_a) / P \quad [\text{ }^{\circ}\text{C} / \text{W}]$$

Thermal derating curve indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance θ_{ja} .

Thermal resistance θ_{ja} depends on chip size, power consumption, package ambient temperature, packaging condition, wind velocity, etc., even when the same package is used. Thermal derating curve indicates a reference value measured at a specified condition. Fig.12 shows a thermal derating curve (Value when mounting FR4 glass epoxy board 70 [mm] x 70 [mm] x 1.6 [mm] (copper foil area below 3 [%]))



Equivalent circuit



Safety measure

1) Reverse connection protection diode

Reverse connection of power results in IC destruction as shown in Fig 13. When reverse connection is possible, reverse connection protection diode must be added between power supply and Vcc.

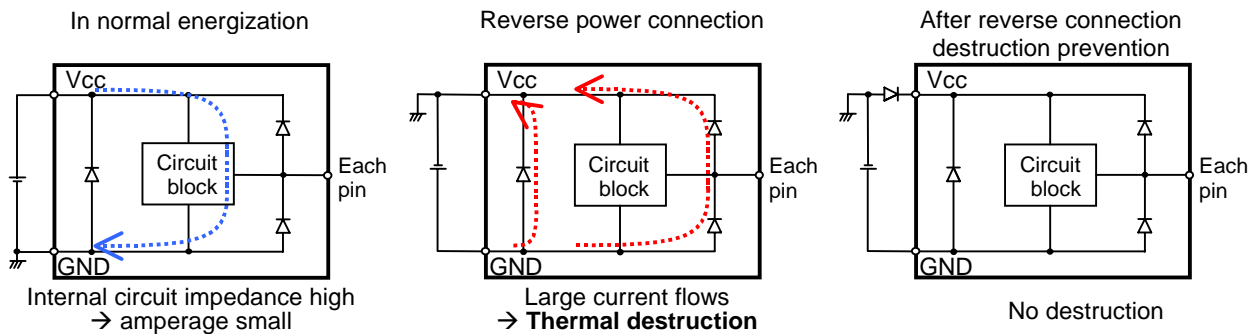


Fig.13 Current flow when power is connected reversely

2) About measures of voltage rise by back electromotive force

The voltage of output terminal rises by back electromotive force. The diode D1 of Fig.14 is necessary to divide a power supply line of motor with small signal line, so that the voltage of the output does not affect a power supply line.

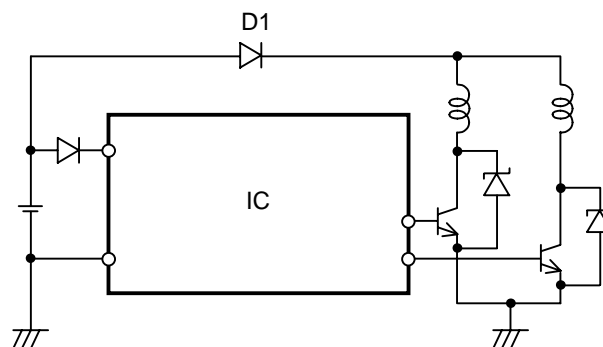


Fig.14 Separation of a power supply line

3) FG output

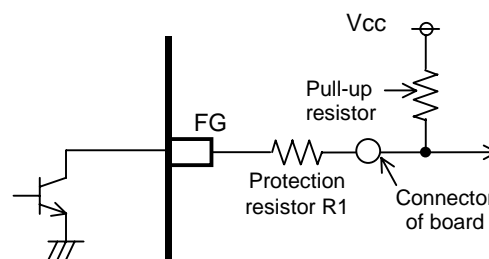


Fig.15 Protection of FG terminal

FG output is an open collector and requires pull-up resistor.

The IC can be protected by adding resistor R1. An excess of absolute maximum rating, when FG output terminal is directly connected to power supply, could damage the IC.

4) Problem of GND line PWM switching

Do not perform PWM switching of GND line because GND terminal potential cannot be kept to a minimum.

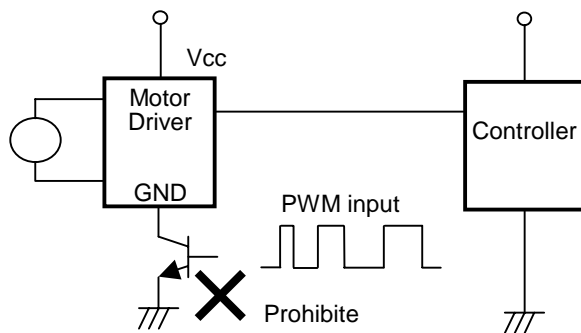


Fig.16 GND Line PWM switching prohibited

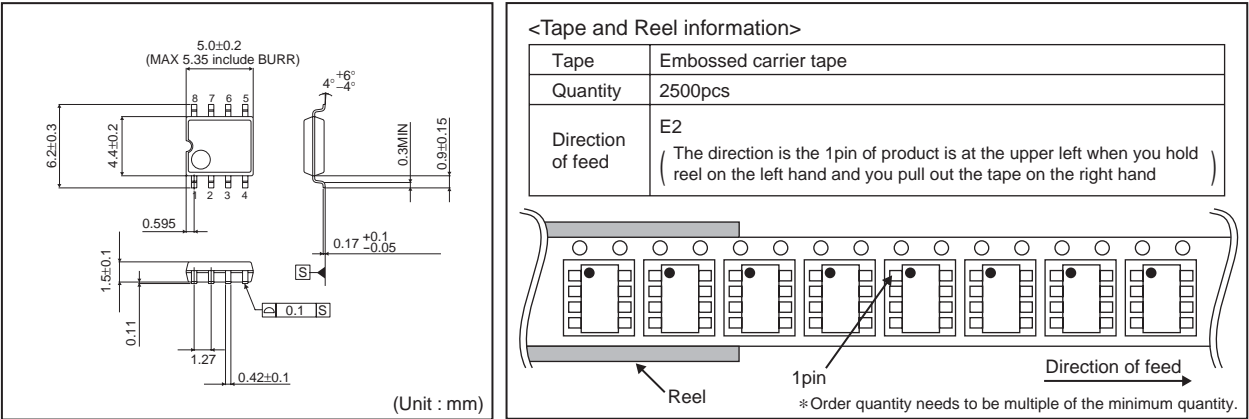
Operational Notes

- 1) Absolute maximum ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.
- 2) Connecting the power supply connector backward
Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added
- 3) Power supply line
Back electromotive force causes regenerated current to power supply line, therefore take a measure such as placing a capacitor between power supply and GND for routing regenerated current. And fully ensure that the capacitor characteristics have no problem before determine a capacitor value. (when applying electrolytic capacitors, capacitance characteristic values are reduced at low temperatures)
- 4) GND potential
The potential of GND pin must be minimum potential in all operating conditions. Also ensure that all terminals except GND terminal do not fall below GND voltage including transient characteristics. However, it is possible that the motor output terminal may deflect below GND because of influence by back electromotive force of motor. Malfunction may possibly occur depending on use condition, environment, and property of individual motor. Please make fully confirmation that no problem is found on operation of IC.
- 5) Thermal design
Use a thermal design that allows for a sufficient margin in light of the power dissipation(Pd) in actual operating conditions
- 6) Inter-pin shorts and mounting errors
Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together
- 7) Actions in strong electromagnetic field
Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction
- 8) ASO
When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO
- 9) Testing on application boards
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC
- 10) GND wiring pattern
When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either
- 11) Capacitor between output and GND
When a large capacitor is connected between output and GND, if Vcc is shorted with 0V or GND for some cause, it is possible that the current charged in the capacitor may flow into the output resulting in destruction. Keep the capacitor between output and GND below 100uF
- 12) IC terminal input
When Vcc voltage is not applied to IC, do not apply voltage to each input terminal. When voltage above Vcc or below GND is applied to the input terminal, parasitic element is actuated due to the structure of IC. Operation of parasitic element causes mutual interference between circuits, resulting in malfunction as well as destruction in the last. Do not use in a manner where parasitic element is actuated

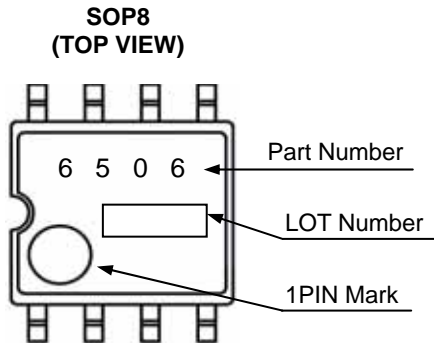
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Physical dimension tape and reel information

SOP8



Marking diagram



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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
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- De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
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