X95840

Quad Digital Controlled Potentiometers (XDCP™) Low Noise/Low Power/I²C Bus/256 Taps

FN8213
Rev 2.00
July 5, 2006

The X95840 integrates four digitally controlled potentiometers (XDCP) on a monolithic CMOS integrated circuit.

The digitally controlled potentiometers are implemented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the I²C bus interface. Each potentiometer has an associated volatile Wiper Register (WR) and a non-volatile Initial Value Register (IVR), that can be directly written to and read by the user. The contents of the WR controls the position of the wiper. At power up the device recalls the contents of the four DCP's IVR to the corresponding WRs.

The DCPs can be used as three-terminal potentiometers or as two-terminal variable resistors in a wide variety of applications including control, parameter adjustments, and signal processing.

Ordering Information

PART NUMBER	PART MARKING	RESISTANCE OPTION	PACKAGE
X95840WV20I-2.7*	X95840WV G	10kΩ	20 Ld TSSOP
X95840WV20IZ-2.7* (Note)	X95840WV Z G	10kΩ	20 Ld TSSOP (Pb-free)
X95840UV20I-2.7*	X95840UV G	50kΩ	20 Ld TSSOP
X95840UV20IZ-2.7* (Note)	X95840UV Z G	50kΩ	20 Ld TSSOP (Pb-free)

*Add "T1" suffix for tape and reel.

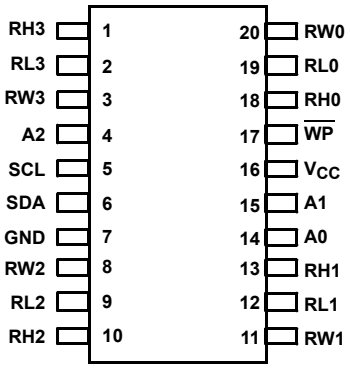
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

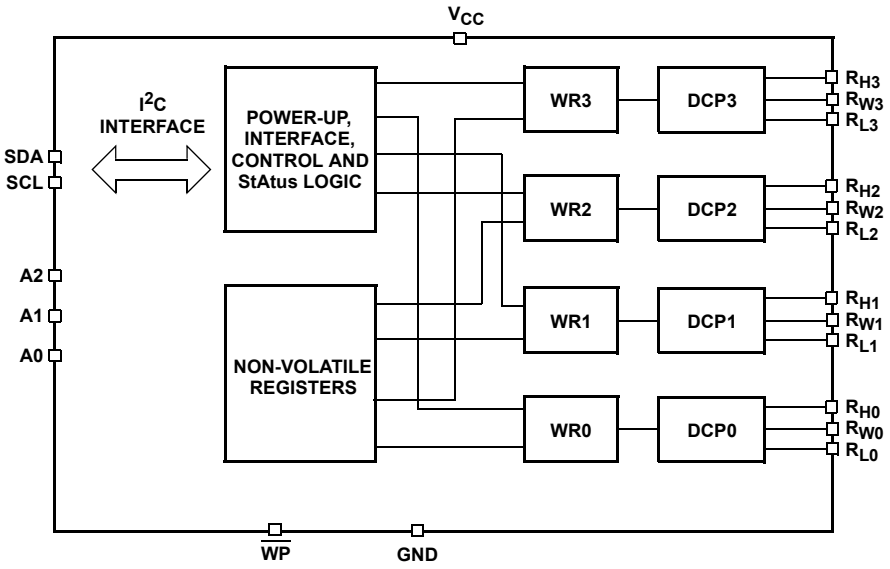
- Four Potentiometers in One Package
- 256 Resistor Taps-0.4% Resolution
- I²C Serial Interface
  - Three address pins, up to eight devices/bus
- Wiper Resistance: 70Ω Typical @ 3.3V
- Non-Volatile Storage of Wiper Position
- Standby Current < 5µA Max
- Power Supply: 2.7V to 5.5V
- 50kΩ, 10kΩ Total Resistance
- High Reliability
  - Endurance: 150,000 data changes per bit per register
  - Register data retention: 50 years @ T ≤ 75°C
- 20 Ld TSSOP
- Pb-Free Plus Anneal Available (RoHS Compliant)

Pinouts

X95840
(20 LD TSSOP)
TOP VIEW



Block Diagram



Pin Descriptions

TSSOP PIN	SYMBOL	DESCRIPTION
1	RH3	“High” terminal of DCP3
2	RL3	“Low” terminal of DCP3
3	RW3	“Wiper” terminal of DCP3
4	A2	Device address for the I^2C interface
5	SCL	I^2C interface clock
6	SDA	Serial data I/O for the I^2C interface
7	GND	Device ground pin
8	RW2	“Wiper” terminal of DCP2
9	RL2	“Low” terminal of DCP2
10	RH2	“High” terminal of DCP2
11	RW1	“Wiper” terminal of DCP1
12	RL1	“Low” terminal of DCP1
13	RH1	“High” terminal of DCP1
14	A0	Device address for the I^2C interface
15	A1	Device address for the I^2C interface
16	V_{CC}	Power supply pin
17	$\overline{WP}$	Hardware write protection pin. Active low. Prevents any “Write” operation of the I^2C interface.
18	RH0	“High” terminal of DCP0
19	RL0	“Low” terminal of DCP0
20	RW0	“Wiper” terminal of DCP0

Absolute Maximum Ratings

Storage Temperature . . . . . -65°C to +150°C
Voltage at any Digital Interface Pin
with Respect to GND . . . . . -0.3V to V_{CC}+0.3
V_{CC} . . . . . -0.3V to +6V
Voltage at any DCP Pin with Respect to GND. . . . . -0.3V to V_{CC}
Lead Temperature (soldering, 10s) . . . . . 300°C
I_W (10s) . . . . . ±6mA

Recommended Operating Conditions

Temperature Range (Industrial) . . . . . -40°C to 85°C
V_{CC} . . . . . 2.7V to 5.5V
Power Rating of Each DCP 5mW
Wiper Current of Each DCP. . . . . ±3.0mA

CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Analog Specifications

Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNIT
R_{TOTAL}	R_H to R_L Resistance	W, U versions respectively		10, 50		kΩ
	R_H to R_L Resistance Tolerance		-20		+20	%
R_W	Wiper Resistance	V_{CC} = 3.3V @ 25°C Wiper current = V_{CC}/R_{TOTAL}		70	200	Ω
$C_H/C_L/C_W$	Potentiometer Capacitance (Note 15)			10/10/25		pF
I_{LkgDCP}	Leakage on DCP Pins (Note 15)	Voltage at pin from GND to V_{CC}		0.1	1	µA
VOLTAGE DIVIDER MODE (0V @ RL_i; V_{CC} @ RH_i; measured at RW_i, unloaded; i = 0, 1, 2, or 3)						
INL (Note 6)	Integral Non-linearity		-1		1	LSB (Note 2)
DNL (Note 5)	Differential Non-linearity	Monotonic over all tap positions	-0.5		0.5	LSB (Note 2)
ZSerror (Note 3)	Zero-scale Error	U option	0	1	7	LSB (Note 2)
		W option	0	0.5	2	
FSerror (Note 4)	Full-scale Error	U option	-7	-1	0	LSB (Note 2)
		W option	-2	-1	0	
V_{MATCH} (Note 7)	DCP to DCP Matching	Any two DCPs at same tap position, same voltage at all RH terminals, and same voltage at all RL terminals	-2		2	LSB (Note 2)
TC_V (Note 8)	Ratiometric Temperature Coefficient	DCP Register set to 80 hex		±4		ppm/°C
RESISTOR MODE (Measurements between RW_i and RL_i with RH_i not connected, or between RW_i and RH_i with RL_i not connected. i = 0, 1, 2 or 3)						
RINL (Note 12)	Integral Non-linearity	DCP register set between 20 hex and FF hex. Monotonic over all tap positions	-1		1	MI (Note 9)
RDNL (Note 11)	Differential Non-linearity		-0.5		0.5	MI (Note 9)
Roffset (Note 10)	Offset	U option	0	1	7	MI (Note 9)
		W option	0	0.5	2	MI (Note 9)
R_{MATCH} (Note 13)	DCP to DCP Matching	Any two DCPs at the same tap position with the same terminal voltages.	-2		2	MI (Note 9)
TC_R (Note 14)	Resistance Temperature Coefficient	DCP register set between 20 hex and FF hex		±45		ppm/°C

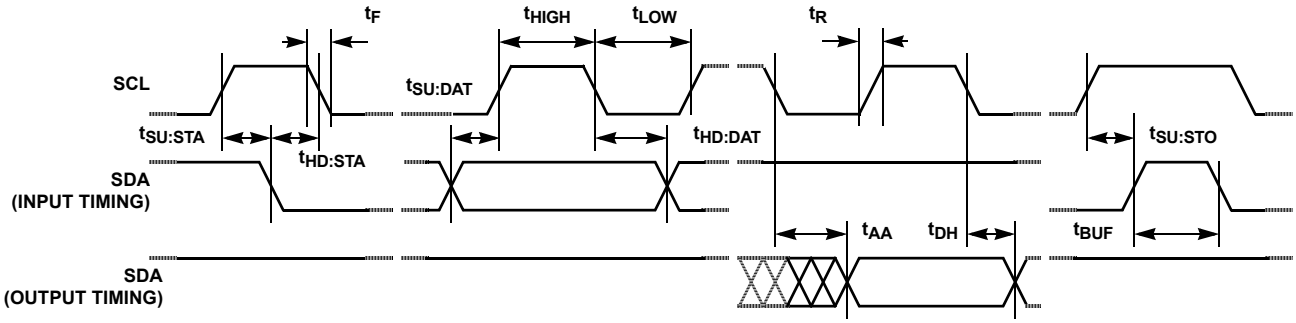
Operating Specifications Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
I_{CC1}	V_{CC} Supply Current (Volatile write/read)	f_{SCL} = 400kHz; SDA = Open; (for I^2C, Active, Read and Volatile Write States only)			1	mA
I_{CC2}	V_{CC} Supply Current (nonvolatile write)	f_{SCL} = 400kHz; SDA = Open; (for I^2C, Active, Nonvolatile Write State only)			3	mA
I_{SB}	V_{CC} Current (standby)	V_{CC} = +5.5V, I^2C Interface in Standby State			5	µA
		V_{CC} = +3.6V, I^2C Interface in Standby State			2	µA
I_{LkgDig}	Leakage Current, at Pins A0, A1, A2, SDA, SCL, and $\overline{WP}$ Pins	Voltage at pin from GND to V_{CC}	-10		10	µA
t_{DCP} (Note 15)	DCP Wiper Response Time	SCL falling edge of last bit of DCP Data Byte to wiper change			1	µs
Vpor	Power-on Recall Voltage	Minimum V_{CC} at which memory recall occurs	1.8		2.6	V
VccRamp	V_{CC} Ramp Rate		0.2			V/ms
t_D (Note 15)	Power-up Delay	V_{CC} above Vpor, to DCP Initial Value Register recall completed, and I^2C Interface in standby state			3	ms
EEPROM SPECS						
	EEPROM Endurance		150,000			Cycles
	EEPROM Retention	Temperature ≤ 75°C	50			Years
SERIAL INTERFACE SPECS						
V_{IL}	$\overline{WP}$, A2, A1, A0, SDA, and SCL Input Buffer LOW Voltage		-0.3		0.3*V_{CC}	V
V_{IH}	$\overline{WP}$, A2, A1, A0, SDA, and SCL Input Buffer HIGH Voltage		0.7*V_{CC}		V_{CC}+0.3	V
Hysteresis (Note 15)	SDA and SCL Input Buffer Hysteresis		0.05* V_{CC}			V
V_{OL} (Note 15)	SDA outPut Buffer LOW Voltage, Sinking 4mA		0		0.4	V
Cpin (Note 15)	$\overline{WP}$, A2, A1, A0, SDA, and SCL Pin Capacitance				10	pF
f_{SCL}	SCL frEquency				400	kHz
t_{IN} (Note 15)	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed.			50	ns
t_{AA} (Note 15)	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{CC}, until SDA exits the 30% to 70% of V_{CC} window.			900	ns
t_{BUF} (Note 15)	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{CC} during the following START condition.	1300			ns
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{CC} crossing.	1300			ns
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{CC} crossing.	600			ns
$t_{SU:STA}$	START Condition Setup Time	SCL rising edge to SDA falling edge. Both crossing 70% of V_{CC}.	600			ns
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{CC} to SCL falling edge crossing 70% of V_{CC}.	600			ns

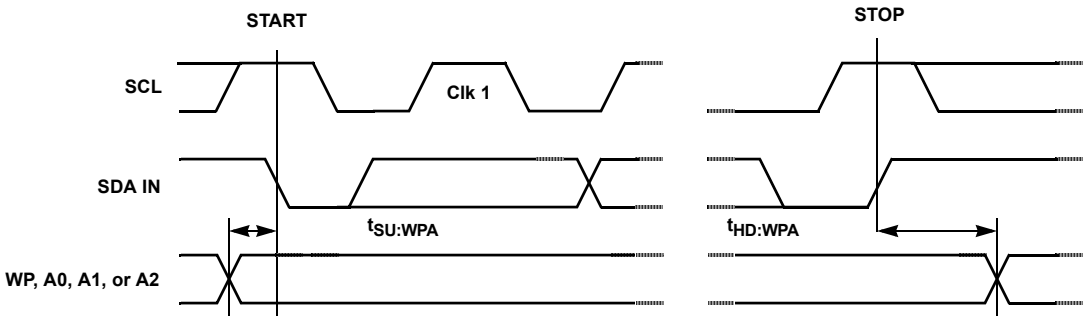
Operating Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
$t_{SU:DAT}$	Input Data Setup Time	From SDA exiting the 30% to 70% of V_{CC} window, to SCL rising edge crossing 30% of V_{CC}	100			ns
$t_{HD:DAT}$	Input Data Hold Time	From SCL rising edge crossing 70% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window.	0			ns
$t_{SU:STO}$	STOP Condition Setup Time	From SCL rising edge crossing 70% of V_{CC}, to SDA rising edge crossing 30% of V_{CC}.	600			ns
$t_{HD:STO}$	STOP Condition Setup Time	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{CC}.	600			ns
t_{DH} (Note 15)	Output Data Hold Time	From SCL falling edge crossing 30% of V_{CC}, until SDA enters the 30% to 70% of V_{CC} window.	0			ns
t_R (Note 15)	SDA and SCL Rise Time	From 30% to 70% of V_{CC}	20 + 0.1 * Cb		250	ns
t_F (Note 15)	SDA and SCL Fall Time	From 70% to 30% of V_{CC}	20 + 0.1 * Cb		250	ns
Cb (Note 15)	Capacitive Loading of SDA or SCL	Total on-chip and off-chip	10		400	pF
Rpu (Note 15)	SDA and SCL Bus Pull-up Resistor Off-chip	Maximum is determined by t_R and t_F. For Cb = 400pF, max is about 2~2.5kΩ. For Cb = 40pF, max is about 15~20kΩ	1			kΩ
t_{WP} (Notes 15, 16)	Non-volatile Write Cycle Time			12	20	ms
$t_{SU:WPA}$	A2, A1, A0, and $\overline{WP}$ Setup Time	Before START condition	600			ns
$t_{HD:WPA}$	A2, A1, A0, and $\overline{WP}$ Hold Time	After STOP condition	600			ns

SDA vs SCL Timing



$\overline{WP}$, A0, A1, and A2 Pin Timing



NOTES:

1. Typical values are for T_A = 25°C and 3.3V supply voltage.
2. LSB: $[V(RW)_{255} - V(RW)_0] / 255$. $V(RW)_{255}$ and $V(RW)_0$ are V(RW) for the DCP register set to FF hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
3. ZS error = $V(RW)_0$ / LSB.
4. FS error = $[V(RW)_{255} - V_{CC}]$ / LSB.
5. DNL = $[V(RW)_i - V(RW)_{i-1}]$ / LSB-1, for i = 1 to 255. i is the DCP register setting.
6. INL = $[V(RW)_i – (i • LSB – V(RW)_0)]$/LSB for i = 1 to 255.
7. V_{MATCH} = $[V(RWx)_i - V(RWy)_i]$ / LSB, for i = 0 to 255, x = 0 to 3 and y = 0 to 3.
8. $TC_V = \frac{Max(V(RW)_i) - Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} \times \frac{10^6}{125°C}$

   for i = 16 to 240 decimal, T = -40°C to 85°C. Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.
9. MI = $|R_{255} - R_0| / 255$. R_{255} and R_0 are the measured resistances for the DCP register set to FF hex and 00 hex respectively.
10. Roffset = R_0 / MI, when measuring between RW and RL.
    Roffset = R_{255} / MI, when measuring between RW and RH.
11. RDNL = $(R_i - R_{i-1})$ / MI, for i = 32 to 255.
12. RINL = $[R_i - (MI • i) - R_0]$ / MI, for i = 32 to 255.
13. R_{MATCH} = $(R_{i,x} - R_{i,y})$ / MI, for i = 0 to 255, x = 0 to 3 and y = 0 to 3.
14. $TC_R = \frac{[Max(Ri) - Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{10^6}{125°C}$

    for i = 32 to 255, T = -40°C to 85°C. Max( ) is the maximum value of the resistance and Min ( ) is the minimum value of the resistance over the temperature range.
15. This parameter is not 100% tested.
16. t_{WC} is the minimum cycle time to be allowed for any non-volatile Write by the user, unless Acknowledge Polling is used. It is the time from a valid STOP condition at the end of a Write sequence of a I^2C serial interface Write operation, to the end of the self-timed internal non-volatile write cycle.

Typical Performance Curves

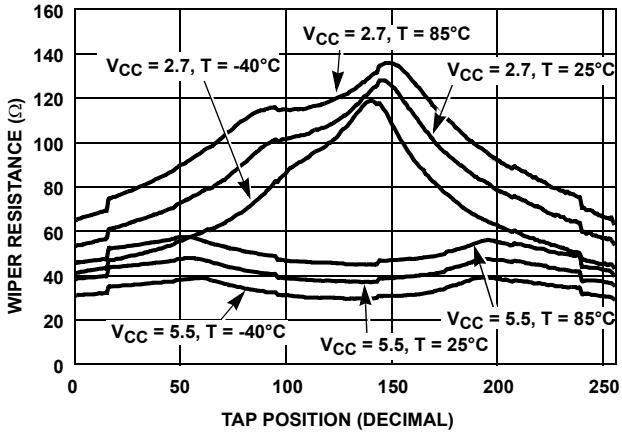


FIGURE 1. WIPER RESISTANCE vs TAP POSITION [I(RW) = V_{CC}/R_{TOTAL}] FOR 50kΩ (U)

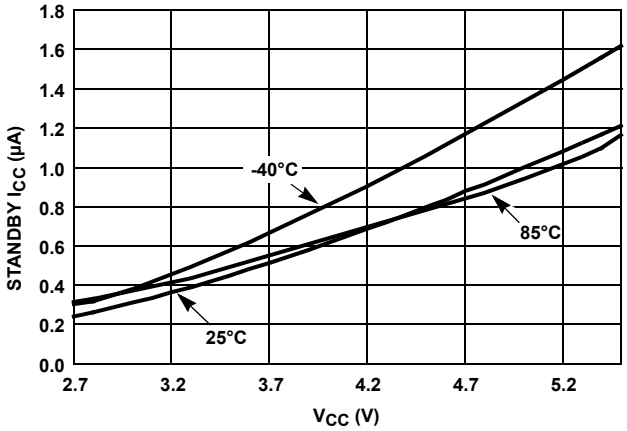


FIGURE 2. STANDBY I_{CC} vs V_{CC}

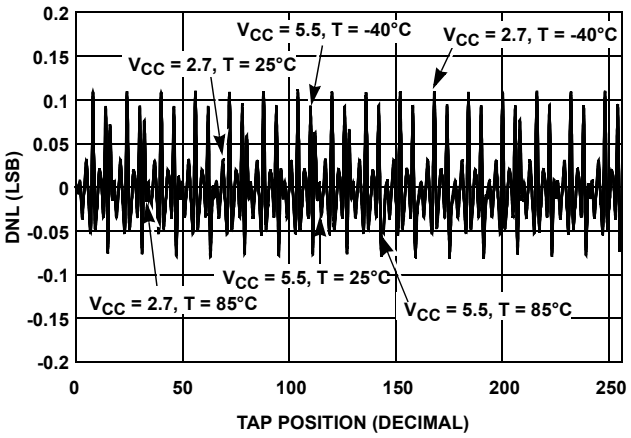


FIGURE 3. DNL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

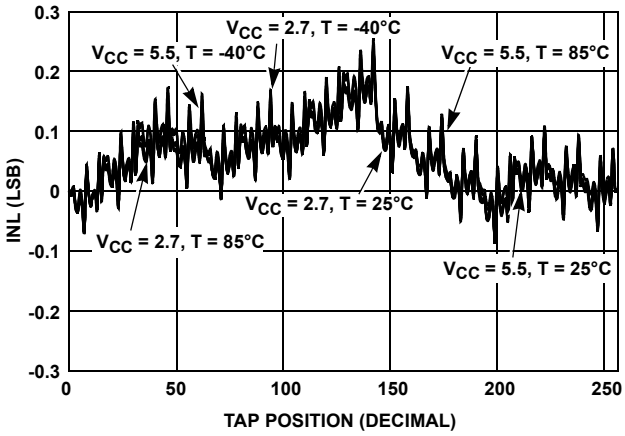


FIGURE 4. INL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

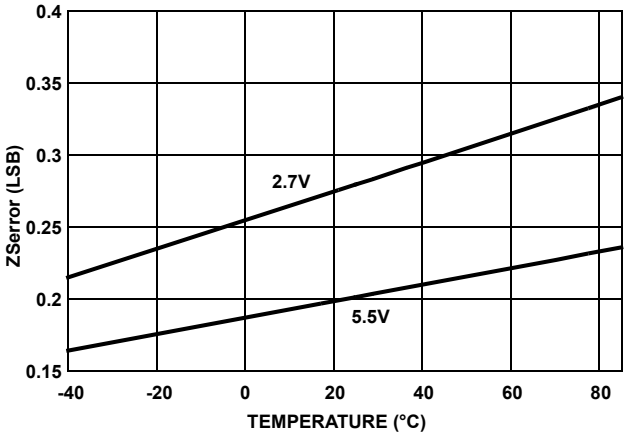


FIGURE 5. ZSerror vs TEMPERATURE

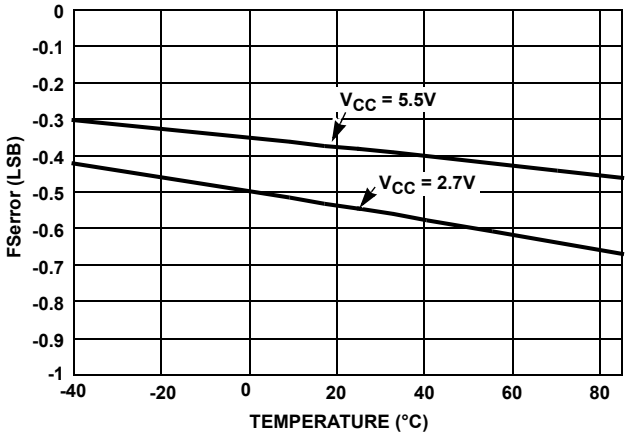


FIGURE 6. FSerror vs TEMPERATURE

Typical Performance Curves (Continued)

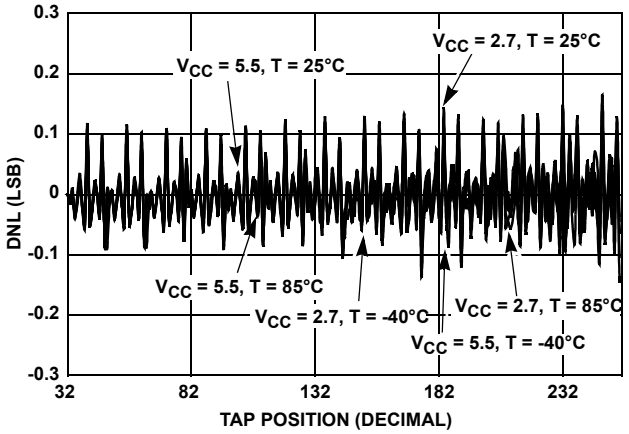


FIGURE 7. DNL vs TAP POSITION IN Rheostat MODE FOR 50kΩ (U)

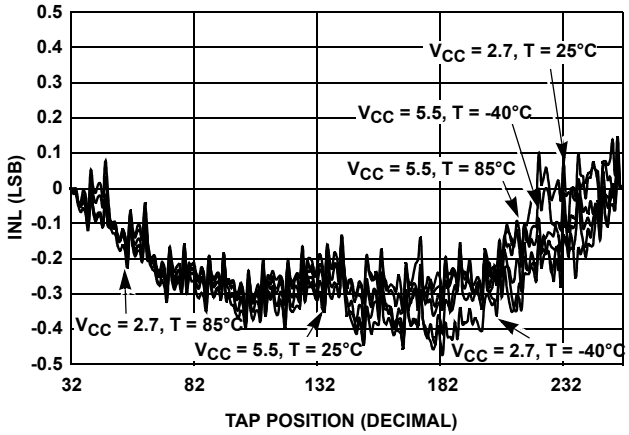


FIGURE 8. INL vs TAP POSITION IN Rheostat MODE FOR 50kΩ (U)

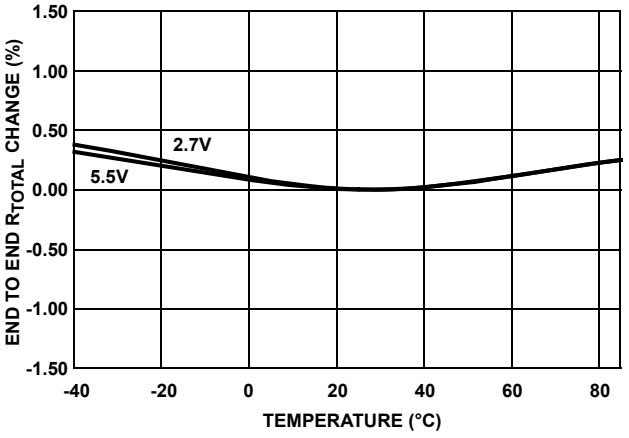


FIGURE 9. END TO END R_{TOTAL} % CHANGE vs TEMPERATURE

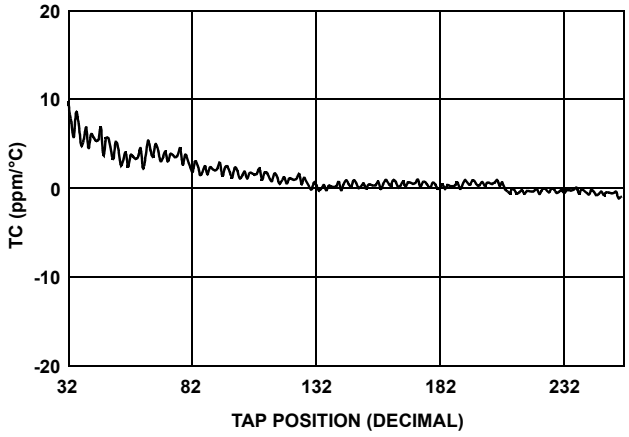


FIGURE 10. TC FOR VOLTAGE DIVIDER MODE IN ppm

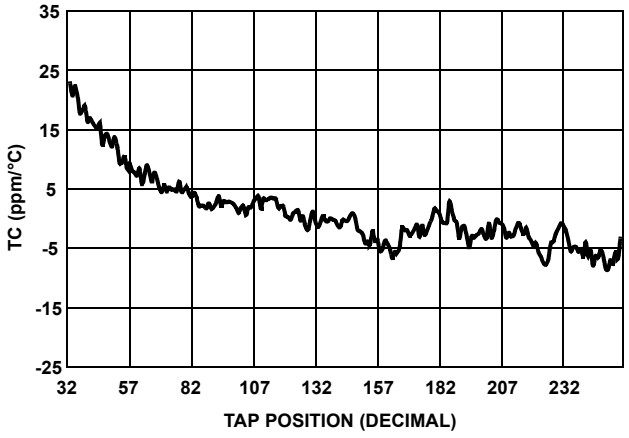


FIGURE 11. TC FOR Rheostat MODE IN ppm

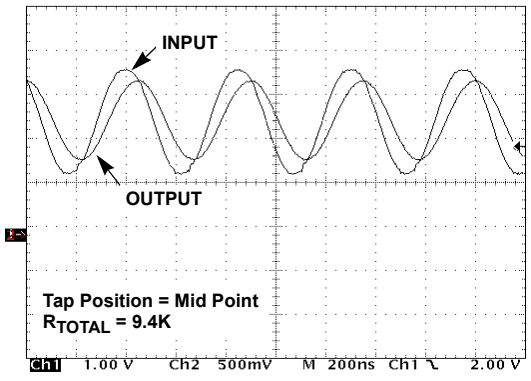


FIGURE 12. FREQUENCY RESPONSE (2.2MHz)

Typical Performance Curves (Continued)

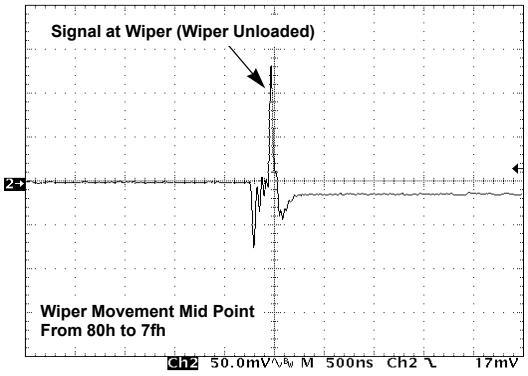


FIGURE 13. MIDSCALE GLITCH, CODE 80h TO 7Fh (WIPER 0)

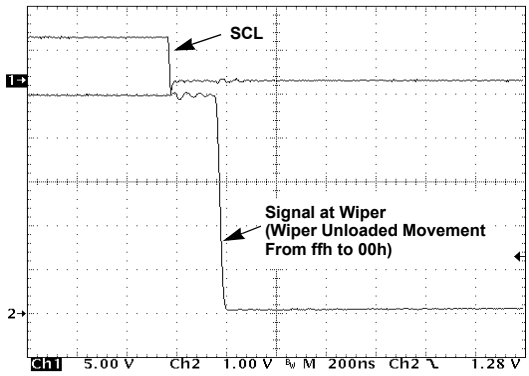


FIGURE 14. LARGE SIGNAL SETTLING TIME

Principles of Operation

The X95840 in as integrated circuit incorporating four DCPs with their associated registers, non-volatile memory, and a I^2C serial interface providing direct communication between a host and the potentiometers and memory.

DCP Description

Each DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer (RH and RL pins). The RW pin of each DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by an 8-bit volatile Wiper Register (WR). Each DCP has its own WR. When the WR of a DCP contains all zeroes (WR<7:0>: 00h), its wiper terminal (RW) is closest to its “Low” terminal (RL). When the WR of a DCP contains all ones (WR<7:0>: FFh), its wiper terminal (RW) is closest to its “High” terminal (RH). As the value of the WR increases from all zeroes (00h) to all ones (255 decimal), the wiper moves monotonically from the position closest to RL to the closest to RH. At the same time, the resistance between RW and RL increases monotonically, while the resistance between RH and RW decreases monotonically.

While the X95840 is being powered up, all four WRs are reset to 80h (128 decimal), which locates RW roughly at the center between RL and RH. Soon after the power supply voltage becomes large enough for reliable non-volatile memory reading, the X95840 reads the value stored on four different non-volatile Initial Value Registers (IVRs) and loads them into their corresponding WRs.

The WRs and IVRs can be read or written directly using the I^2C serial interface as described in the following sections.

Memory Description

The X95840 contains eight non-volatile bytes. they are accessed by I^2C interface operations with Address Bytes 0 through 7 decimal. The first four non-volatile bytes at addresses 0, 1, 2, and 3, contain the initial value loaded at power-up into the volatile Wiper Registers (WRs) of DCP0, DCP1, DCP2, and DCP3 respectively. Bytes at addresses 4, 5, and 6 are available to the user as general purpose registers. The byte at address 7 is reserved; the user should not write to it, and its value should be ignored if read.

The volatile WR, and the non-volatile Initial Value Register (IVR) of a DCP are accessed with the same Address Byte.

A volatile byte at address 8 decimal, controls what byte is read or written when accessing DCP registers: the WR, the IVR, or both.

When the byte at address 8 is all zeroes, which is the default at power up:

- A read operation to addresses 0, 1, 2 or 3 outputs the value of the non-volatile IVRs.
- A write operation to addresses 0, 1, 2, or 3 writes the same value to the WR and IVR of the corresponding DCP.

When the byte at address 8 is 80h (128 decimal):

- A read operation to addresses 0, 1, 2, or 3 outputs the value of the volatile WR.
- A write operation to addresses 0, 1, 2, or 3 only writes to the corresponding volatile WR.

It is not possible to write to an IVR without writing the same value to its corresponding WR.

00h and 80h are the only values that should be written to address 8. All other values are reserved and must not be written to address 8.

To access the general purpose bytes at addresses 4, 5, or 6, the value at address 8 must be all zeros.

The X95840 is pre-programed with 80h in the four IVRs.

TABLE 1. MEMORY MAP

ADDRESS	NON-VOLATILE	VOLATILE
8	—	Access Control
7	Reserved	
6 5 4	General Purpose	Not Available
3 2 1 0	IVR3 IVR2 IVR1 IVR0	WR3 WR2 WR1 WR0

WR: Wiper Register, IVR: Initial value Register.

I²C Serial Interface

The X95840 supports a bidirectional I²C bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the X95840 operates as a slave device in all applications.

All communication over the I²C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (See Figure 15). On power up of the X95840 the SDA pin is in the input mode.

All I²C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The X95840 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (See Figure 15). A START condition is ignored during the power up sequence and during internal non-volatile write cycles.

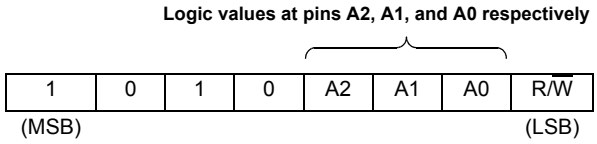
All I²C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (See Figure 15). A STOP condition at the end of a read operation, or at the end of a write operation to volatile bytes only places the device in its standby mode. A STOP condition during a write operation to a non-volatile byte, initiates an internal non-volatile write cycle. The device enters its standby state when the internal non-volatile write cycle is completed.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (See Figure 16).

The X95840 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The X95840 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation

A valid Identification Byte contains 1010 as the four MSBs, and the following three bits matching the logic values present at pins A2, A1, and A0. The LSB in the Read/$\overline{\text{Write}}$ bit. Its value is “1” for a Read operation, and “0” for a Write operation. See Table 2.

TABLE 2. IDENTIFICATION BYTE FORMAT



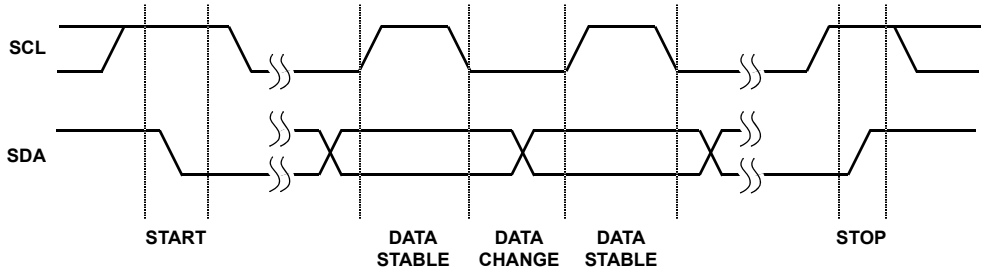


FIGURE 15. VALID DATA CHANGES, START, AND STOP CONDITIONS

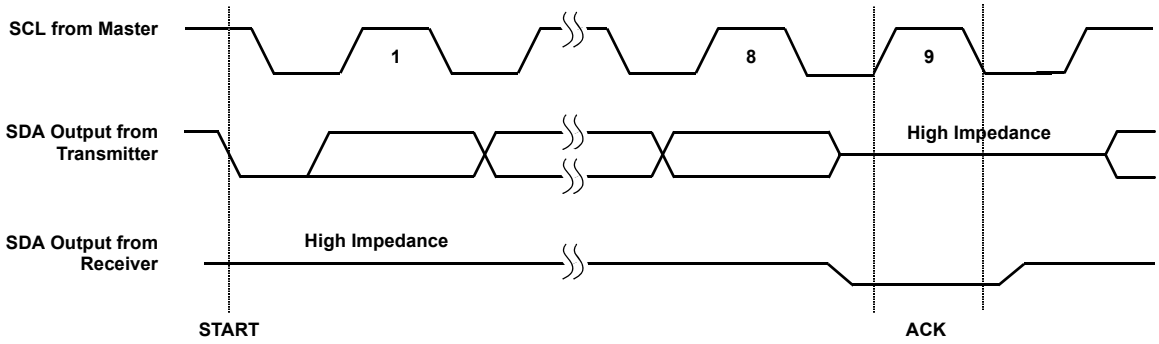


FIGURE 16. ACKNOWLEDGE RESPONSE FROM RECEIVER

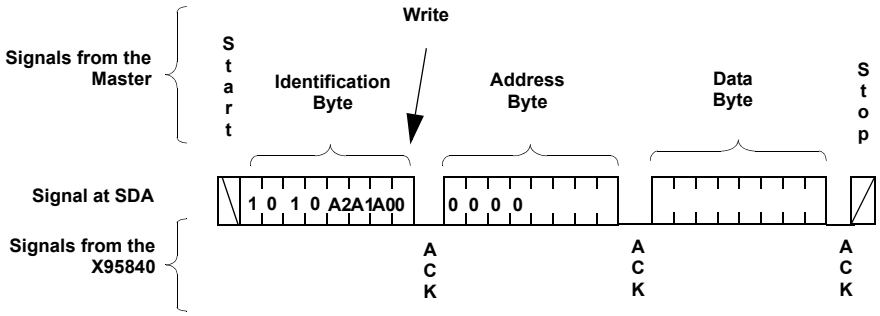


FIGURE 17. BYTE WRITE SEQUENCE

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the X95840 responds with an ACK. At this time, if the Data Byte is to be written only to volatile registers, then the device enters its standby state. If the Data Byte is to be written also to non-volatile memory, the X95840 begins its internal write cycle to non-volatile memory. During the internal non-volatile write cycle, the device ignores transitions at the SDA and SCL pins, and the SDA output is at a high impedance state. When the internal non-volatile write cycle is completed, the X95840 enters its standby state (See Figure 17).

The byte at address 00001000 bin (8 decimal) determines if the Data Byte is to be written to volatile and/or non-volatile memory. See “Memory Description” on page 9.

Data Protection

The $\overline{WP}$ pin has to be at logic HIGH to perform any Write operation to the device. When the $\overline{WP}$ is active (LOW) the device ignores Data Bytes of a Write Operation, does not respond to the Data Bytes with an ACK, and instead, goes to its standby state waiting for a new START condition.

A STOP condition also acts as a protection of non-volatile memory. A valid Identification Byte, Address Byte, and total number of SCL pulses act as a protection of both volatile and non-volatile registers. During a Write sequence, the Data Byte is loaded into an internal shift register as it is received. If the Address Byte is 0, 1, 2, 3, or 8 decimal, the Data Byte is transferred to the appropriate Wiper Register (WR) or to the Access Control Register, at the falling edge of the SCL pulse that loads the last bit (LSB) of the Data Byte. If the Address Byte is between 0 and 6 (inclusive), and the Access Control Register is all zeros (default), then the STOP condition initiates the internal write cycle to non-volatile memory.

Read Operation

A Read operation consist of a three byte instruction followed by one or more Data Bytes (See Figure 18). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the X95840 responds with an ACK. Then the X95840 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eight bit of each byte. The master terminates the read operation (issuing a STOP condition) following the last bit of the last Data Byte (See Figure 18).

The Data Bytes are from the memory location indicated by an internal pointer. This pointer initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location 08h (8 decimal) the pointer “rolls over” to 00h, and the device continues to output data for each ACK received.

The byte at address 00001000 bin (8 decimal) determines if the Data Bytes being read are from volatile or non-volatile memory. See “Memory Description” on page 9.

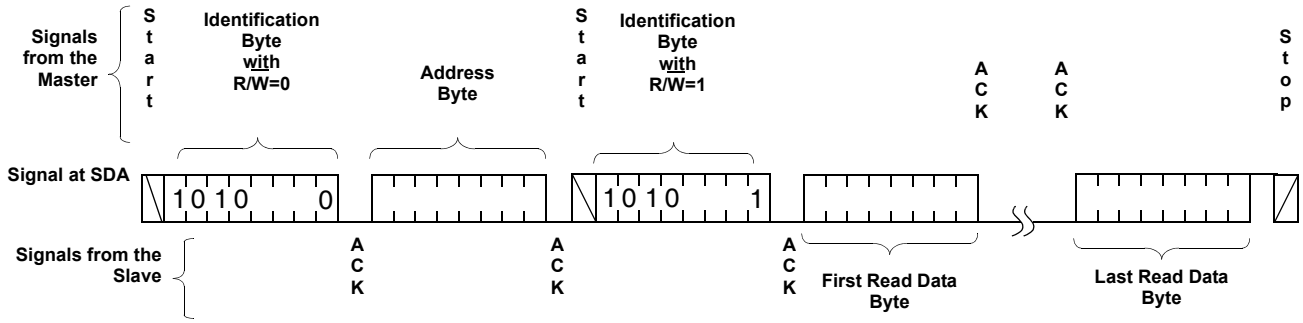
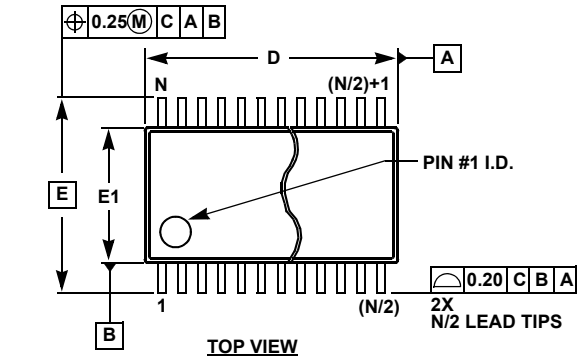
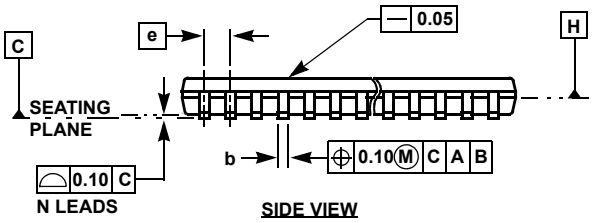
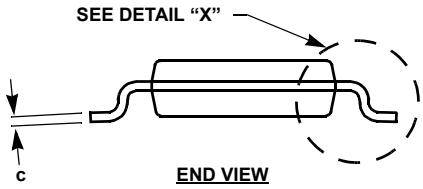


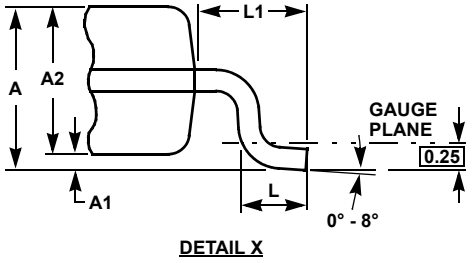
FIGURE 18. READ SEQUENCE

Thin Shrink Small Outline Package Family (TSSOP)









MDP0044

THIN SHRINK SMALL OUTLINE PACKAGE FAMILY

SYMBOL	14 LD	16 LD	20 LD	24 LD	28 LD	TOLERANCE
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.10	0.10	0.10	0.10	0.10	±0.05
A2	0.90	0.90	0.90	0.90	0.90	±0.05
b	0.25	0.25	0.25	0.25	0.25	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	5.00	6.50	7.80	9.70	±0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
e	0.65	0.65	0.65	0.65	0.65	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference

Rev. E 12/02

NOTES:

1. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions “D” and “E1” are measured at dAtum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

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