



# FAST CMOS 16-BIT LATCHED TRANSCEIVER

**IDT74FCT162543AT/CT**

## FEATURES:

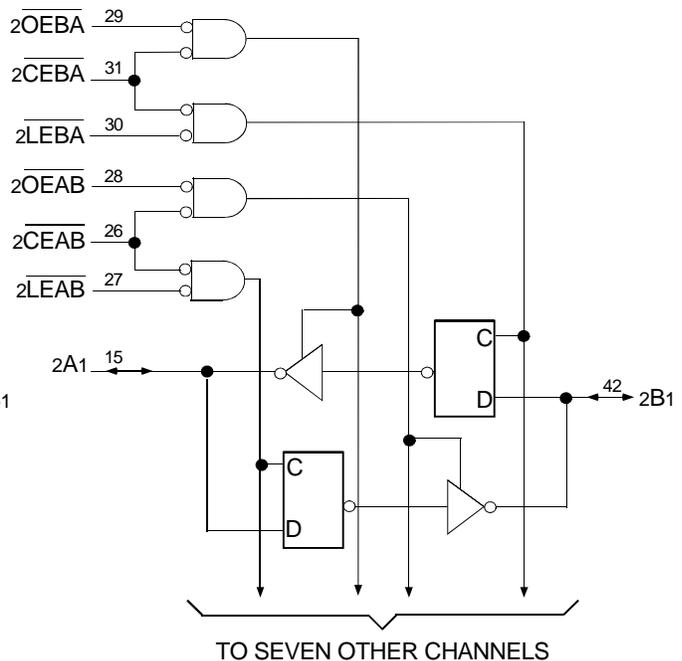
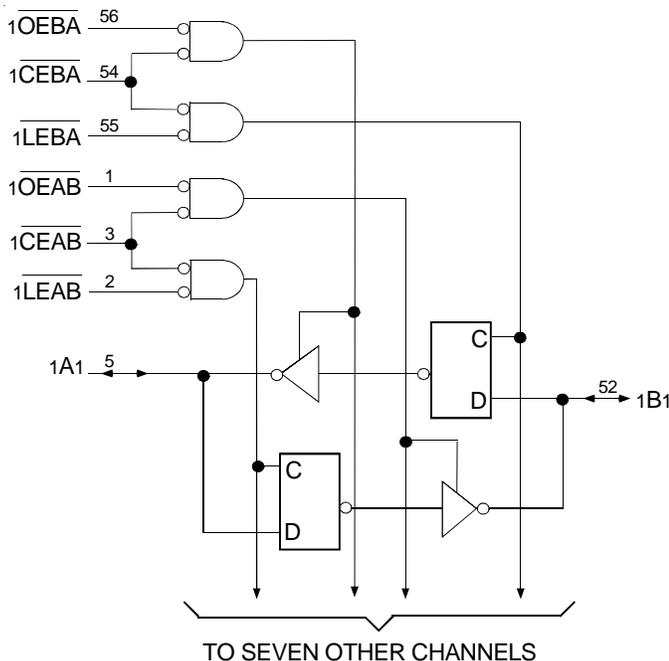
- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical  $t_{sk(o)}$  (Output Skew) < 250ps
- Low input and output leakage  $\leq 1\mu A$  (max.)
- $V_{CC} = 5V \pm 10\%$
- Balanced Output Drivers:  $\pm 24mA$
- Reduced system switching noise
- Typical VOLP (Output Ground Bounce) < 0.6V at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$
- Available in SSOP and TSSOP packages

## DESCRIPTION:

The FCT162543T 16-bit latched transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit D-type latched transceivers with separate input and output control to permit independent control of data flow in either direction. For example, the A-to-B Enable ( $\overline{xCEAB}$ ) must be low in order to enter data from the A port or to output data from the B port.  $\overline{xLEAB}$  controls the latch function. When  $\overline{xLEAB}$  is low, the latches are transparent. A subsequent low-to-high transition of  $\overline{xLEAB}$  signal puts the A latches in the storage mode.  $\overline{xOEAB}$  performs output enable function on the B port. Data flow from the B port to the A port is similar but requires using  $\overline{xCEBA}$ ,  $\overline{xLEBA}$ , and  $\overline{xOEBA}$  inputs. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT162543T has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors. The FCT162543T is a plug-in replacement for the FCT16543T and 54/74ABT16543 for on-board bus interface applications.

## FUNCTIONAL BLOCK DIAGRAM



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INDUSTRIAL TEMPERATURE RANGE

JUNE 2002



## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$I_{IH}$	Input HIGH Current (Input pins) <sup>(5)</sup>	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	$\pm 1$	$\mu\text{A}$
	Input HIGH Current (I/O pins) <sup>(5)</sup>			—	—	$\pm 1$	
$I_{IL}$	Input LOW Current (Input pins) <sup>(5)</sup>		$V_I = \text{GND}$	—	—	$\pm 1$	
	Input LOW Current (I/O pins) <sup>(5)</sup>			—	—	$\pm 1$	
$I_{OZH}$	High Impedance Output Current (3-State Output pins) <sup>(5)</sup>	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZL}$			$V_O = 0.5\text{V}$	—	—	$\pm 1$	
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-80	-140	-250	mA
$V_H$	Input Hysteresis	—		—	100	—	mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND}$ or $V_{CC}$		—	5	500	$\mu\text{A}$

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$I_{ODL}$	Output LOW Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}^{(3)}$		60	115	200	mA
$I_{ODH}$	Output HIGH Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}^{(3)}$		-60	-115	-200	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -24\text{mA}$	2.4	3.3	—	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = 24\text{mA}$	—	0.3	0.55	V

### NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- The test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^{\circ}\text{C}$ .

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ Outputs Open $\overline{xCEAB}$ and $\overline{xOEAB} = \text{GND}$ $\overline{xCEBA} = V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	60	100	$\mu\text{A}/\text{MHz}$
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{xLEAB}$ , $\overline{xCEAB}$ and $\overline{xOEAB} = \text{GND}$ $\overline{xCEBA} = V_{CC}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.6	1.5	mA
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{xLEAB}$ , $\overline{xCEBA}$ and $\overline{xOEAB} = \text{GND}$ $\overline{xCEBA} = V_{CC}$ Sixteen Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	2.4	4.5 <sup>(5)</sup>	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{xLEAB}$ , $\overline{xCEAB}$ and $\overline{xOEAB} = \text{GND}$ $\overline{xCEBA} = V_{CC}$ One Bit Toggling	$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	0.9	2.3	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{xLEAB}$ , $\overline{xCEBA}$ and $\overline{xOEAB} = \text{GND}$ $\overline{xCEBA} = V_{CC}$ Sixteen Bit Toggling	$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	6.4	16.5 <sup>(5)</sup>	

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient.

3. Per TTL driven input ( $V_{IN} = 3.4V$ ). All other inputs at  $V_{CC}$  or  $\text{GND}$ .

4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

5. Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.

6.  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$

$I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$

$\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V \text{)}$

$D_H = \text{Duty Cycle for TTL Inputs High}$

$N_T = \text{Number of TTL Inputs at } D_H$

$I_{CCD} = \text{Dynamic Current caused by an Input Transition Pair (HLH or LHL)}$

$f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$

$N_{CP} = \text{Number of Clock Inputs at } f_{CP}$

$f_i = \text{Input Frequency}$

$N_i = \text{Number of Inputs at } f_i$

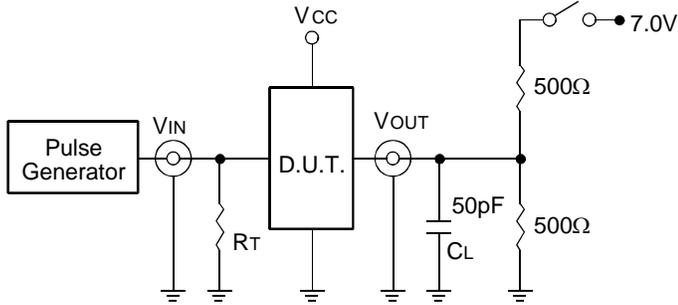
## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition <sup>(1)</sup>	74FCT162543AT		74FCT162543CT		Unit
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Transparent Mode xAx to xBx or xBx to xAx	CL = 50pF RL = 500Ω	1.5	6.5	1.5	3.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay xLEB $\bar{A}$ to xAx, xLEAB to xBx		1.5	8	1.5	4.1	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time xOEBA or xOEAB to xAx or xBx xCEBA or xCEAB to xAx or xBx		1.5	9	1.5	4.8	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time xOEBA or xOEAB to xAx or xBx xCEBA or xCEAB to xAx or xBx		1.5	7.5	1.5	4	ns
t <sub>SU</sub>	Set-up Time HIGH or LOW xAx or xBx to xLEAB or xLEBA		2	—	1	—	ns
t <sub>H</sub>	Hold Time HIGH or LOW xAx or xBx to xLEAB or xLEBA		2	—	1	—	ns
t <sub>w</sub>	xLEB $\bar{A}$ or xLEAB Pulse Width LOW		4	—	3 <sup>(4)</sup>	—	ns
t <sub>SK(o)</sub>	Output Skew <sup>(3)</sup>		—	0.5	—	0.5	ns

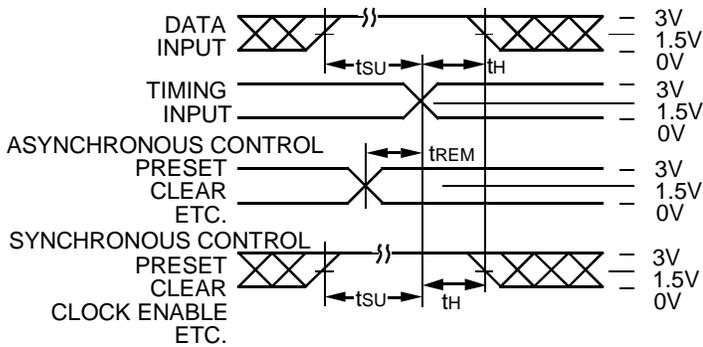
NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.

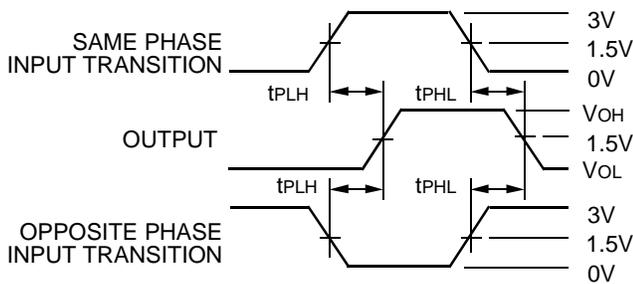
## TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-up, Hold, and Release Times



Propagation Delay

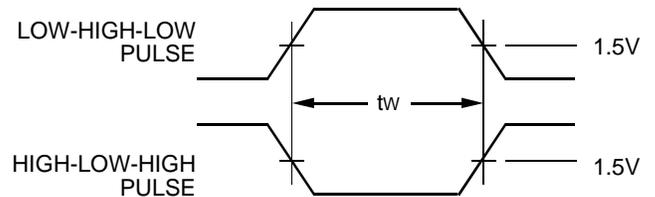
## SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

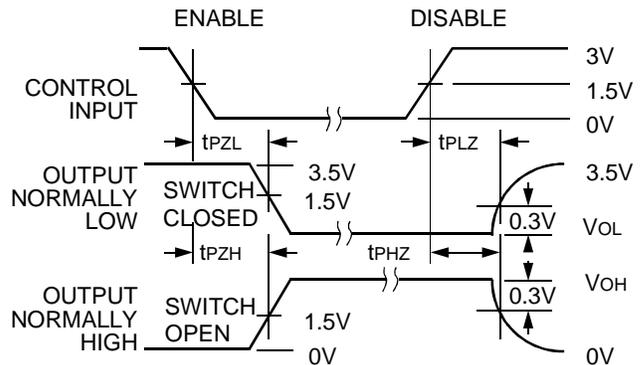
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

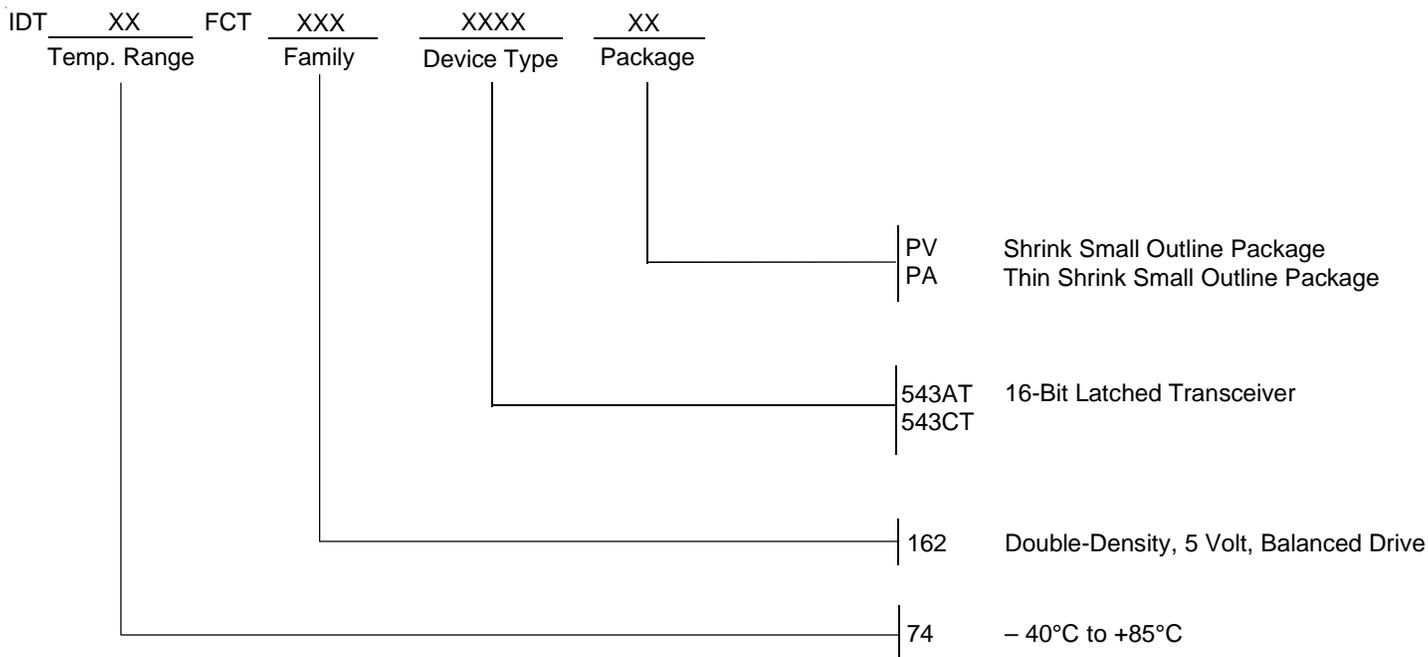


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate  $\leq$  1.0MHz;  $t_f \leq$  2.5ns;  $t_r \leq$  2.5ns.

## ORDERING INFORMATION



## DATA SHEET DOCUMENT HISTORY

- 3/28/2002    Removed standard speed grade
- 5/21/2002    Removed TVSOP package
- 6/20/2002    Updated as per PDNs Logic-00-07 and Logic-01-04



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