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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

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SEMICONDUCTOR®

74LCX38
Low Voltage Quad 2-Input NAND Gate (Open Drain) with 5V Tolerant Inputs

General Description

The LCX38 contains four 2-input open drain NAND gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

The 74LCX38 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

■ 5V tolerant inputs

■ 2.3V to 3.6V V_{CC} specifications provided

■ 5.0 ns t_{PD} max (V_{CC} = 3.3V), 10 μA I_{CC} max

■ Power down high impedance inputs and outputs

■ 24 mA output drive (V_{CC} = 3.0V)

■ Implements proprietary noise/EMI reduction circuitry

■ Latch-up performance exceeds 500 mA

■ ESD performance:
   Human body model > 2000V
   Machine model > 150V

Ordering Code:

Order Number	Package Number	Package Description
74LCX38M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LCX38MX_NL (Note 1)	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LCX38SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX38MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74LCX38MTCX_NL (Note 1)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

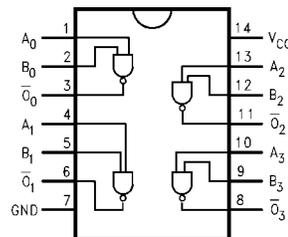Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Note 1: "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

Logic Symbol
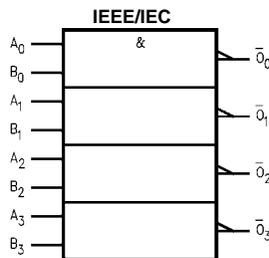
Connection Diagram

Pin Descriptions

Pin Names	Description
A_n, B_n	Inputs
$\overline{O}_n$	Outputs

Absolute Maximum Ratings(Note 2)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in HIGH or LOW State (Note 3)	V
I_{IK}	DC Input Diode Current	−50	$V_I <$ GND	mA
I_{OK}	DC Output Diode Current	−50	$V_O <$ GND	mA
I_O	DC Output Sink Current (I_{OL})	+50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions (Note 4)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage		0	5.5	V
I_{OL}	Output Current	$V_{CC} = 3.0V – 3.6V$		24	mA
		$V_{CC} = 2.7V – 3.0V$		12	
		$V_{CC} = 2.3V – 2.7V$		8	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V–2.0V$, $V_{CC} = 3.0V$		0	10	ns/V

Note 2: The Absolute Maximum Ratings are those beyond which the safety of the device cannot be guaranteed. The device should not be operating at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I_O Absolute Maximum Rating must be observed.

Note 4: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$ Min	$T_A = -40°C$ to $+85°C$ Max	Units
V_{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		
V_{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.3 – 3.6		0.8	
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100\mu A$	2.3 – 3.6		0.2	V
		$I_{OL} = 8mA$	2.3		0.6	
		$I_{OL} = 12$ mA	2.7		0.4	
		$I_{OL} = 16$ mA	3.0		0.4	
		$I_{OL} = 24$ mA	3.0		0.55	
I_I	Input Leakage Current	$0 \le V_I \le 5.5V$	2.3 – 3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or $V_O = 5.5V$	0		10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 – 3.6		10	μA
		$3.6V \le V_I \le 5.5V$	2.3 – 3.6		±10	
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} -0.6V$	2.3 – 3.6		500	μA
I_{OHZ}	Off State Current	$V_O = 5.5$	2 - 3.6		10	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $R_L = 500 \Omega$						Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5V \pm 0.2V$		
		$C_L = 50$ pF		$C_L = 50$ pF		$C_L = 30$ pF		
		Min	Max	Min	Max	Min	Max	
t_{PZL}	Propagation Delay Time	1.5	5.0	1.5	5.5	1.5	6.5	ns
t_{PLZ}		1.5	5.0	1.5	5.5	1.5	6.0	
t_{OSHL}	Output to Output Skew		1.0					ns
t_{OSLH}	(Note 5)		1.0					

Note 5: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	−0.8	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	−0.6	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, f = 10 MHz	25	pF

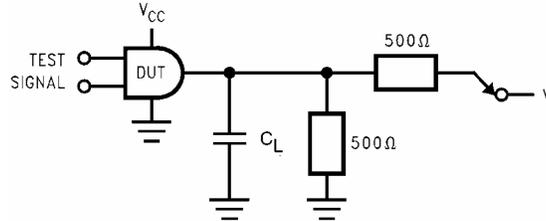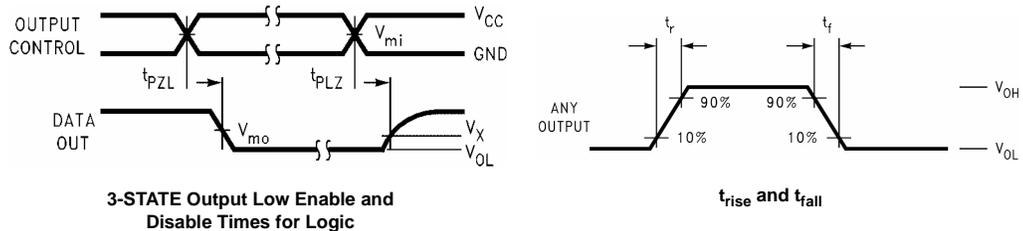# AC Loading and Waveforms Generic for LCX Family

FIGURE 1. AC Test Circuit
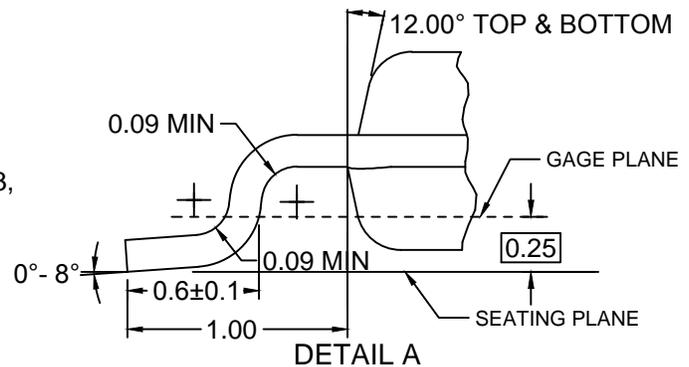**(C$_L$ includes probe and jig capacitance)**
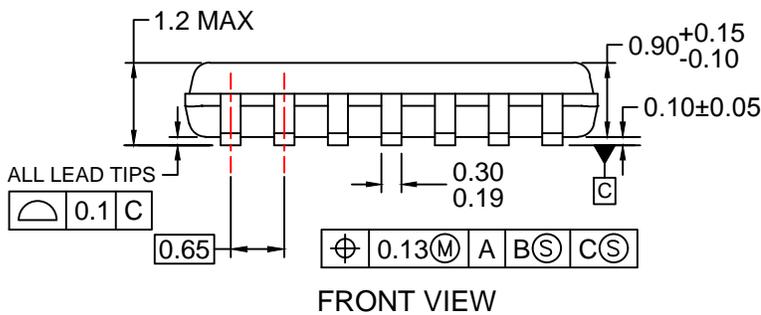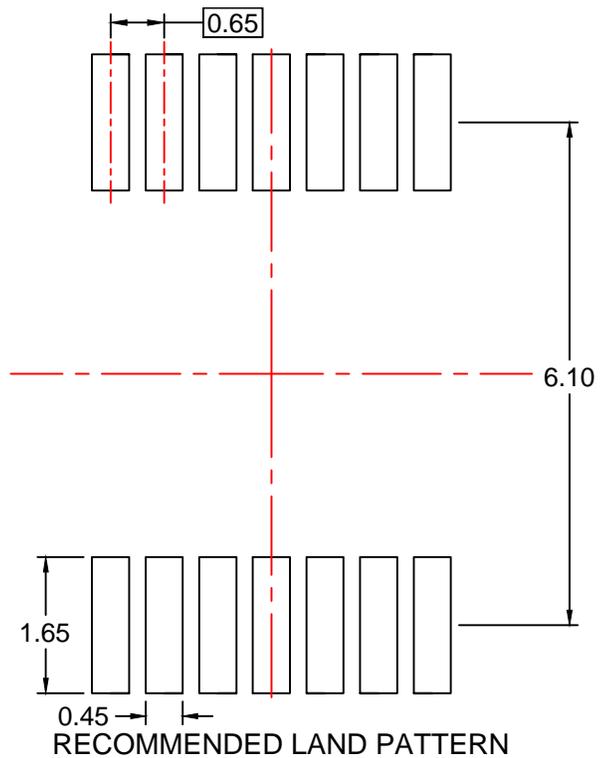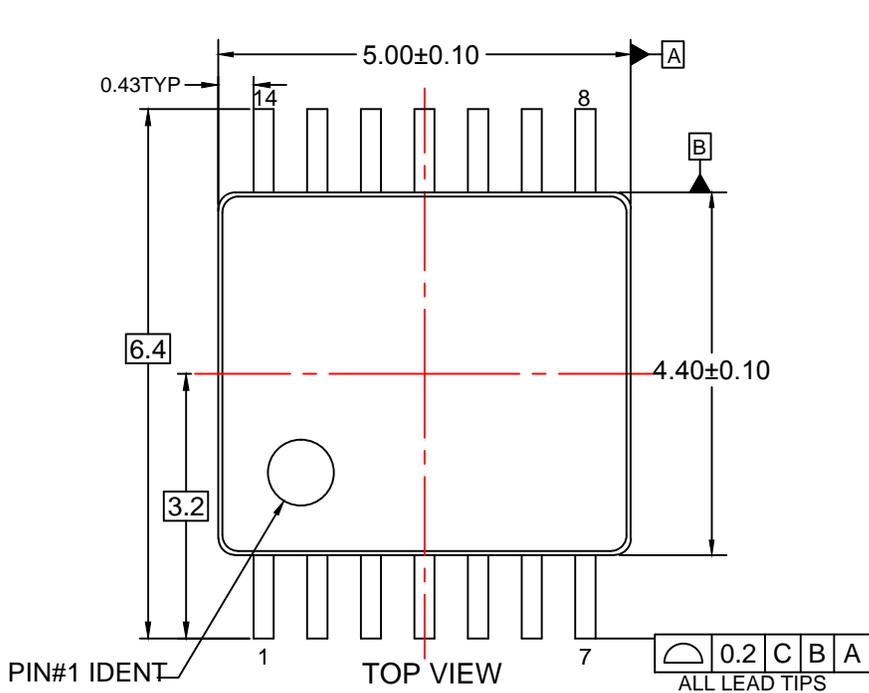
Test	Switch
t$_{PZL}$, t$_{PLZ}$	6V at V$_{CC}$ = 3.3 ± 0.3V V$_{CC}$ x 2 at V$_{CC}$ = 2.5 ± 0.2V

3-STATE Output Low Enable and
Disable Times for Logic

t$_{rise}$ and t$_{fall}$

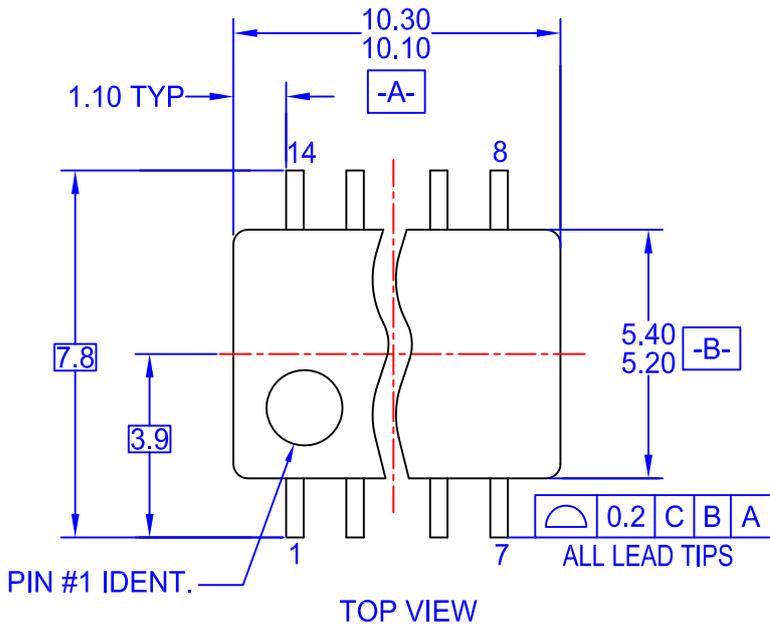**FIGURE 2. Waveforms**
(Input Pulse Characteristics; f = 1MHz, t$_r$ = t$_f$ = 3ns)

Symbol	V$_{CC}$		
	3.3V ± 0.3V	2.7V	2.5V ± 0.2V
V$_{mi}$	1.5V	1.5V	V$_{CC}$/2
V$_{mo}$	1.5V	1.5V	V$_{CC}$/2
V$_x$	V$_{OL}$ + 0.3V	V$_{OL}$ + 0.3V	V$_{OL}$ + 0.15V
V$_y$	V$_{OH}$ − 0.3V	V$_{OH}$ − 0.3V	V$_{OH}$ − 0.15V

5.00±0.10

A

0.43TYP

14

8

B

6.4

4.40±0.10

3.2

PIN#1 IDENT

1

TOP VIEW

7

⌒ 0.2 C B A
ALL LEAD TIPS

0.65

6.10

1.65

0.45

RECOMMENDED LAND PATTERN

1.2 MAX

0.90 +0.15 -0.10

0.10±0.05

ALL LEAD TIPS

⌒ 0.1 C

0.30
0.19

C

0.65

⊕ 0.13 Ⓜ A BⓈ CⓈ

FRONT VIEW

SEE DETAIL A

0.20
0.09

12.00° TOP & BOTTOM

0.09 MIN

GAGE PLANE

0° - 8°

0.09 MIN

0.25

0.6±0.1

1.00

SEATING PLANE

DETAIL A
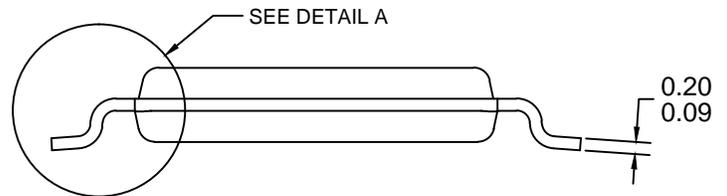
NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-153,
   VARIATION AB, REF NOTE 6
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS,
   MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONING AND TOLERANCES PER ANSI
   Y14.5M, 2009.
E. LANDPATTERN STANDARD: SOP65P640X110-14M.
F. DRAWING FILE NAME: MKT-MTC14rev7.

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TOP VIEW

10.30
10.10
-A-

1.10 TYP

14   8

7.8

3.9

5.40
5.20 -B-

PIN #1 IDENT.

1   7

⌒ 0.2 C B A
ALL LEAD TIPS

FRONT VIEW

ALL LEAD TIPS

⌒ 0.1 C

2.1 MAX

-C-

1.90
1.70

0.16
0.14

1.27 TYP

0.51
0.35

⊕ 0.12 Ⓜ C A

DETAIL A

7° TYP

GAGE PLANE

0-8° TYP

0.25

0.75
0.45

1.25

SEATING PLANE

LAND PATTERN RECOMMENDATION

14   13   9   8

5.01 TYP

9.27 TYP

1   2   6   7

(2.13 TYP)

1.27
TYP

0.60 TYP

SIDE VIEW

SEE DETAIL A

0.25
0.15
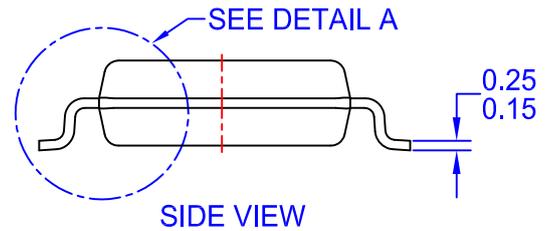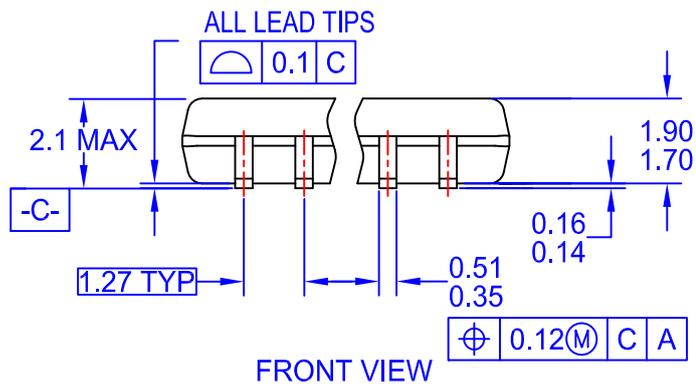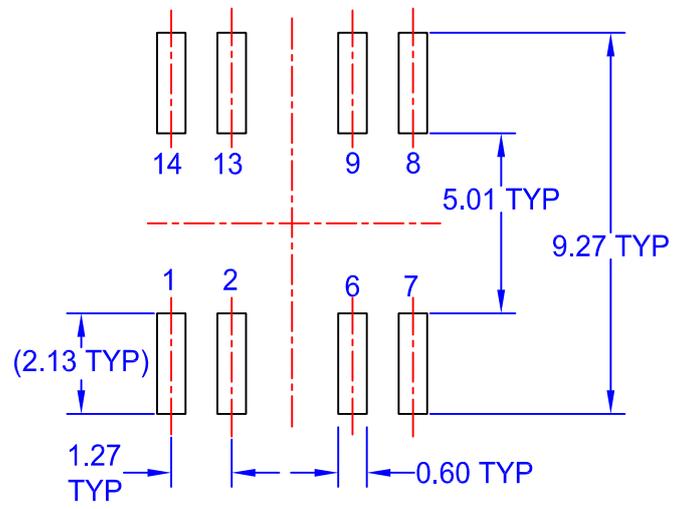
NOTES:
A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DRAWING FILENAME: MKT-M14Drev4.

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TOP VIEW

8.75 / 8.50 → A

7.62

14 | 8 → B

6.00

4.00 / 3.80

PIN #1 IDENT.

1 | 7

1.27

0.51 / 0.35

(0.33)

⊕ | 0.25 (M) | C | B | A

LAND PATTERN RECOMMENDATION

14 | 0.65 | 8

5.60

1.70

1 | 7

1.27

FRONT VIEW

1.75 MAX

1.50 / 1.25

0.25 / 0.10

C

⌒ | 0.10 | C

SIDE VIEW

A

0.25 / 0.19

DETAIL A
SCALE 16 : 1

0.50 / 0.25 X 45°

R0.10

R0.10

GAGE PLANE

8° / 0°

0.36

0.90 / 0.50

(1.04)

SEATING PLANE
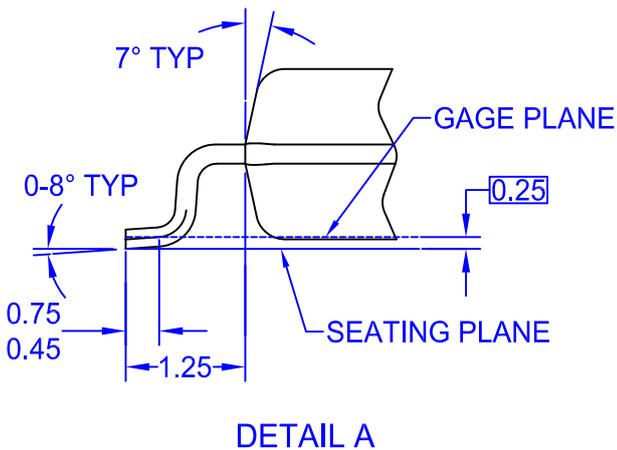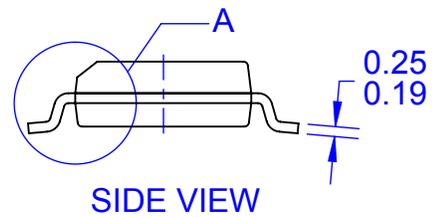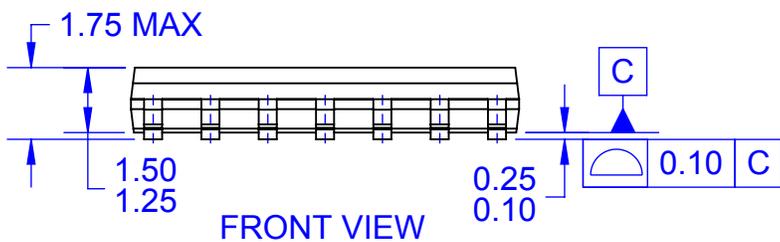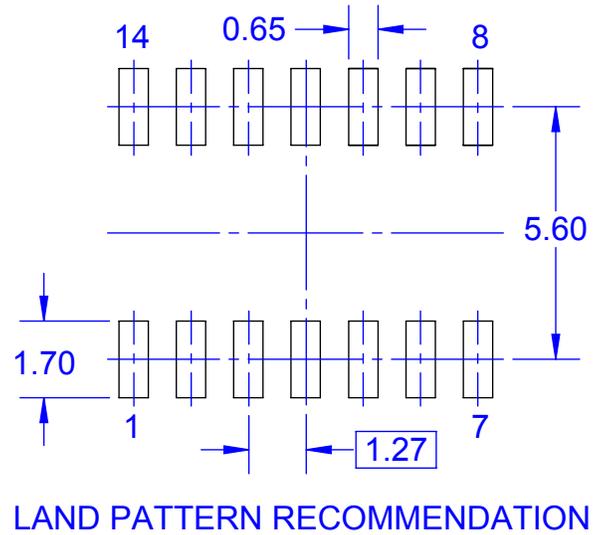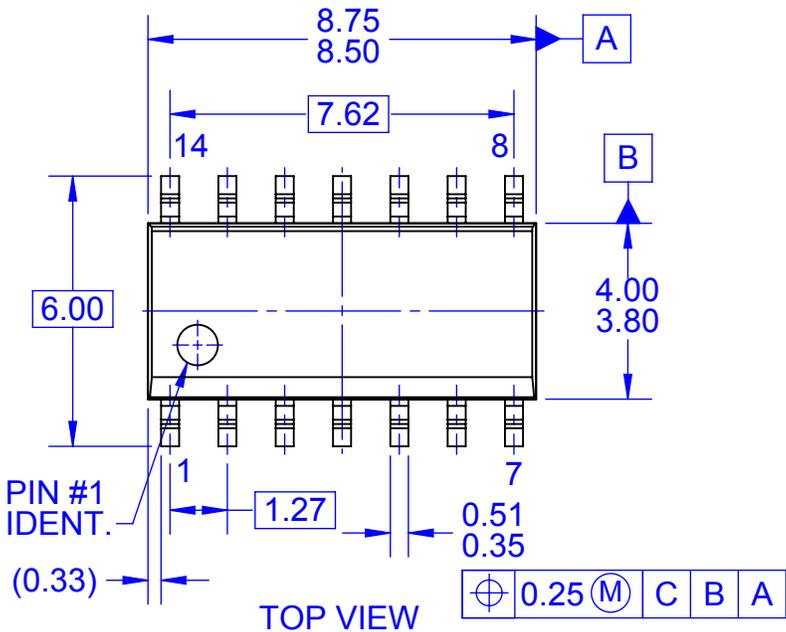
NOTES:
A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
D. LAND PATTERN STANDARD: SOIC127P600X145-14M
E. CONFORMS TO ASME Y14.5M, 2009
D. DRAWING FILENAME: MKT-M14Arev14

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PUBLICATION ORDERING INFORMATION