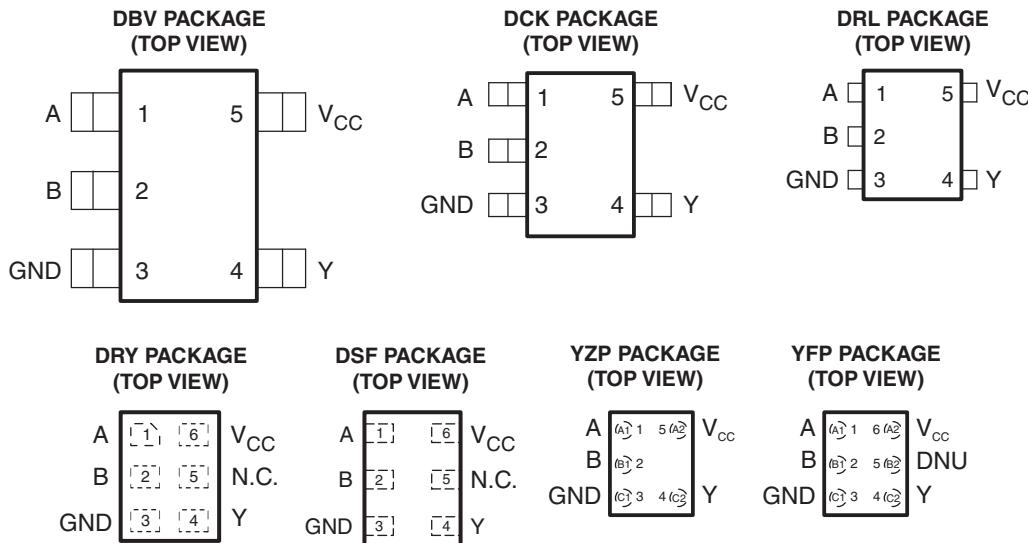


## LOW-POWER SINGLE 2-INPUT POSITIVE-NAND GATE

Check for Samples: [SN74AUP1G00](http://www.ti.com)

### FEATURES

- Available in the Texas Instruments NanoStar™ Package
- Low Static-Power Consumption ( $I_{cc} = 0.9 \mu A$  Max)
- Low Dynamic-Power Consumption ( $C_{pd} = 4 \text{ pF}$  Typ at 3.3 V)
- Low Input Capacitance ( $C_i = 1.5 \text{ pF}$  Typ)
- Low Noise Overshoot and Undershoot <10% of  $V_{CC}$
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input ( $V_{hys} = 250 \text{ mV}$  Typ at 3.3 V)
- Wide Operating  $V_{CC}$  Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 4.8 \text{ ns}$  Max at 3.3 V
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)



DNU – Do not use

N.C. – No internal connection

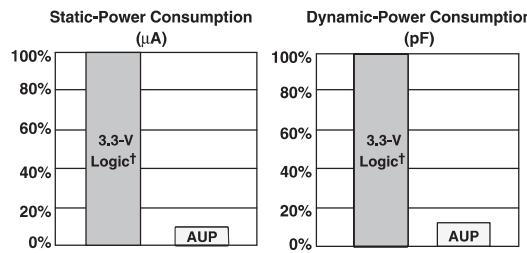
See mechanical drawings for dimensions.

### DESCRIPTION/ORDERING INFORMATION

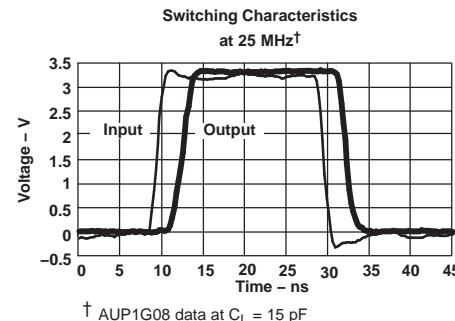
The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire  $V_{CC}$  range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity (see [Figure 1](#) and [Figure 2](#)).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



† Single, dual, and triple gates.



† AUP1G08 data at  $C_L = 15 \text{ pF}$

**Figure 1. AUP – The Lowest-Power Family**

**Figure 2. Excellent Signal Integrity**

This single 2-input positive-NAND gate performs the Boolean function  $Y = \overline{A} \cdot \overline{B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### ORDERING INFORMATION<sup>(1)</sup>

$T_A$	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(3)</sup>
$-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YFP (Pb-free)	Reel of 3000	SN74AUP1G00YFPR	_ _ _ H A _
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUP1G00YZPR	_ _ _ H A _
	QFN – DRY	Reel of 5000	SN74AUP1G00DRYR	PREVIEW
	uQFN – DSF	Reel of 5000	SN74AUP1G00DSFR	HA
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUP1G00DBVR	H00_
	SOT (SC-70) – DCK	Reel of 3000	SN74AUP1G00DCKR	HA_
	SOT (SOT-553) – DRL	Reel of 4000	SN74AUP1G00DRLR	HA_

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).
- (3) DBV/DCK/DRL: The actual top-side marking has one additional character that designates the wafer fab/assembly site. YFP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

#### FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

#### LOGIC DIAGRAM (POSITIVE LOGIC)



**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	4.6	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	4.6	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	4.6	V
$V_O$	Output voltage range in the high or low state <sup>(2)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	50	mA
$I_O$	Continuous output current		20	mA
	Continuous current through $V_{CC}$ or GND		50	mA
$\theta_{JA}$	Package thermal impedance <sup>(3)</sup>	DBV package	206	°C/W
		DCK package	252	
		DRL package	142	
		DSF package	300	
		DRY package	234	
		YFP/YZP package	132	
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	0.8	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 0.8 \text{ V}$	$V_{CC}$	V
		$V_{CC} = 1.1 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.6	
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	2	
$V_{IL}$	Low-level input voltage	$V_{CC} = 0.8 \text{ V}$	0	V
		$V_{CC} = 1.1 \text{ V to } 1.95 \text{ V}$	$0.35 \times V_{CC}$	
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.7	
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	0.9	
$V_I$	Input voltage	0	3.6	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 0.8 \text{ V}$	-20	$\mu\text{A}$
		$V_{CC} = 1.1 \text{ V}$	-1.1	
		$V_{CC} = 1.4 \text{ V}$	-1.7	
		$V_{CC} = 1.65 \text{ V}$	-1.9	
		$V_{CC} = 2.3 \text{ V}$	-3.1	
		$V_{CC} = 3 \text{ V}$	-4	
$I_{OL}$	Low-level output current	$V_{CC} = 0.8 \text{ V}$	20	mA
		$V_{CC} = 1.1 \text{ V}$	1.1	
		$V_{CC} = 1.4 \text{ V}$	1.7	
		$V_{CC} = 1.65 \text{ V}$	1.9	
		$V_{CC} = 2.3 \text{ V}$	3.1	
		$V_{CC} = 3 \text{ V}$	4	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	200	ns/V
$T_A$	Operating free-air temperature		-40	$^{\circ}\text{C}$

(1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -20 µA	0.8 V to 3.6 V	V <sub>CC</sub> – 0.1		V <sub>CC</sub> – 0.1			V
	I <sub>OH</sub> = -1.1 mA	1.1 V	0.75 × V <sub>CC</sub>		0.7 × V <sub>CC</sub>			
	I <sub>OH</sub> = -1.7 mA	1.4 V	1.11			1.03		
	I <sub>OH</sub> = -1.9 mA	1.65 V	1.32			1.3		
	I <sub>OH</sub> = -2.3 mA	2.3 V	2.05			1.97		
	I <sub>OH</sub> = -3.1 mA		1.9			1.85		
	I <sub>OH</sub> = -2.7 mA	3 V	2.72			2.67		
	I <sub>OH</sub> = -4 mA		2.6			2.55		
V <sub>OL</sub>	I <sub>OL</sub> = 20 µA	0.8 V to 3.6 V		0.1		0.1		V
	I <sub>OL</sub> = 1.1 mA	1.1 V		0.3 × V <sub>CC</sub>		0.3 × V <sub>CC</sub>		
	I <sub>OL</sub> = 1.7 mA	1.4 V		0.31		0.37		
	I <sub>OL</sub> = 1.9 mA	1.65 V		0.31		0.35		
	I <sub>OL</sub> = 2.3 mA	2.3 V		0.31		0.33		
	I <sub>OL</sub> = 3.1 mA			0.44		0.45		
	I <sub>OL</sub> = 2.7 mA	3 V		0.31		0.33		
	I <sub>OL</sub> = 4 mA			0.44		0.45		
I <sub>I</sub>	A or B input	V <sub>I</sub> = GND to 3.6 V	0 V to 3.6 V		0.1		0.5	µA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V	0 V		0.2		0.6	µA
ΔI <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V	0 V to 0.2 V		0.2		0.6	µA
I <sub>CC</sub>		V <sub>I</sub> = GND or (V <sub>CC</sub> to 3.6 V), I <sub>O</sub> = 0	0.8 V to 3.6 V		0.5		0.9	µA
ΔI <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> – 0.6 V <sup>(1)</sup> , I <sub>O</sub> = 0	3.3 V		40		50	µA
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	0 V		1.5			pF
			3.6 V		1.5			
C <sub>o</sub>		V <sub>O</sub> = GND	0 V		3			pF

(1) One input at V<sub>CC</sub> – 0.6 V, other input at V<sub>CC</sub> or GND

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C<sub>L</sub> = 5 pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	Y	0.8 V		16.6				ns
			1.2 V ± 0.1 V	2.6	7	13.8	2.1	17.1	
			1.5 V ± 0.1 V	2.9	5	9.2	2.9	11.1	
			1.8 V ± 0.15 V	2	4	7.1	2	9	
			2.5 V ± 0.2 V	1.3	2.9	4.9	1.3	6.2	
			3.3 V ± 0.3 V	1	2.4	3.8	1	4.8	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $C_L = 10 \text{ pF}$  (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A or B	Y	0.8 V		18.9				ns
			$1.2 \text{ V} \pm 0.1 \text{ V}$	1.5	8	15.7	1	18.8	
			$1.5 \text{ V} \pm 0.1 \text{ V}$	2.9	5.8	10.5	2.9	12.1	
			$1.8 \text{ V} \pm 0.15 \text{ V}$	2	4.7	8.2	2	9.8	
			$2.5 \text{ V} \pm 0.2 \text{ V}$	1.3	3.4	5.7	1.3	6.8	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	1	2.9	4.5	1	5.2	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $C_L = 15 \text{ pF}$  (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A or B	Y	0.8 V		21.3				ns
			$1.2 \text{ V} \pm 0.1 \text{ V}$	3.6	9	17.3	3.1	21.5	
			$1.5 \text{ V} \pm 0.1 \text{ V}$	2.9	6.5	11.6	2.9	14	
			$1.8 \text{ V} \pm 0.15 \text{ V}$	2	5.3	9.2	2	11.4	
			$2.5 \text{ V} \pm 0.2 \text{ V}$	1.3	3.9	6.4	1.3	8	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	1	3.3	5.1	1	6.4	

## SWITCHING CHARACTERISTICS

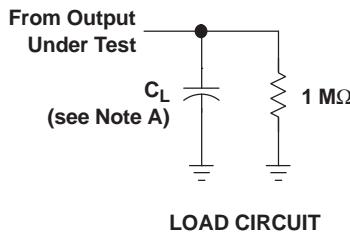
over recommended operating free-air temperature range,  $C_L = 30 \text{ pF}$  (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A or B	Y	0.8 V		28.4				ns
			$1.2 \text{ V} \pm 0.1 \text{ V}$	4.9	11.9	21.9	4.4	27.1	
			$1.5 \text{ V} \pm 0.1 \text{ V}$	2.9	8.6	14.7	2.9	17.7	
			$1.8 \text{ V} \pm 0.15 \text{ V}$	2	7.1	11.5	2	14.2	
			$2.5 \text{ V} \pm 0.2 \text{ V}$	1.3	5.3	8.1	1.3	10	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	1	4.5	6.5	1	8	

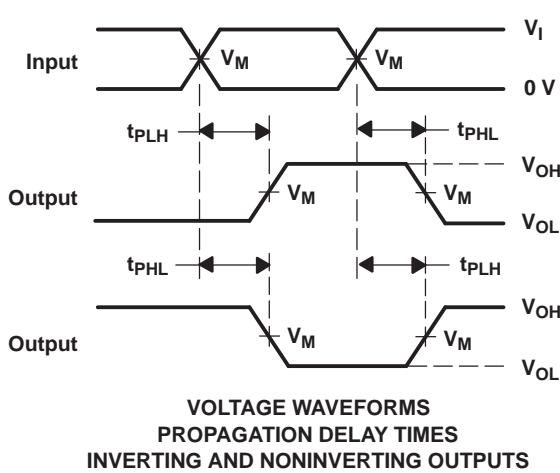
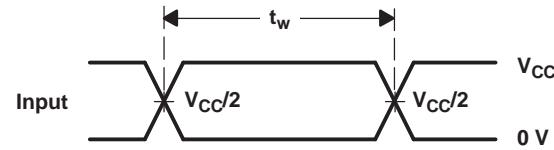
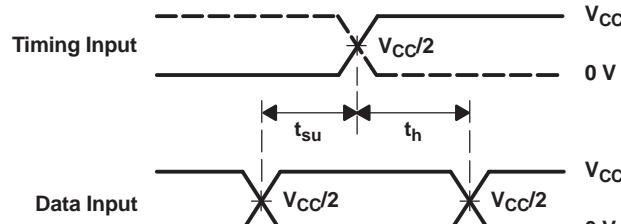
## OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$f = 10 \text{ MHz}$	0.8 V	4	pF
		$1.2 \text{ V} \pm 0.1 \text{ V}$	4	
		$1.5 \text{ V} \pm 0.1 \text{ V}$	4	
		$1.8 \text{ V} \pm 0.15 \text{ V}$	4	
		$2.5 \text{ V} \pm 0.2 \text{ V}$	4	
		$3.3 \text{ V} \pm 0.3 \text{ V}$	4	

**PARAMETER MEASUREMENT INFORMATION  
(Propagation Delays, Setup and Hold Times, and Pulse Width)**

**LOAD CIRCUIT**

	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$
$C_L$	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
$V_M$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
$V_I$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$

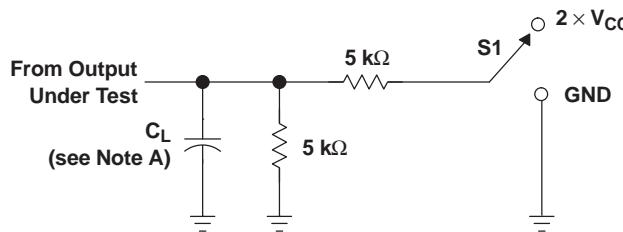

**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS  
PULSE DURATION**

**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**

NOTES:

- $C_L$  includes probe and jig capacitance.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ , slew rate  $\geq 1 \text{ V/ns}$ .
- The outputs are measured one at a time, with one transition per measurement.
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**

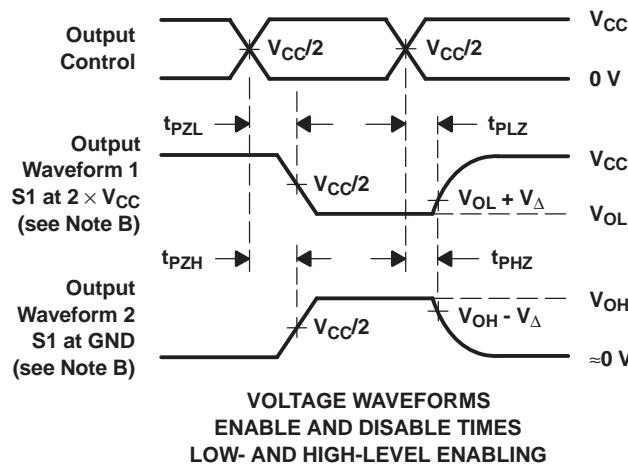
### PARAMETER MEASUREMENT INFORMATION (Enable and Disable Times)



TEST	S1
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

LOAD CIRCUIT

	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$
$C_L$	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
$V_M$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
$V_I$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$
$V_\Delta$	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ , slew rate  $\geq 1 \text{ V/ns}$ .
- The outputs are measured one at a time, with one transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74AUP1G00DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G00DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G00DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G00DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G00DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G00DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G00DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G00DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G00DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G00DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G00DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G00DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G00DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G00DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G00DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM
SN74AUP1G00YFPR	ACTIVE	DSBGA	YFP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
SN74AUP1G00YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame

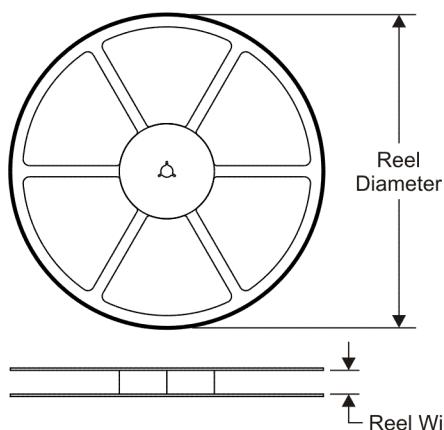
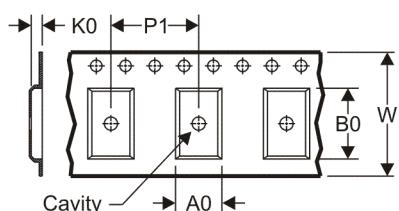
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retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

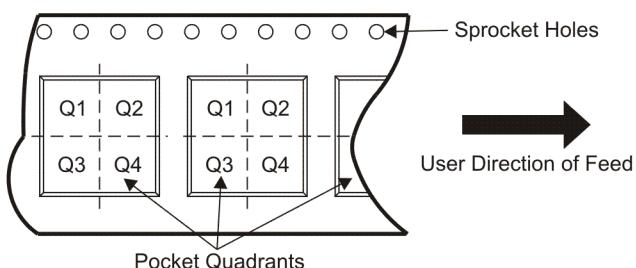
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G00DBVR	SOT-23	DBV	5	3000	180.0	9.2	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G00DBVT	SOT-23	DBV	5	250	180.0	9.2	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G00DCKR	SC70	DCK	5	3000	180.0	9.2	2.24	2.34	1.22	4.0	8.0	Q3
SN74AUP1G00DCKT	SC70	DCK	5	250	180.0	9.2	2.24	2.34	1.22	4.0	8.0	Q3
SN74AUP1G00DRLR	SOT	DRL	5	4000	180.0	9.2	1.78	1.78	0.69	4.0	8.0	Q3
SN74AUP1G00YZPR	DSBGA	YZP	5	3000	180.0	8.4	1.02	1.52	0.63	4.0	8.0	Q1

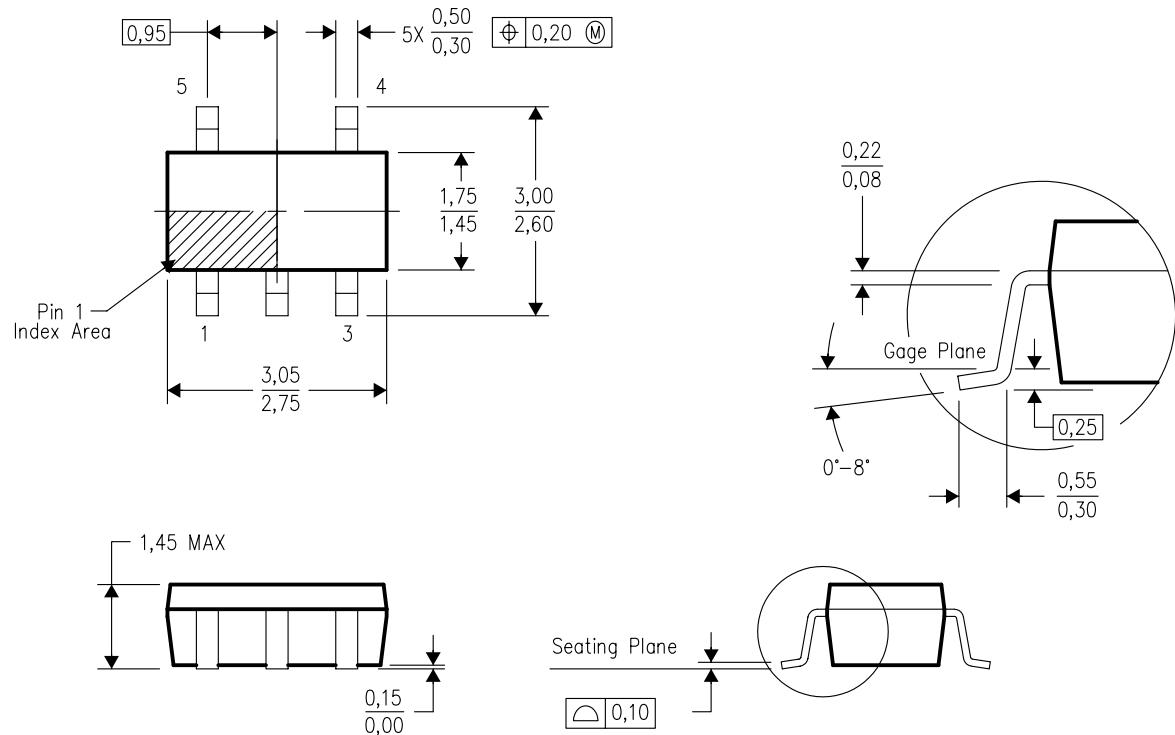
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G00DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AUP1G00DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74AUP1G00DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74AUP1G00DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74AUP1G00DRLR	SOT	DRL	5	4000	202.0	201.0	28.0
SN74AUP1G00YZPR	DSBGA	YZP	5	3000	220.0	220.0	34.0

## DBV (R-PDSO-G5)

## PLASTIC SMALL-OUTLINE PACKAGE

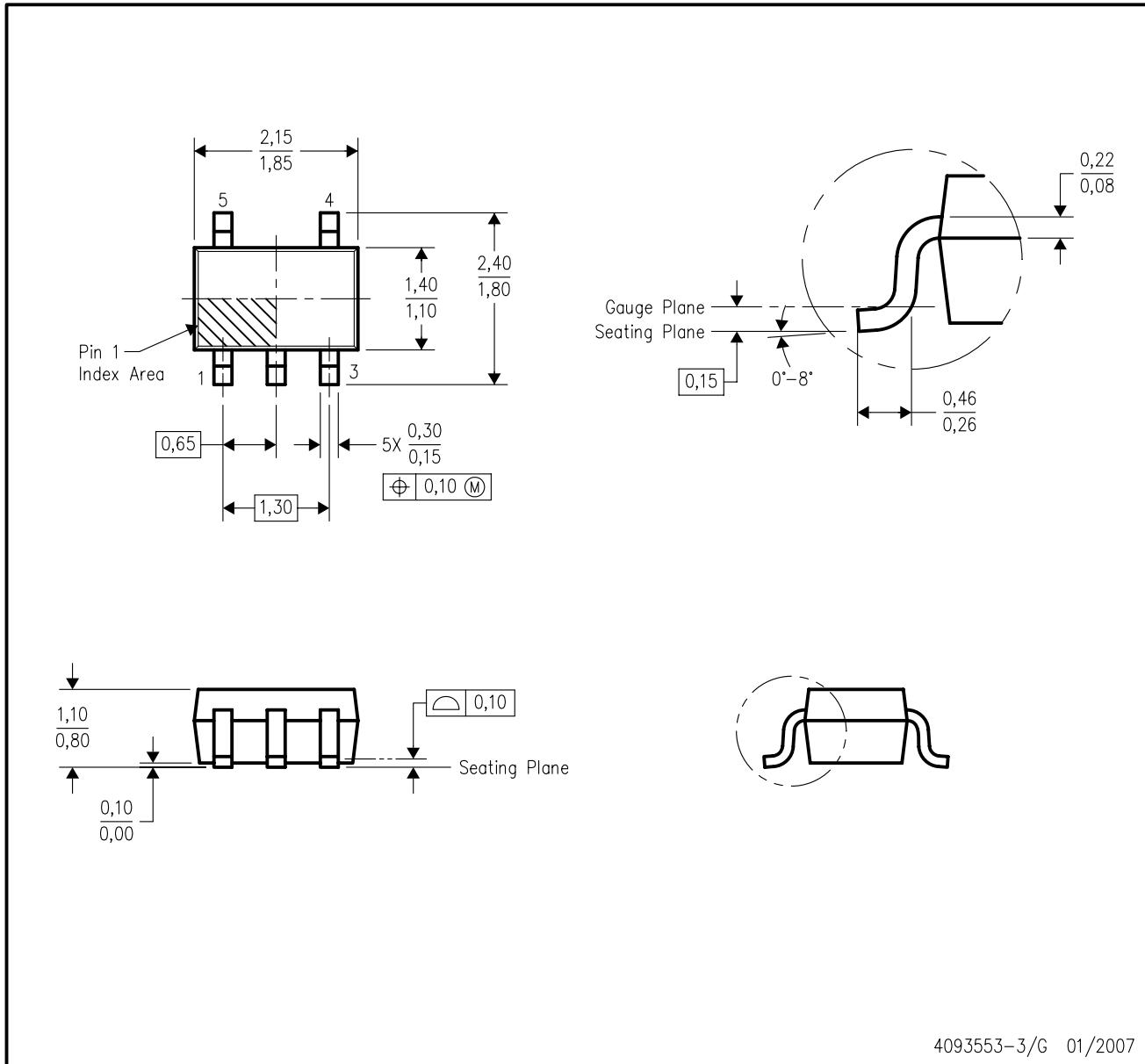


4073253-4/K 03/2006

NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.  
D. Falls within JEDEC MO-178 Variation AA.

## DCK (R-PDSO-G5)

## PLASTIC SMALL-OUTLINE PACKAGE



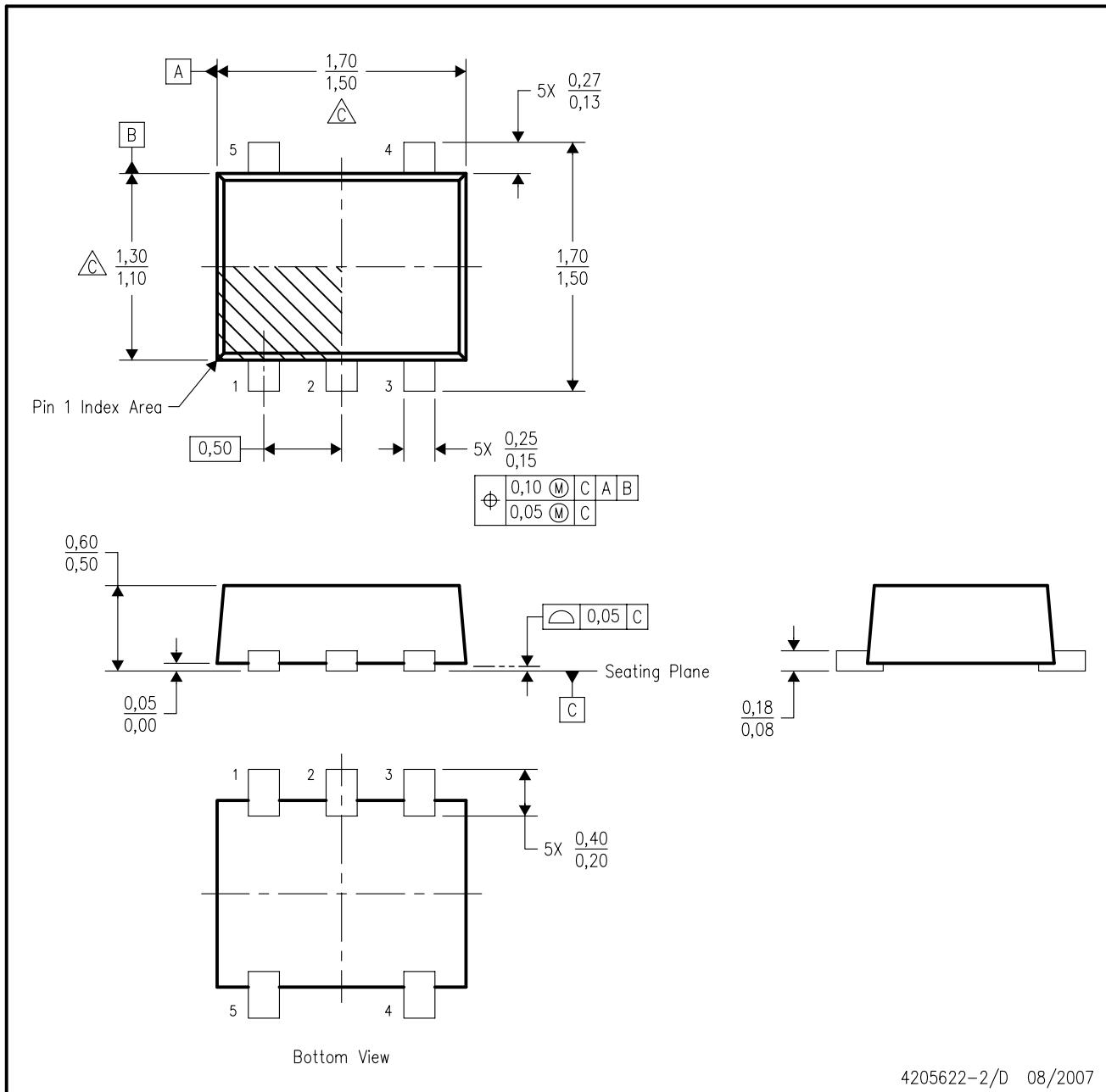
4093553-3/G 01/2007

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-203 variation AA.

## DRL (R-PDSO-N5)

## PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
B. This drawing is subject to change without notice.

 THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.

 Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.

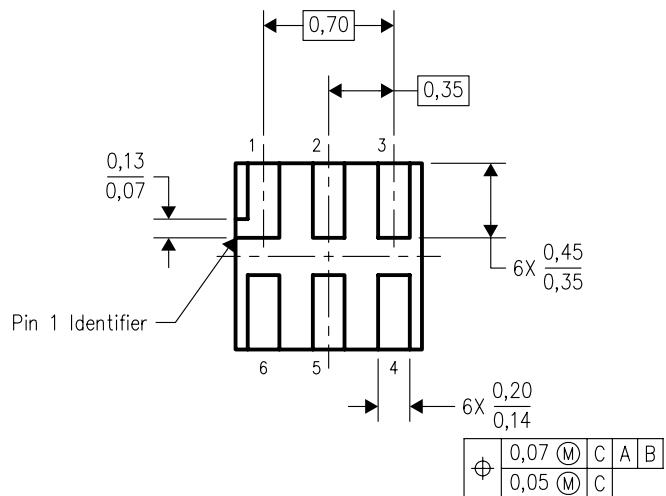
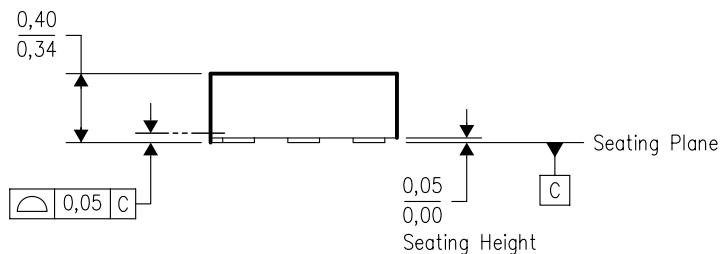
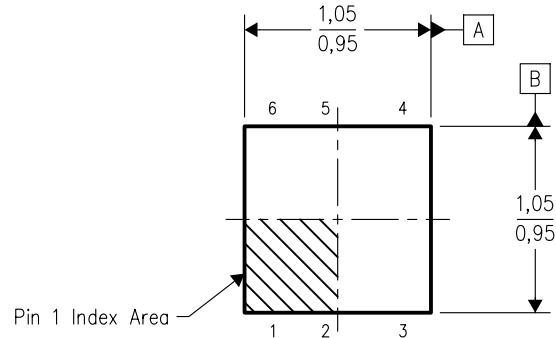
D. JEDEC package registration is pending.

D. JEDEC package registration is pending.

## MECHANICAL DATA

DSF (S-PDSO-N6)

PLASTIC SMALL OUTLINE



Bottom View

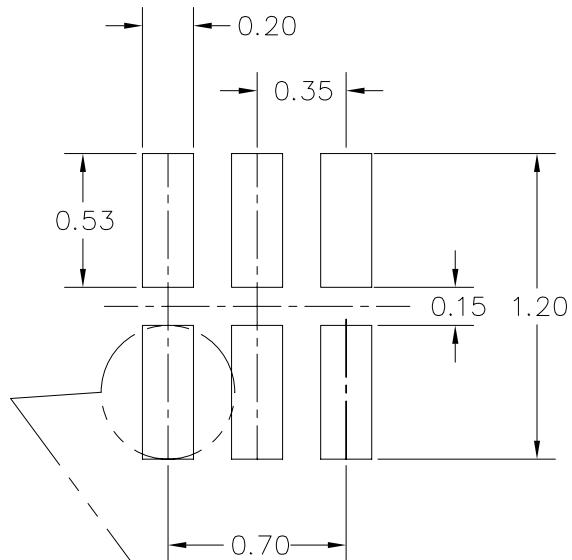
4208186/D 11/2007

NOTES:

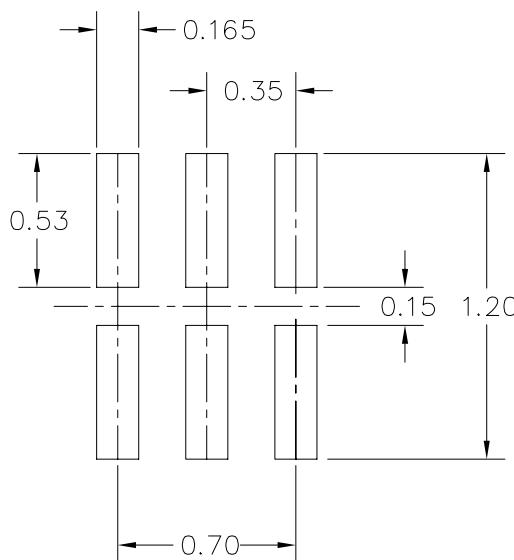
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- SON (Small Outline No-Lead) package configuration.
- This package complies to JEDEC MO-287 variation X2AAF.

DSF (S-PDSO-N6)

Land Pattern



Stencil Pattern



Contact your PCB vendor for  
allowable Solder Mask clearance (Note I.)

4210277/A 06/09

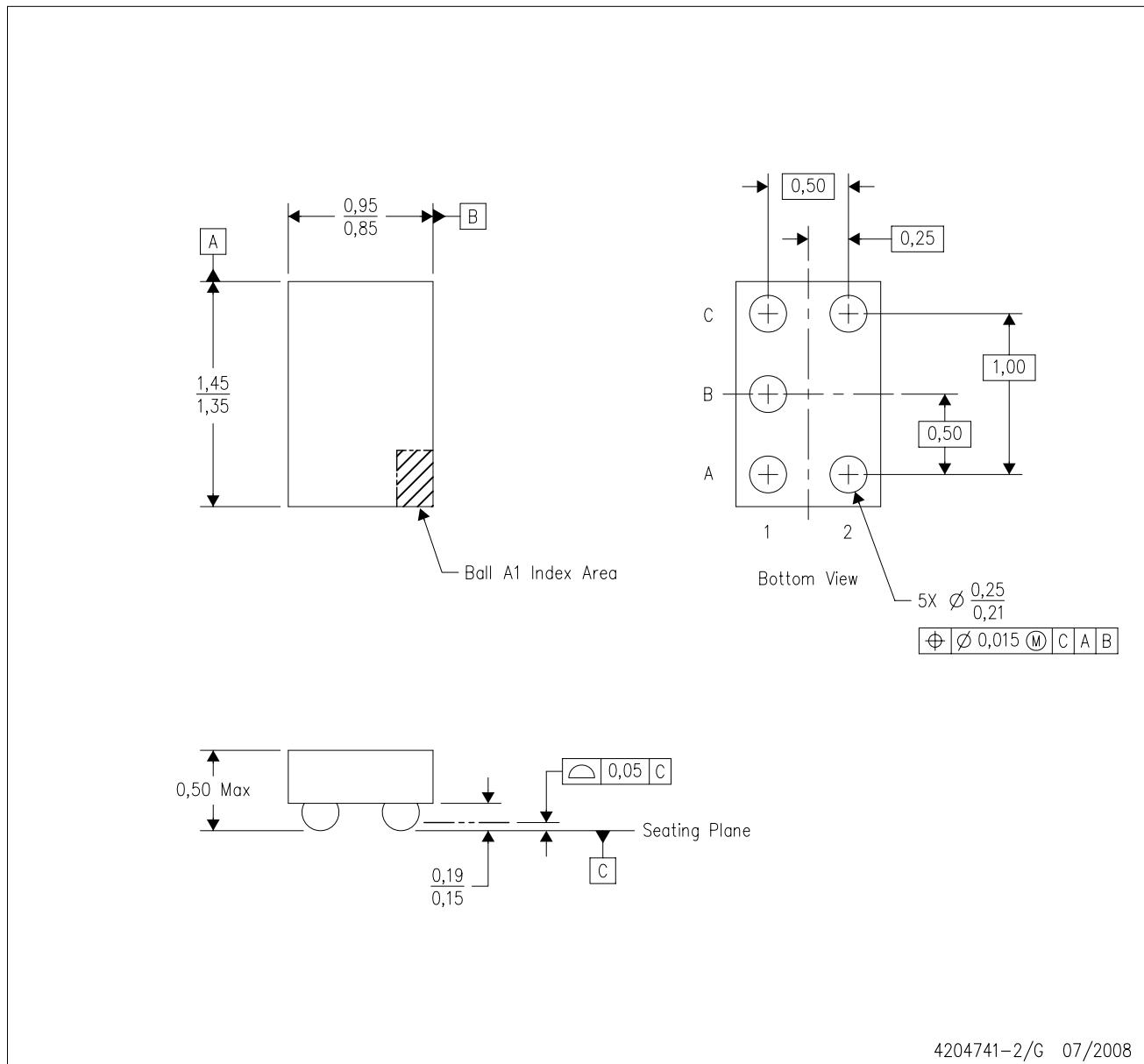
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
- E. Maximum stencil thickness 0.1016 mm (4 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Over-printing land for acceptable area ratio is not viable due to land width and bridging potential. Customer may further reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.
- H. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
- I. Component placement force should be minimized to prevent excessive paste block deformation.

## MECHANICAL DATA

YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



4204741-2/G 07/2008

NOTES:

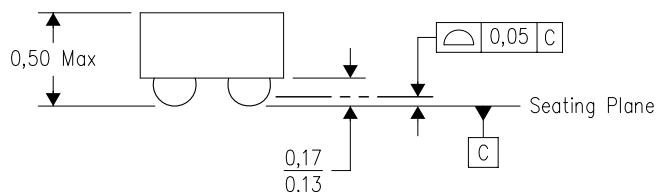
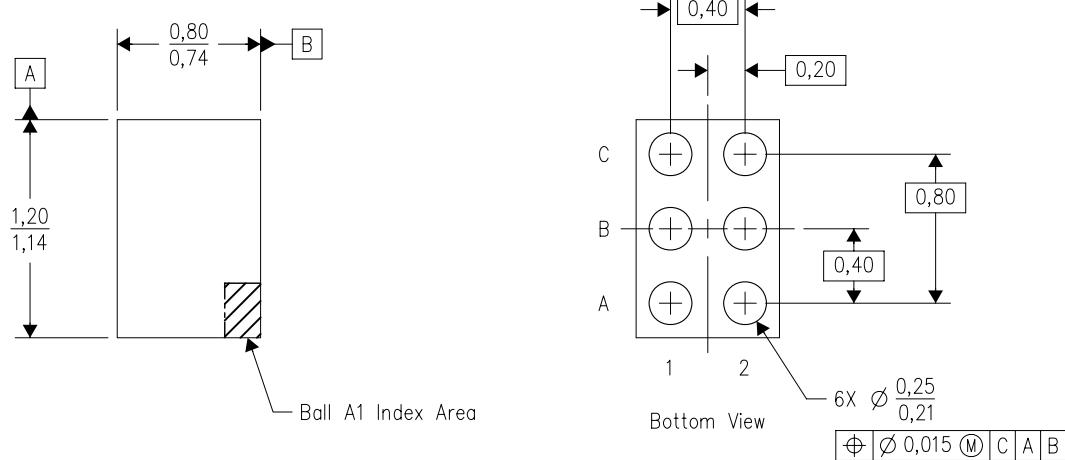
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- NanoFree™ package configuration.
- This package is lead-free. Refer to the 5 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

## MECHANICAL DATA

YFP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



4206986-3/0 08/2008

NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- NanoFree™ package configuration.
- This is a Pb-free solder ball design.

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DLP® Products <a href="http://www.dlp.com">www.dlp.com</a>	Communications and Telecom <a href="http://www.ti.com/communications">www.ti.com/communications</a>
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RFID <a href="http://www.ti-rfid.com">www.ti-rfid.com</a>	Space, Avionics & Defense <a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
RF/IF and ZigBee® Solutions <a href="http://www.ti.com/lprf">www.ti.com/lprf</a>	Video and Imaging <a href="http://www.ti.com/video">www.ti.com/video</a>
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