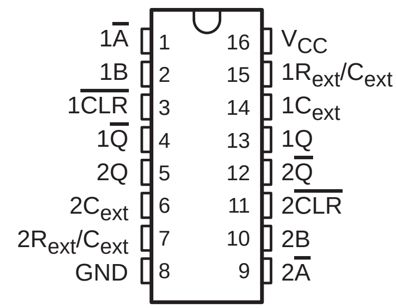
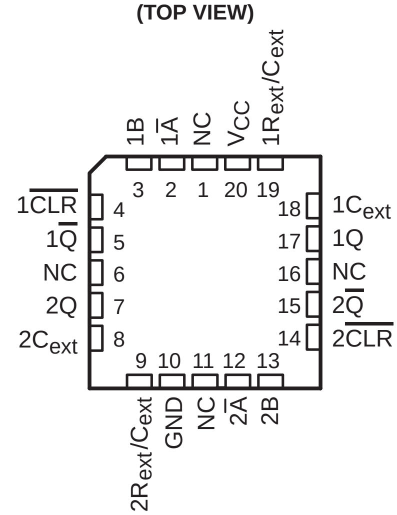
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Process**
- **Schmitt-Trigger Circuitry on $\overline{A}$, B, and $\overline{CLR}$ Inputs for Slow Input Transition Rates**
- **Edge Triggered From Active-High or Active-Low Gated Logic Inputs**
- **Retriggerable for Very Long Output Pulses, up to 100% Duty Cycle**
- **Overriding Clear Terminates Output Pulse**
- **Glitch-Free Power-Up Reset on Outputs**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

SN54LV123A . . . J OR W PACKAGE
SN74LV123A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV123A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The ’LV123A devices are dual retriggerable monostable multivibrators designed for 2-V to 5.5-V V_{CC} operation.

These edge-triggered multivibrators feature output pulse-duration control by three methods. In the first method, the $\overline{A}$ input is low and the B input goes high. In the second method, the B input is high and the $\overline{A}$ input goes low. In the third method, the $\overline{A}$ input is low, the B input is high, and the clear ($\overline{CLR}$) input goes high.

The output pulse duration is programmable by selecting external resistance and capacitance values. The external timing capacitor must be connected between C_{ext} and R_{ext}/C_{ext} (positive) and an external resistor connected between R_{ext}/C_{ext} and V_{CC}. To obtain variable pulse durations, connect an external variable resistance between R_{ext}/C_{ext} and V_{CC}. The output pulse duration can also be reduced by taking $\overline{CLR}$ low.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. The $\overline{A}$, B, and $\overline{CLR}$ inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

description (continued)

Once triggered, the basic pulse duration can be extended by retriggering the gated low-level-active ($\overline{A}$) or high-level-active (B) input. Pulse duration can be reduced by taking $\overline{CLR}$ low. The input/output timing diagram illustrates pulse control by retriggering the inputs and early clearing.

The variance in output pulse duration from device to device typically is less than ±0.5% for given external timing components. An example of this distribution for the ’LV123A is shown in Figure 11. Variations in output pulse width versus supply voltage and temperature are shown in Figure 7.

During power up, Q outputs will be in the high state, and $\overline{Q}$ outputs will be in the low state. The outputs will be glitch free without applying a reset pulse.

Pin assignments for these devices are identical to those of the ’AHC123A and ’AHCT123A devices for interchangeability when allowed.

The SN54LV123A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV123A is characterized for operation from –40°C to 85°C.

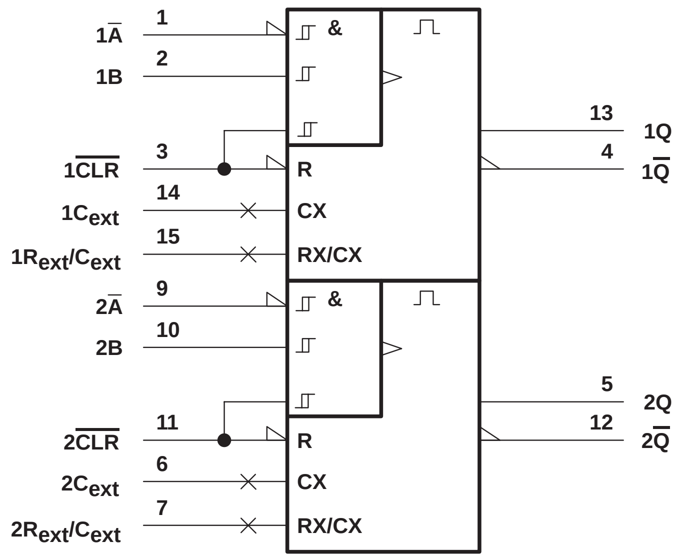
For additional application information on multivibrators, see the application report *Designing With The SN74AHC123A and SN74AHCT123A*, literature number SCLA014.

FUNCTION TABLE
(each multivibrator)

INPUTS			OUTPUTS	
$\overline{CLR}$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L†	H†
X	X	L	L†	H†
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔
↑	L	H	⊓	⊔

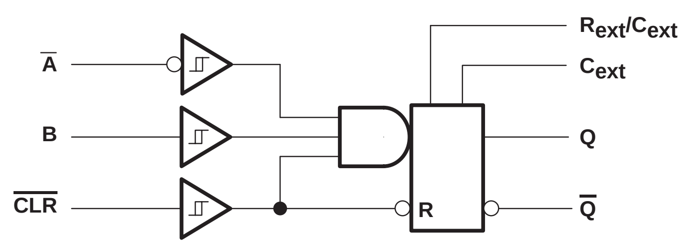
† These outputs are based on the assumption that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the setup.

logic symbol†

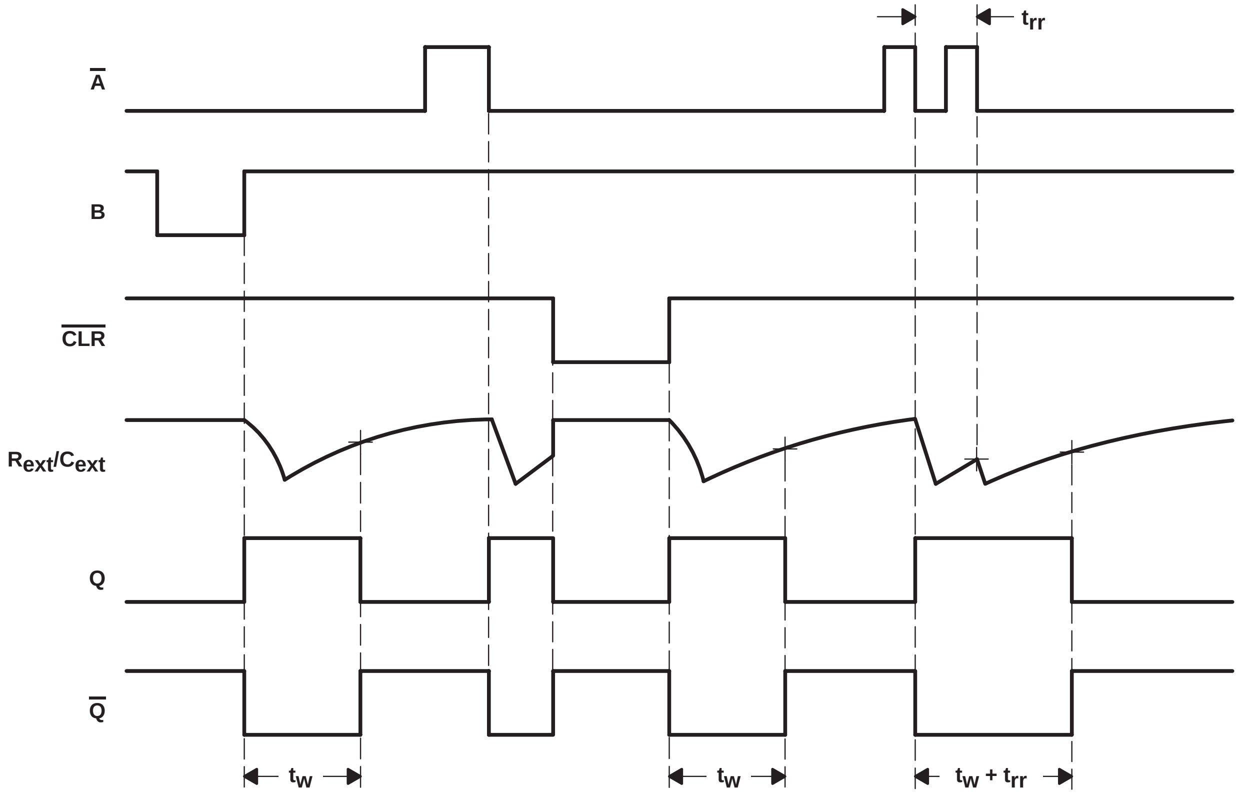


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram, each multivibrator (positive logic)



input/output timing diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range in high or low state, V_O (see Notes 1 and 2)	–0.5 V to V_{CC} + 0.5 V
Output voltage range in power-off state, V_O (see Note 1)	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	113°C/W
DB package	131°C/W
DGV package	180°C/W
NS package	111°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LV123A		SN74LV123A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	µA
		V_{CC} = 2.3 V to 2.7 V		–2		–2	mA
		V_{CC} = 3 V to 3.6 V		–6		–6	
		V_{CC} = 4.5 V to 5.5 V		–12		–12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	µA
		V_{CC} = 2.3 V to 2.7 V		2		2	mA
		V_{CC} = 3 V to 3.6 V		6		6	
		V_{CC} = 4.5 V to 5.5 V		12		12	
R_{ext}	External timing resistance	V_{CC} = 2 V	5k		5k		Ω
		$V_{CC} \geq 3$ V	1k		1k		
C_{ext}	External timing capacitance		No restriction		No restriction		pF
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		1		1		ms/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	SN54LV123A			SN74LV123A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}		I_{OH} = –50 μA	2 V to 5.5 V	V_{CC}–0.1			V_{CC}–0.1			V
		I_{OH} = –2 mA	2.3 V	2			2			
		I_{OH} = –6 mA	3 V	2.48			2.48			
		I_{OH} = –12 mA	4.5 V	3.8			3.8			
V_{OL}		I_{OL} = 50 μA	2 V to 5.5 V			0.1			0.1	V
		I_{OL} = 2 mA	2.3 V			0.4			0.4	
		I_{OL} = 6 mA	3 V			0.44			0.44	
		I_{OL} = 12 mA	4.5 V			0.55			0.55	
I_I	R_{ext}/C_{ext}†	$V_I = V_{CC}$ or GND	2 V to 5.5 V			±2.5			±2.5	μA
	$\overline{A}$, B, and $\overline{CLR}$	$V_I = V_{CC}$ or GND	0 V			±1			±1	
			5.5 V			±1			±1	
I_{CC}	Quiescent	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			20			20	μA
I_{CC}	Active state (per circuit)	$V_I = V_{CC}$ or GND, $R_{ext}/C_{ext} = 0.5\ V_{CC}$	2.3 V			220			220	μA
			3 V			280			280	
			4.5 V			650			650	
			5.5 V			975			975	
I_{off}		V_I or V_O = 0 to 5.5 V	0 V						5	μA
C_i		$V_I = V_{CC}$ or GND	3.3 V		1.9			1.9		pF
			5 V		1.9			1.9		

† This test is performed with the terminal in the off-state condition.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

			TEST CONDITIONS		T_A = 25°C			SN54LV123A		SN74LV123A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$			6			6.5		6.5		ns
		$\overline{A}$ or B trigger			6			6.5		6.5		
t_{rr}	Pulse retrigger time		R_{ext} = 1 kΩ	C_{ext} = 100 pF	‡	94		‡		‡		ns
				C_{ext} = 0.01 μF	‡	2		‡		‡		μs

‡ See retriggering data in the *application information* section.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			TEST CONDITIONS		T_A = 25°C			SN54LV123A		SN74LV123A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$			5			5		5		ns
		$\overline{A}$ or B trigger			5			5		5		
t_{rr}	Pulse retrigger time		R_{ext} = 1 kΩ	C_{ext} = 100 pF	‡	76		‡		‡		ns
				C_{ext} = 0.01 μF	‡	1.8		‡		‡		μs

‡ See retriggering data in the *application information* section.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			TEST CONDITIONS		T_A = 25°C			SN54LV123A		SN74LV123A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{\text{CLR}}$			5			5		5		ns
		$\overline{\text{A}}$ or B trigger			5			5		5		
t_{rr}	Pulse retrigger time		R_{ext} = 1 kΩ	C_{ext} = 100 pF	†	59		†		†		ns
				C_{ext} = 0.01 µF	†	1.5		†		†		µs

† See retriggering data in the *application information* section.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54LV123A		SN74LV123A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	$\overline{\text{A}}$ or B	Q or $\overline{\text{Q}}$	C_L = 15 pF		14.5*	31.4*	1*	37*	11	37	ns
	$\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$			13*	25*	1*	29.5*	1	29.5	
	$\overline{\text{CLR}}$ trigger	Q or $\overline{\text{Q}}$			15.1*	33.4*	1*	39*	1	39	
t_{pd}	$\overline{\text{A}}$ or B	Q or $\overline{\text{Q}}$	C_L = 50 pF		16.6	36	1	42	1	42	ns
	$\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$			14.7	32.8	1	34.5	1	34.5	
	$\overline{\text{CLR}}$ trigger	Q or $\overline{\text{Q}}$			17.4	38	1	44	1	44	
t_w‡		Q or $\overline{\text{Q}}$	C_L = 50 pF, C_{ext} = 28 pF, R_{ext} = 2 kΩ		197	260		320		320	ns
			C_L = 50 pF, C_{ext} = 0.01 µF, R_{ext} = 10 kΩ	90	100	110	90	110	90	110	µs
			C_L = 50 pF, C_{ext} = 0.1 µF, R_{ext} = 10 kΩ	0.9	1	1.1	0.9	1.1	0.9	1.1	ms
Δt_w§			C_L = 50 pF		±1						%

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
‡ t_w = Duration of pulse at Q and $\overline{\text{Q}}$ outputs
§ Δt_w = Output pulse duration variation (Q and $\overline{\text{Q}}$) between circuits in same package

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54LV123A		SN74LV123A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	$\overline{A}$ or B	Q or $\overline{Q}$	C_L = 15 pF		10.2*	20.6*	1*	24*	1	24	ns
	$\overline{CLR}$	Q or $\overline{Q}$			9.3*	15.8*	1*	18.5*	1	18.5	
	$\overline{CLR}$ trigger	Q or $\overline{Q}$			10.6*	22.4*	1*	26*	1	26	
t_{pd}	$\overline{A}$ or B	Q or $\overline{Q}$	C_L = 50 pF		11.8	24.1	1	27.5	1	27.5	ns
	$\overline{CLR}$	Q or $\overline{Q}$			10.5	19.3	1	22	1	22	
	$\overline{CLR}$ trigger	Q or $\overline{Q}$			12.3	25.9	1	29.5	1	29.5	
t_w†		Q or $\overline{Q}$	C_L = 50 pF, C_{ext} = 28 pF, R_{ext} = 2 kΩ		182	240		300		300	ns
			C_L = 50 pF, C_{ext} = 0.01 μF, R_{ext} = 10 kΩ	90	100	110	90	110	90	110	μs
			C_L = 50 pF, C_{ext} = 0.1 μF, R_{ext} = 10 kΩ	0.9	1	1.1	0.9	1.1	0.9	1.1	ms
Δt_w‡			C_L = 50 pF		±1						%

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† t_w = Duration of pulse at Q and $\overline{Q}$ outputs
‡ Δt_w = Output pulse duration variation (Q and $\overline{Q}$) between circuits in same package

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

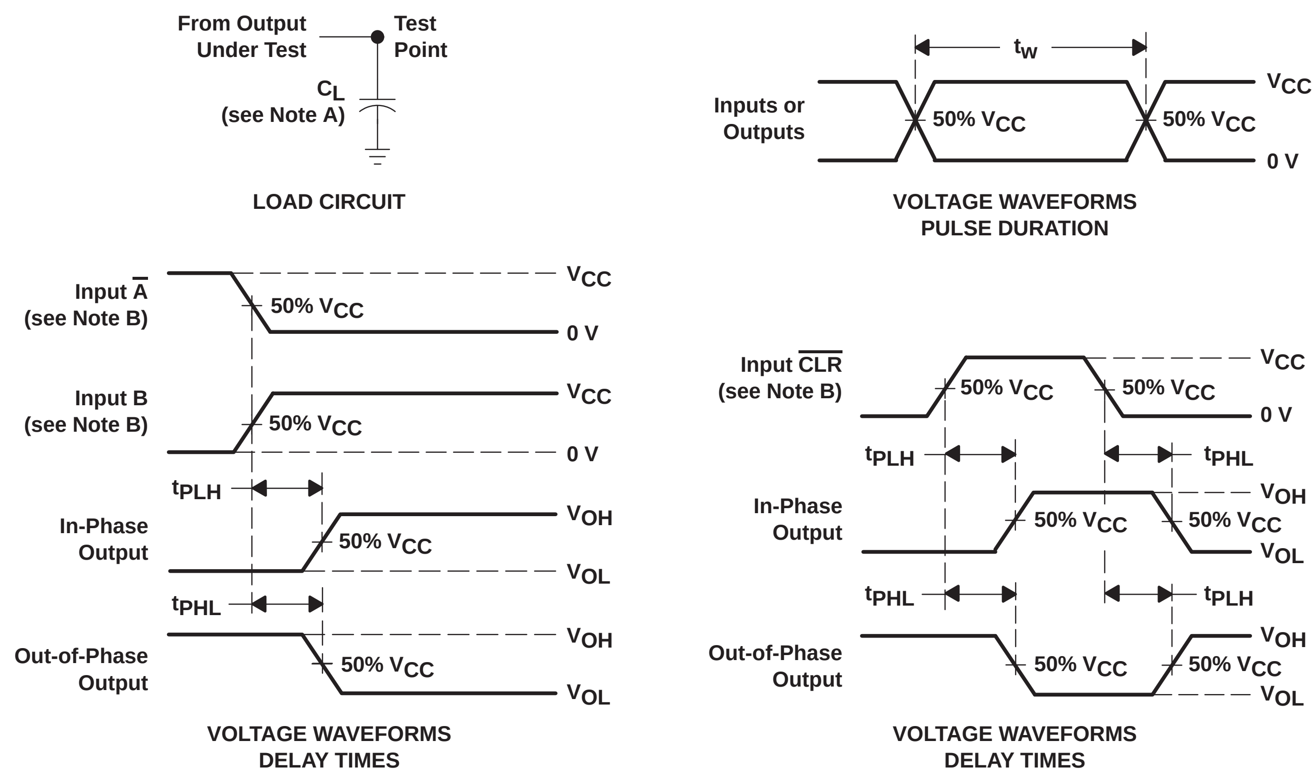
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54LV123A		SN74LV123A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	$\overline{A}$ or B	Q or $\overline{Q}$	C_L = 15 pF		7.1*	12*	1*	14*	1	14	ns
	$\overline{CLR}$	Q or $\overline{Q}$			6.5*	9.4*	1*	11*	1	11	
	$\overline{CLR}$ trigger	Q or $\overline{Q}$			7.4*	12.9*	1*	15*	1	15	
t_{pd}	$\overline{A}$ or B	Q or $\overline{Q}$	C_L = 50 pF		8.3	14	1	16	1	16	ns
	$\overline{CLR}$	Q or $\overline{Q}$			7.4	11.4	1	13	1	13	
	$\overline{CLR}$ trigger	Q or $\overline{Q}$			8.7	14.9	1	17	1	17	
t_w†		Q or $\overline{Q}$	C_L = 50 pF, C_{ext} = 28 pF, R_{ext} = 2 kΩ		167	200		240		240	ns
			C_L = 50 pF, C_{ext} = 0.01 μF, R_{ext} = 10 kΩ	90	100	110	90	110	90	110	μs
			C_L = 50 pF, C_{ext} = 0.1 μF, R_{ext} = 10 kΩ	0.9	1	1.1	0.9	1.1	0.9	1.1	ms
Δt_w‡					±1						%

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† t_w = Duration of pulse at Q and $\overline{Q}$ outputs
‡ Δt_w = Output pulse duration variation (Q and $\overline{Q}$) between circuits in same package

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	3.3 V	44	pF
			5 V	49	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

caution in use

To prevent malfunctions due to noise, connect a high-frequency capacitor between V_{CC} and GND, and keep the wiring between the external components and C_{ext} and R_{ext}/C_{ext} terminals as short as possible.

power-down considerations

Large values of C_{ext} may cause problems when powering down the ’LV123A because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge from V_{CC} through the protection diodes at pin 2 or pin 14. Current through the input protection diodes must be limited to 30 mA; therefore, the turn-off time of the V_{CC} power supply must not be faster than $t = V_{CC} \times C_{ext}/30$ mA. For example, if V_{CC} = 5 V and C_{ext} = 15 pF, the V_{CC} supply must turn off no faster than t = (5 V) × (15 pF)/30mA = 2.5 ms. Usually, this is not a problem because power supplies are heavily filtered and cannot discharge at this rate. When a more rapid decrease of V_{CC} to zero occurs, the ’LV123A may sustain damage. To avoid this possibility, use external clamping diodes.

output pulse duration

The output pulse duration, t_W, is determined primarily by the values of the external capacitance (C_T) and timing resistance (R_T). The timing components are connected as shown in Figure 2.

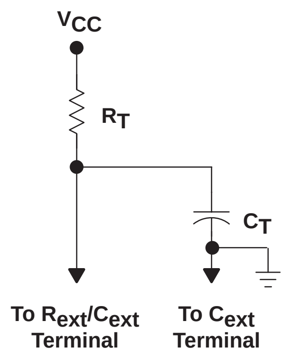


Figure 2. Timing-Component Connections

The pulse duration is given by:

$$t_w = K \times R_T \times C_T \qquad (1)$$

if C_T is ≥ 1000 pF, K = 1.0

or

if C_T is < 1000 pF, K can be determined from Figure 9

where:

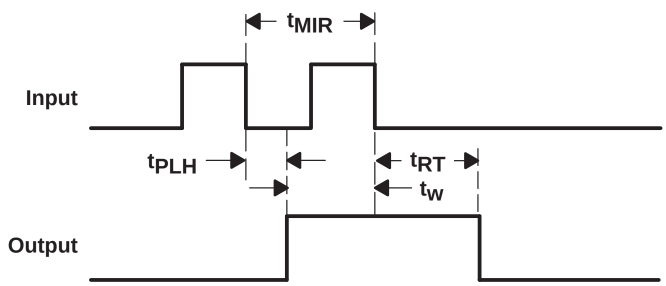
t_W = pulse duration in ns
R_T = external timing resistance in kΩ
C_T = external capacitance in pF
K = multiplier factor

Equation 1 and Figures 5 or 6 can be used to determine values for pulse duration, external resistance, and external capacitance.

APPLICATION INFORMATION

retriggering data

The minimum input retriggering time (t_{MIR}) is the minimum time required after the initial signal before retriggering the input. After t_{MIR}, the device retriggers the output. Experimentally, it also can be shown that, to retrigger the output pulse, the two adjacent input signals should be t_{MIR} apart, where $t_{MIR} = 0.30 \times t_W$. The retrigger pulse duration is calculated as shown in Figure 3.

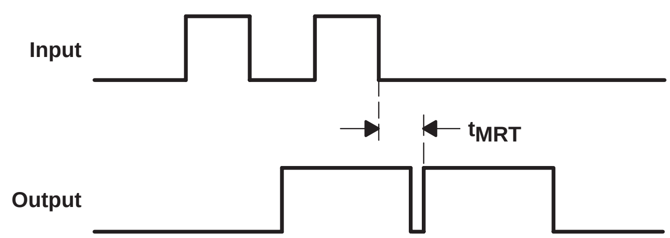


$t_{RT} = t_W + t_{PLH} = (K \times R_T \times C_T) + t_{PLH}$

Where:
t_{MIR} = Minimum Input Retriggering Time
t_{PLH} = Propagation Delay
t_{RT} = Retrigger Time
t_W = Output Pulse Duration Before Retriggering

Figure 3. Retrigger Pulse Duration

The minimum value from the end of the input pulse to the beginning of the retriggered output should be approximately 15 ns to ensure a retriggered output. This is illustrated in Figure 4.



t_{MRT} = Minimum Time Between the End of the Second Input Pulse and the Beginning of the Retriggered Output
t_{MRT} = 15 ns

Figure 4. Input/Output Requirements

APPLICATION INFORMATION†

OUTPUT PULSE DURATION vs EXTERNAL TIMING CAPACITANCE

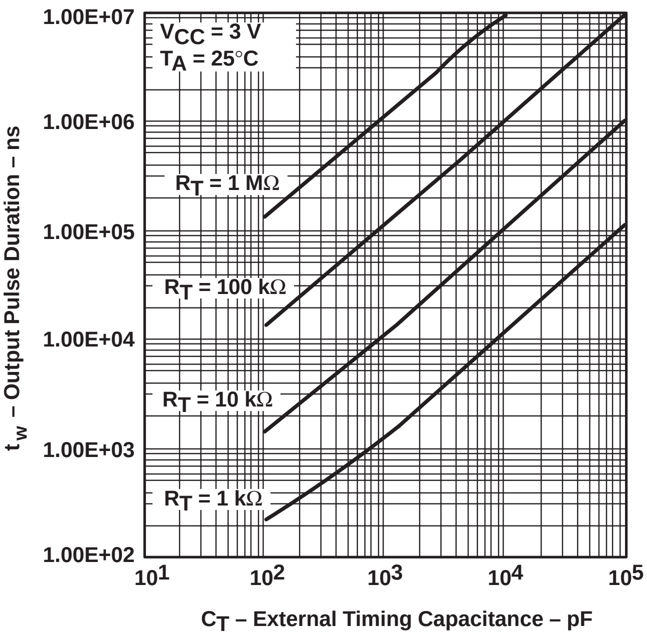


Figure 5

OUTPUT PULSE DURATION vs EXTERNAL TIMING CAPACITANCE

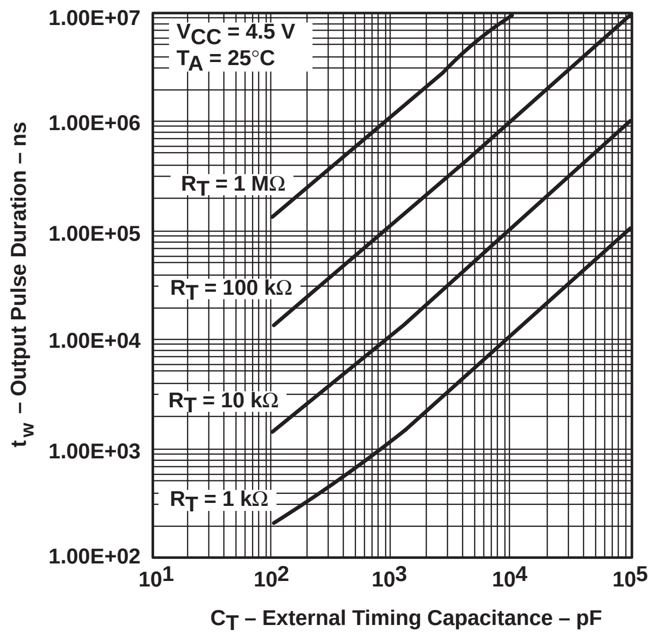


Figure 6

VARIATION IN OUTPUT PULSE DURATION vs TEMPERATURE

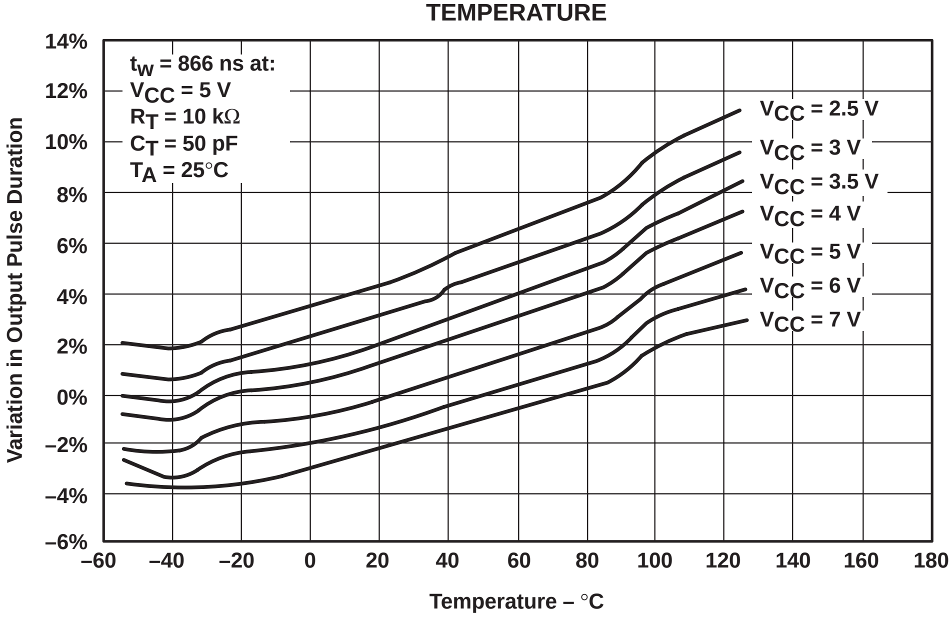


Figure 7

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

APPLICATION INFORMATION†

MINIMUM TRIGGER TIME vs V_{CC} CHARACTERISTICS

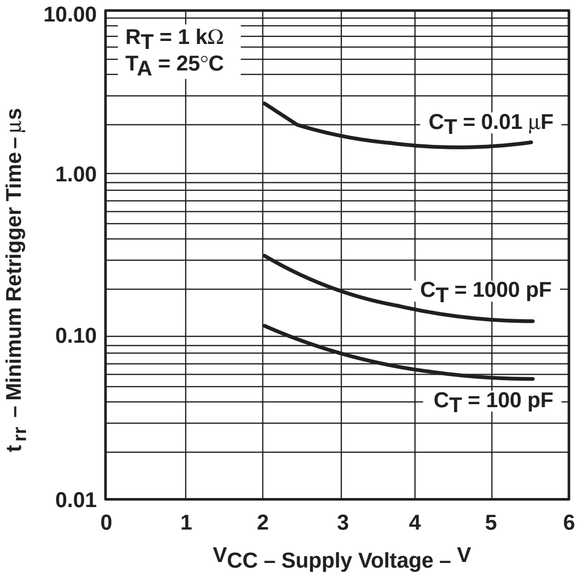


Figure 8

OUTPUT PULSE DURATION CONSTANT vs SUPPLY VOLTAGE

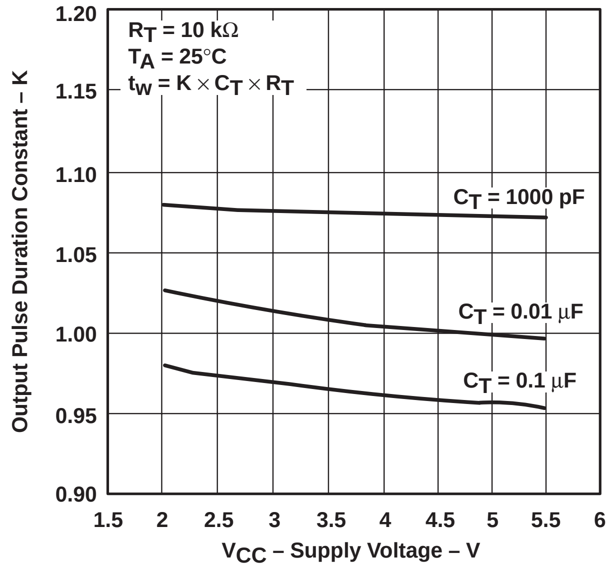


Figure 9

EXTERNAL CAPACITANCE vs MULTIPLIER FACTOR

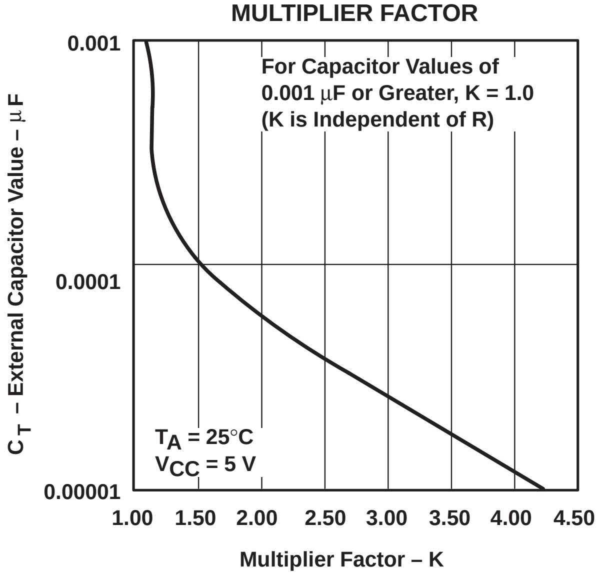


Figure 10

DISTRIBUTION OF UNITS vs OUTPUT PULSE DURATION

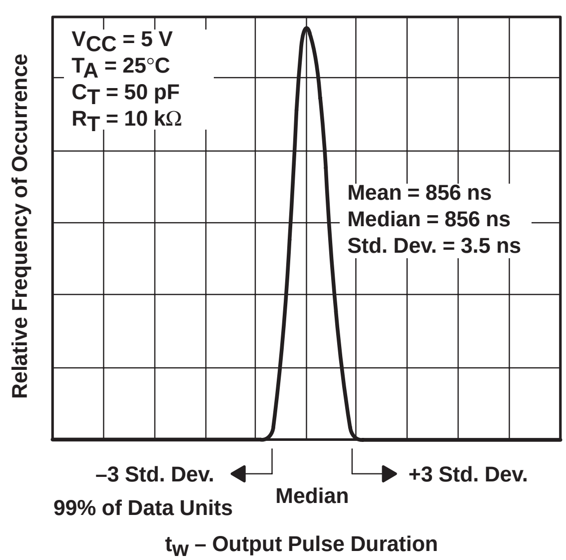


Figure 11

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

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