TC81220F
MPEG2 Video Audio Decoder, Transport Stream Processor RISC 32-bit MIPS System CPU

Overview

TC81220F combines Toshiba's MPEG1/2 audio and MPEG2 video decoder, Transport Stream (TS) processor, and a high performance 32-bit RISC MIPS compatible R3900 CPU into one integrated device. The TS processor handles DVB, DSS, DMC and DVD demultiplexing functions through Toshiba's Application Specific Software (TASS) libraries, downloaded by the R3900 CPU. The R3900 CPU processes software tasks associated with set-top functions including Real-Time Operating System, set-top initialization/test/diagnostics, security/decryption, communication protocols, software modem, IR control, OSD, closed caption and Electronic Program Guide functions. Dedicated MPEG A/V core implementation fully supports MPEG1/2 video (ISO/IEC13818-2) and MPEG1/2 audio (ISO11172-3) standards as well as DVD video standard. Additionally, the MPEG core features Toshiba's exclusive real-time A/V synchronization logic.

TC81220F provides built-in peripheral support for a complete system solution. These include serial, parallel, modem, I^2C interfaces, parallel/serial Smart Card, DMA controller, DRAM controller, serial port, and HP Processor Probe debug port. The on-chip DRAM controllers support 16Mb synchronous DRAM for MPEG2 decoding, and 4Mb or greater Fast Page mode DRAM system memory.

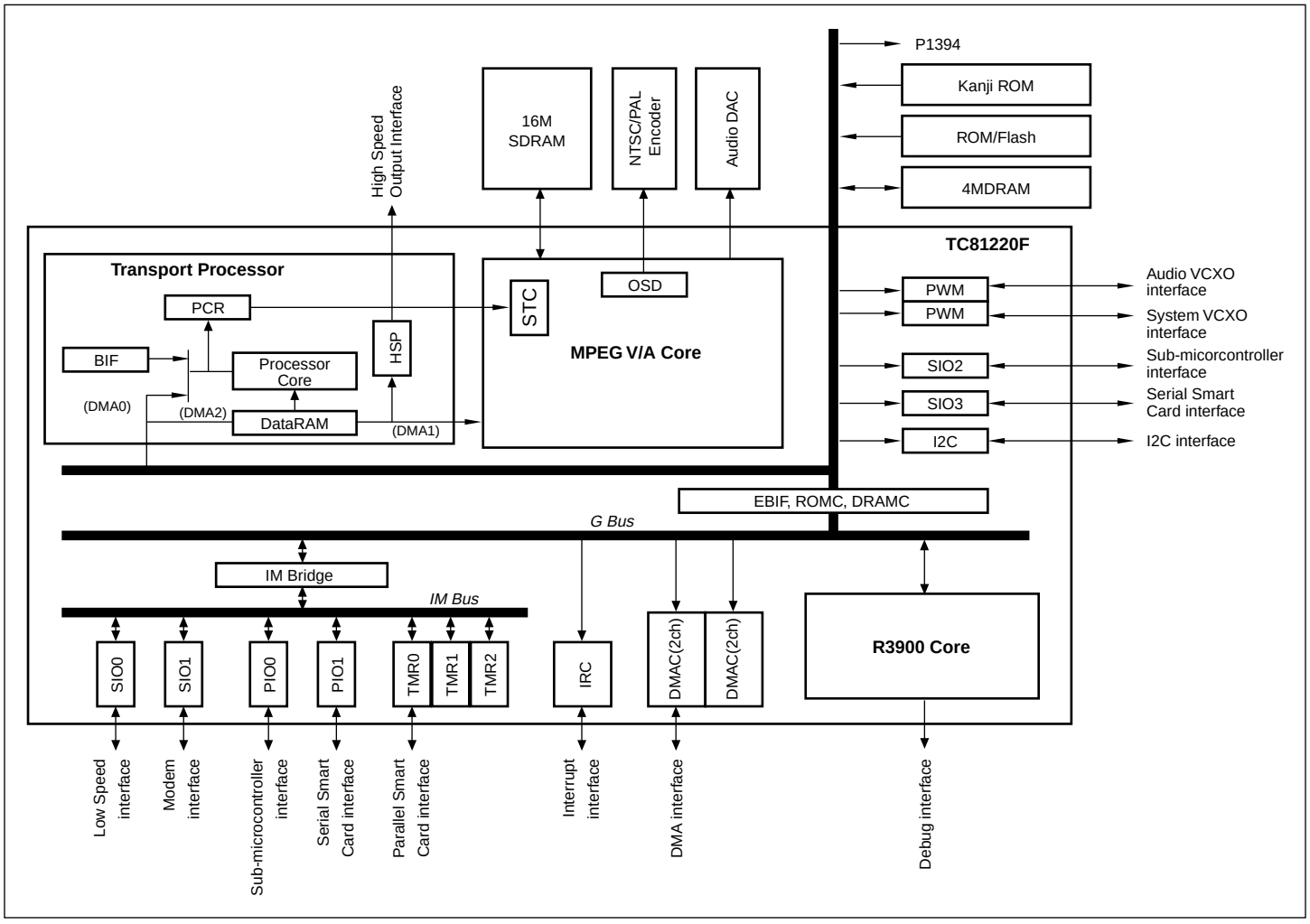


Figure 1. TC81220F Block Diagram

Features

TC81220F integrates MPEG1/2 Main Profile/Main Level video, MPEG1/2 audio decoder with a Transport Stream (TS) processor and high performance MIPS RISC microcontroller. The MPEG decoder features audio and video decoding with automatic Audio/Video synchronization logic, utilizing STC, PTS and DTS time stamps, requiring no intervention from the CPU.

Since MPEG processing is independent from the MIPS CPU, further processing of standard OS, developer system applications and Toshiba Application Specific Software (TASS), i.e. conditional access, modem, DVD, etc. can be performed by the CPU. TASS enables the customer to upgrade target system functions with minimal hardware dependencies.

A 4Mb DRAM is used for system and application programs. ROM/Flash/P1394 interface are supported on the external bus.

The TC81220F can be connected directly with FEC and receive MPEG1/2 bitstreams in the Transport Layer, Program Layer or Packetized Elementary Layer. Elementary Stream is also accepted. The memory interface of the integrated MPEG A/V decoder supports 16Mb external synchronous DRAM, also accessible by RISC CPU. An internal PLL is used for CPU clock generation, 54MHz, from the system 27MHz clock.

Integrated MIPS R3904 Microcontroller

- 32-bit R3900 family, 54MHz, 54.5 Dhrystone MIPS RISC microcontroller, MIPS R3000 architecture
- 25-bit Address/16-bit Data separated external bus
- R3904 microcontroller includes R3900 processor, memory controller, DMA controller, serial ports, timer/counter, interrupt controller and PIO's
- Software Modem VAS
- Single Word, Burst read/write, 5 stage pipelined architecture
- DSP function support: MAC (multiply-accumulate), non-blocking loads, and branch-likely instructions
- Dedicated HP debug port for software/hardware development and debugging
- Bus arbitration and Data Cache snoop functions
- 4KB Instruction Cache, 1KB Data Cache, 2-way associative
- RAM memory configuration of 2 channels
- DRAM Fast Page/Hyper Page (EDO) configuration
- ROM configuration of 2 channels
- Mask ROM, EPROM, E2PROM , Flash, SRAM memory types supported
- DMA independent 4 channel Controller (DMAC)
- 4 Serial I/O, two channel UART
- Prioritized Interrupt Controller (IRC)
- Supports 9 internal interrupts, 8 external interrupts, 1 NMI
- 3 channels 24-bit up-counter, 1 Watchdog timer
- Universal 8-bit parallel I/O, Dedicated smart card I/O
- I2C control bus interface, Smart Card interface, High Speed Interface (HSP)
- CPU Power Management: 4 management modes supported
- Low-power consumption, 3.3V process (1.8–3.3V operating)

Transport Stream (TS) Processor

- Firmware programmable
- Sustained 100 Mbits/sec input rate
- More than 32 PIDs supported
- Dedicated Data/Instruction RAM for external code download (via CPU)
- DVB, DSS, DMC and DVD compliant
- Video clock recovery logic through program PCR management, controlling external VCXO
- Standard Input interface for FEC/Error Correction
- Error Handling capability at the Transport Level
- Conditional Access interface support
- DVB descrambler integrated
- High Speed Output interface (PID matched)

MPEG A/V Decoder Core

Decodable Bitstreams

- System Layer
- MPEG2 Program layer including video and audio
- MPEG2 PES layer including video and audio
- MPEG2 Main Profile or Simple profile
- MPEG2 main level (ITU-R601 resolution)
- Audio MPEG1 Layer 1 and Layer 2, MPEG2 main channels

Video Decoding

- Fully compliant with ISO/IEC13818-2, compatible with PAL/NTSC formats (ITU-R601)
- PAL/NTSC, Selectable 4:2:2 or 4:2:0, NTSC decoding in 3 frame memory and PAL decoding in 2.75 frame memories

Audio Decoding

- Fully compliant with ISO/IEC13818-3 and MPEG2 Audio, supports all common DACs sampling frequencies
- MPEG1 layer 1 and 2, MPEG2, half rate sampling, single/dual/Joint-stereo/stereo decode
- Supports 32KHz, 44.1KHz, 48KHz, 16KHz , 22.05KHz, 24KHz sampling
- Supports five types of DAC: 32fs/48fs/64fs/128fs/256fs

On Screen Display/Graphics (OSD)

- 16 million color palette
- 4, 16, 256 color per window
- 16 levels of blending per pixel

Error Concealment

- Fully compliant with MPEG2 standard
- TC81220F's MPEG A/V decoder core features automatic error concealment without software intervention from CPU

Video Trick/Special Effects Modes

- Entirely handled by MPEG A/V decoder core, by CPU programming internal registers. Audio in all cases is muted gradually
- FAST: Only I and P frames displayed
- SLOW: Reduced speed decoding, which can be selected from 1/2 to 1/32 of normal speed
- FREEZE: Decoding is discontinued, last picture processed is displayed repeatedly. Reading from VBV buffer is halted
- STILL : Last frame is displayed repeatedly. Bitstream is continuously read from VBV buffer but discarded

MPEG Decoder Interrupt Conditions

- Bitstream errors
- Decode time out
- Detect header error
- VBV buffer overflow/underflow

3/2 Pulldown

- Automatic 3/2 pull down by MPEG2 decoder core

Channel Hopping

- During bitstream interruption (i.e. channel hopping), the MPEG decoder automatically displays the last decoded frame

Pan and Scan

- MPEG2 decoder core supports pan and scan using bitstream data

Audio/Video Synchronization and Control of Decode Timing

- MPEG decoder features built-in logic for automatic synchronization of audio and video, achieved without CPU intervention
- STC incremented in sync with SCRCLK. SCR / PCR in the transport / program layer is automatically extracted and set to STC according to MPEG2 system standard
- Video DTS, Audio PTS comparison for presentation start time

Interface

Bitstream Input

- 8-bit parallel input to on-chip Data RAM

Display Interface

- 2 separate video output channels
- Video output channel 1: programmable Video + OSD
- Video output channel 2: programmable between Video + OSD and Video only

Chrominance Output

- 4:2:0 and 4:2:2 are supported. Independent of bitstream sequence.
- For 4:2:2 chrominance signal, on-chip vertical filter is used with required coefficient, instead of simple pixel duplication

Video Synchronization Signals

- Both Master and Slave mode are supported
- Master mode: Generates required VSYNC and HSYNC signals
- Slave mode: Receives VSYNC and HSYNC signals

Video Filters

- Five horizontal filters supported: x2, x3/2, x4/3, x16/9 and x8/3
- Three vertical filters, x2 filter, x3/4 filter and x3/5 filter, are integrated in addition to the chrominance vertical filter to generate 4:2:2 format from 4:2:0 format. X2 filter is assumed to be used for half resolution source picture on the vertical direction.
- Video Letter Boxing function supported for 16:9 and 20:9

Audio Output Interface

- Serial audio data
- Left/Right clock
- Bitclock
- Oversampling clock (Input)

Memory Configuration for MPEG2 Decoder Core

- 16Mb
- Synchronous DRAM interface is integrated on the chip for direct SDRAM connection

Memory Configuration for MIPS Microcontroller

- 4Mb DRAM fast page mode (memory supported up to 16MB)

System Development Environment

The TC81220F supports a growing library of Toshiba Application Specific Software (TASS) for specific design requirements. The TASS libraries are provided by Toshiba and other third party software vendors. The development environment is supported by the following tools:

Software Development Tools

The TC81220F's MIPS RISC R3900 is supported by a host of industry standard software development platforms and Real Time OS/Tools Systems:

Green Hills Software Inc. MULTI software development tool, includes: C & C++ compilers, assembler, linker, librarian and run-time debug module, common API to Real Time OSs, i.e. VwWorks, pSOS, etc.

Integrated Systems Inc. pSOS+ Real Time OS, and a suite of cross development support tools for the R3900 microcontroller.

Wind River Systems Inc. VxWorks-5.2 Real Time OS. Tornado-1.0 Cross-Development Tools suite, which includes: VxWorks run-time OS and a support for communication protocols, complete GNU software development tools including compiler, ICE and ROM emulator modules for the target specific development.

Accelerated Technologies Inc. Nucleus PLUS, Real Time Kernel, TCP/IP protocol stack, UDB Source Debugger, PCMCIA Device Drivers, Ethernet Driver, and GUAPI Graphic User Interface.

Hardware Debug Tools

HP E3492A Embedded MIPS Processor Probe

Toshiba, in cooperation with Hewlett Packard, has developed an on-chip debug monitor logic for the TC81220F. The HP E3492A Embedded MIPS Processor Probe utilizes this logic interface to support a full real-time software debug and development platform. E3492A combines support for standard emulation functions such as interrupts, code trace, hardware/ software breakpoints, address/register access and modification, PC trace, etc., supported even with the cache enabled. The Processor Probe encompasses a complete real-time development and debug environment exclusively designed for the TC81220F R3900 processor.

The primary benefit for using the processor probe vs. in-circuit emulator (ICE) is that the microprocessor is not displaced. Access to the target system is gained via built-in high speed dedicated debug port, affecting no other user signals (serial port, etc). The Processor Probe solution simply renders the traditional ICE inefficient and costly.

– E3492A Software Compiler/Debugger Interface

Green Hills Software's MULTI Environment provides a high-level debug interface API to the HP E3492A processor probe.

HP E3492A Supports Green Hills Software's MULTI C-CROSS MIPS compiler /assembler Version 1.8.7 or higher.

– Host Interface:

Processor probe interfaces to the host through LAN 10BASE-T or 10BASE-2 Ethernet Connections, TCP/IP protocol.

– Supported Hosts

Sun SparcStation , Sun OS 4.1.3 or higher, Solaris 2.3 or higher

HP9000 700, HP-UX9.0 or higher

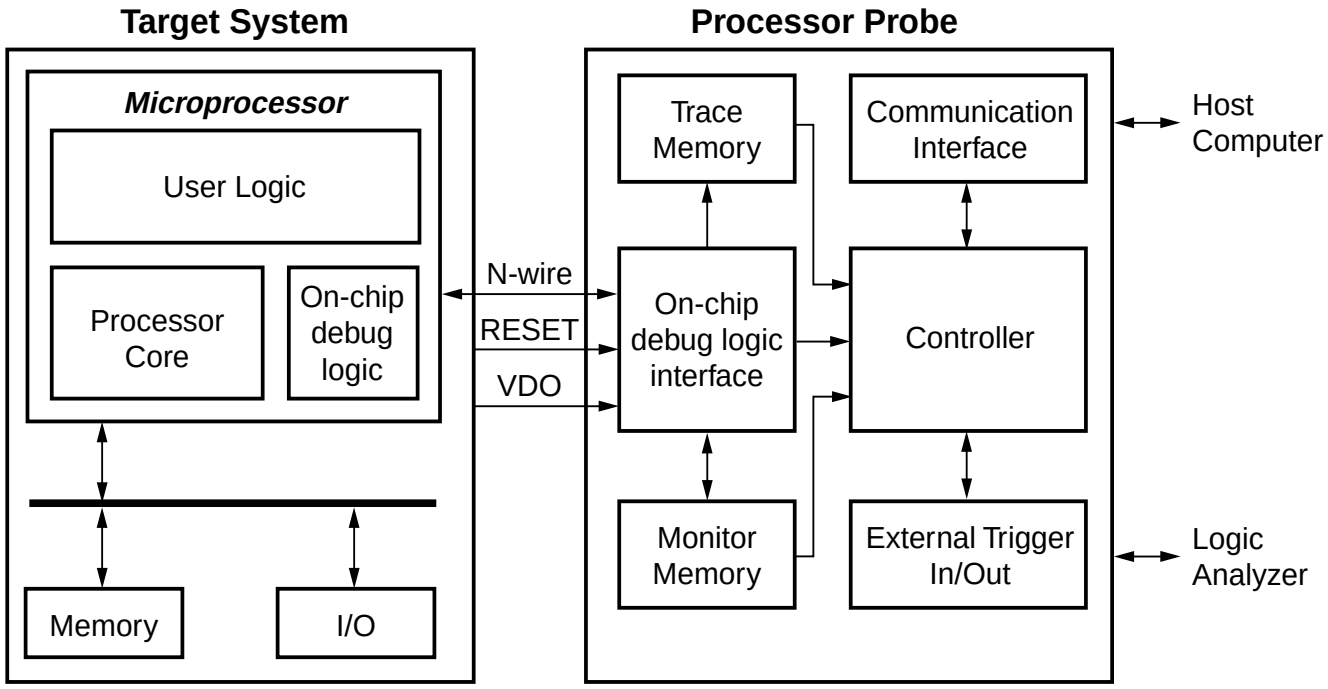
IBM-PC compatibles, MS-Windows 3.1 or Windows95.

TC81220F Development System

Toshiba offers an independent Development Board (DB) for customer evaluation and software development and porting. The TC81220F-DB is a stand-alone system with full run-time and debug capabilities. Peripherals and OS support for Set-Top box, PC MPEG decoders, servers, and target software/ firmware development applications are provided.

Toshiba TC81220F-DB Evaluation System

- TC81220F: MPEG A/V, TS Processor, R3900 microcontroller
- VCXO System 27MHz clock generator
- VCXO – Audio clock generator
- 16Mb SDRAM
- NTSC/PAL/SECAM encoder
- Audio DAC
- HP E3492A 8-bit Debug Port, 20 Pin connector
- 8Mb EPROM
- 4Mb DRAM
- FEC, Smart Card, Modem, Low speed and SubMicron interfaces



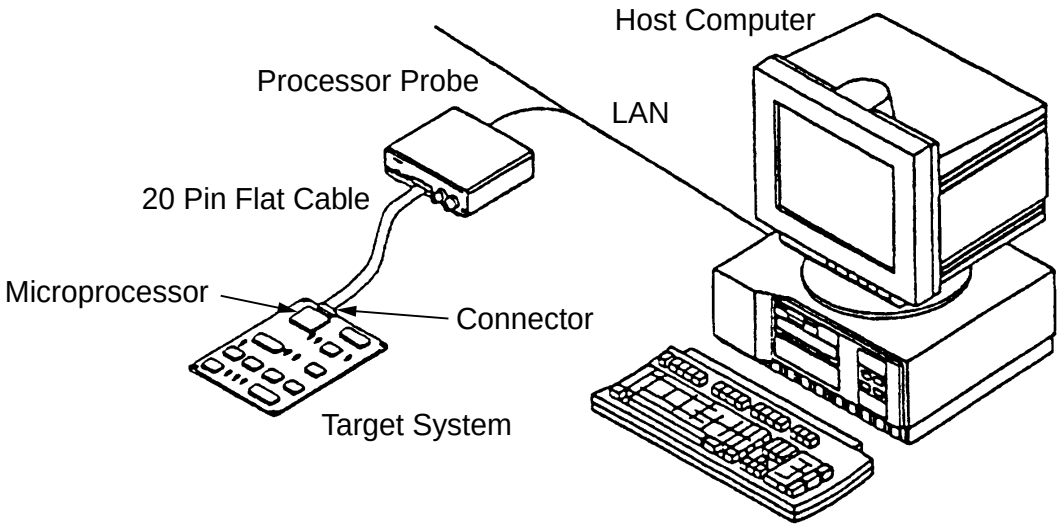


Figure 2. Processor Probe Block Diagram and System Setup

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