

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT4515**

4-to-16 line decoder/demultiplexer  
with input latches; inverting

Product specification  
File under Integrated Circuits, IC06

September 1993

## 4-to-16 line decoder/demultiplexer with input latches; inverting

## 74HC/HCT4515

### FEATURES

- Inverting outputs
- Output capability: standard
- $I_{CC}$  category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT4515 are high-speed Si-gate CMOS devices and are pin compatible with "4515" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4515 are 4-to-16 line decoders/demultiplexers having four binary weighted address inputs ( $A_0$  to  $A_3$ ) with latches, a latch enable input (LE), and an active LOW enable input ( $\overline{E}$ ). The 16 inverting outputs ( $\overline{Q}_0$  to  $\overline{Q}_{15}$ ) are mutually exclusive active LOW. When LE is HIGH, the selected output is determined by the data on  $A_n$ . When LE goes LOW, the last data present at  $A_n$  are stored in the latches and the outputs remain stable. When  $\overline{E}$  is LOW, the selected output, determined by the contents of the latch, is LOW. When  $\overline{E}$  is HIGH, all outputs are HIGH. The enable input ( $\overline{E}$ ) does not affect the state of the latch.

When the "4515" is used as a demultiplexer,  $\overline{E}$  is the data input and  $A_0$  to  $A_3$  are the address inputs.

### QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

| SYMBOL            | PARAMETER                                   | CONDITIONS                                   | TYPICAL |     | UNIT |
|-------------------|---------------------------------------------|----------------------------------------------|---------|-----|------|
|                   |                                             |                                              | HC      | HCT |      |
| $t_{PHL}/t_{PLH}$ | propagation delay $A_n$ to $\overline{Q}_n$ | $C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$ | 25      | 26  | ns   |
| $C_I$             | input capacitance                           |                                              | 3.5     | 3.5 | pF   |
| $C_{PD}$          | power dissipation capacitance per package   | notes 1 and 2                                | 44      | 46  | pF   |

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

### ORDERING INFORMATION

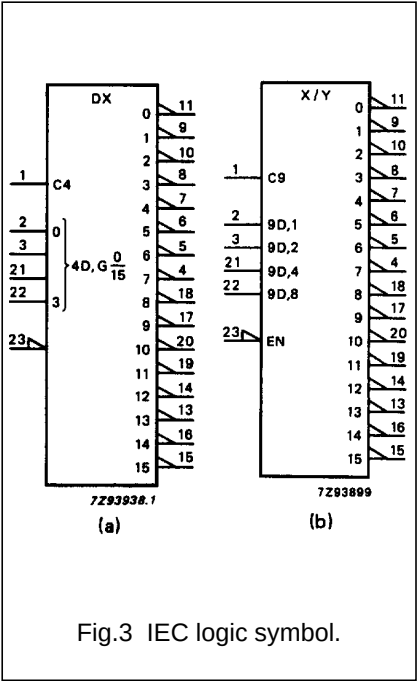
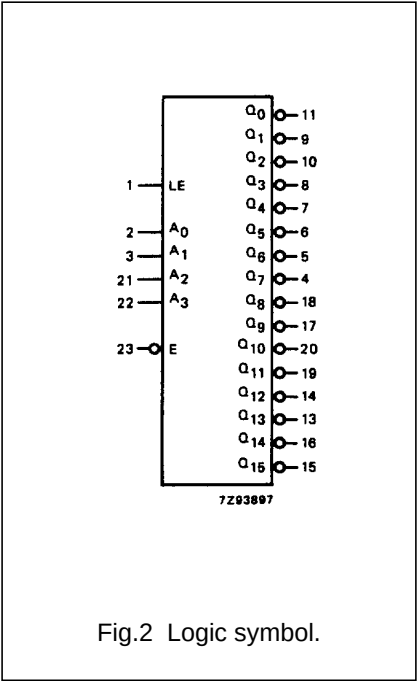
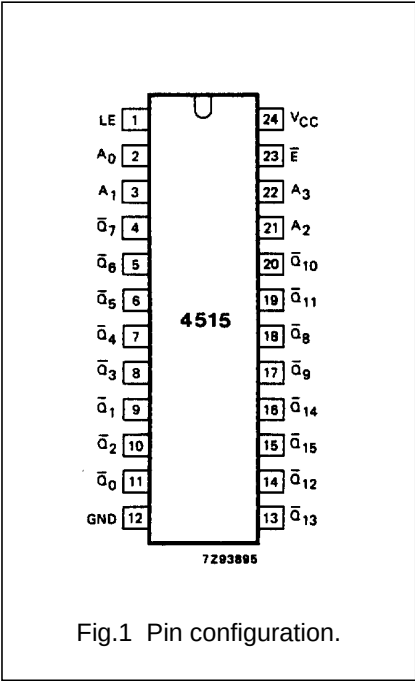
See "74HC/HCT/HCU/HCMOS Logic Package Information".

4-to-16 line decoder/demultiplexer with  
input latches; inverting

74HC/HCT4515

PIN DESCRIPTION

| PIN NO.                                                  | SYMBOL                                  | NAME AND FUNCTION                |
|----------------------------------------------------------|-----------------------------------------|----------------------------------|
| 1                                                        | LE                                      | latch enable input (active HIGH) |
| 2, 3, 21, 22                                             | A <sub>0</sub> to A <sub>3</sub>        | address inputs                   |
| 11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15 | $\overline{Q}_0$ to $\overline{Q}_{15}$ | multiplexer outputs (active LOW) |
| 12                                                       | GND                                     | ground (0 V)                     |
| 23                                                       | $\overline{E}$                          | enable input (active LOW)        |
| 24                                                       | V <sub>CC</sub>                         | positive supply voltage          |



4-to-16 line decoder/demultiplexer with  
input latches; inverting

74HC/HCT4515

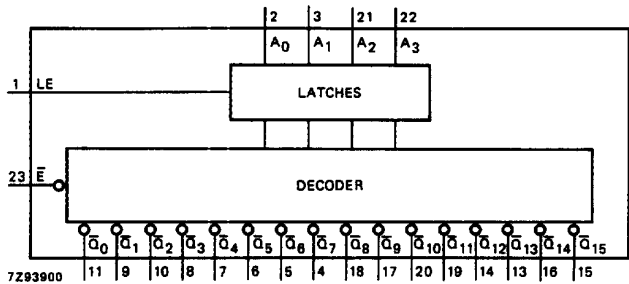


Fig.4 Functional diagram.

APPLICATIONS

- Digital multiplexing
- Address decoding
- Hexadecimal/BCD decoding

FUNCTION TABLE

| INPUTS         |       |       |       |       | OUTPUTS          |                  |                  |                  |                  |                  |                  |                  |                  |                  |                     |                     |                     |                     |                     |                     |
|----------------|-------|-------|-------|-------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| $\overline{E}$ | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $\overline{Q_0}$ | $\overline{Q_1}$ | $\overline{Q_2}$ | $\overline{Q_3}$ | $\overline{Q_4}$ | $\overline{Q_5}$ | $\overline{Q_6}$ | $\overline{Q_7}$ | $\overline{Q_8}$ | $\overline{Q_9}$ | $\overline{Q_{10}}$ | $\overline{Q_{11}}$ | $\overline{Q_{12}}$ | $\overline{Q_{13}}$ | $\overline{Q_{14}}$ | $\overline{Q_{15}}$ |
| H              | X     | X     | X     | X     | H                | H                | H                | H                | H                | H                | H                | H                | H                | H                | H                   | H                   | H                   | H                   | H                   | H                   |
| L              | L     | L     | L     | L     | L                | H                | H                | H                | H                | H                | H                | H                | H                | H                | H                   | H                   | H                   | H                   | H                   | H                   |
| L              | H     | L     | L     | L     | H                | L                | H                | H                | H                | H                | H                | H                | H                | H                | H                   | H                   | H                   | H                   | H                   | H                   |
| L              | L     | H     | L     | L     | H                | H                | L                | H                | H                | H                | H                | H                | H                | H                | H                   | H                   | H                   | H                   | H                   | H                   |
| L              | H     | H     | L     | L     | H                | H                | H                | L                | H                | H                | H                | H                | H                | H                | H                   | H                   | H                   | H                   | H                   | H                   |
| L              | L     | L     | H     | L     | H                | H                | H                | H                | L                | H                | H                | H                | H                | H                | H                   | H                   | H                   | H                   | H                   | H                   |
| L              | H     | L     | H     | L     | H                | H                | H                | H                | H                | L                | H                | H                | H                | H                | H                   | H                   | H                   | H                   | H                   | H                   |
| L              | L     | H     | H     | L     | H                | H                | H                | H                | H                | H                | L                | H                | H                | H                | H                   | H                   | H                   | H                   | H                   | H                   |
| L              | H     | H     | H     | L     | H                | H                | H                | H                | H                | H                | H                | L                | H                | H                | H                   | H                   | H                   | H                   | H                   | H                   |
| L              | L     | L     | L     | H     | H                | H                | H                | H                | H                | H                | H                | H                | L                | H                | H                   | H                   | H                   | H                   | H                   | H                   |
| L              | H     | L     | L     | H     | H                | H                | H                | H                | H                | H                | H                | H                | H                | L                | H                   | H                   | H                   | H                   | H                   | H                   |
| L              | L     | H     | L     | H     | H                | H                | H                | H                | H                | H                | H                | H                | H                | H                | L                   | H                   | H                   | H                   | H                   | H                   |
| L              | H     | H     | L     | H     | H                | H                | H                | H                | H                | H                | H                | H                | H                | H                | H                   | L                   | H                   | H                   | H                   | H                   |
| L              | L     | L     | H     | H     | H                | H                | H                | H                | H                | H                | H                | H                | H                | H                | H                   | H                   | L                   | H                   | H                   | H                   |
| L              | H     | L     | H     | H     | H                | H                | H                | H                | H                | H                | H                | H                | H                | H                | H                   | H                   | H                   | L                   | H                   | H                   |
| L              | L     | H     | H     | H     | H                | H                | H                | H                | H                | H                | H                | H                | H                | H                | H                   | H                   | H                   | H                   | L                   | H                   |
| L              | H     | H     | H     | H     | H                | H                | H                | H                | H                | H                | H                | H                | H                | H                | H                   | H                   | H                   | H                   | H                   | L                   |

Notes

1. LE = HIGH  
H = HIGH voltage level  
L = LOW voltage level  
X = don't care

4-to-16 line decoder/demultiplexer with  
input latches; inverting

74HC/HCT4515

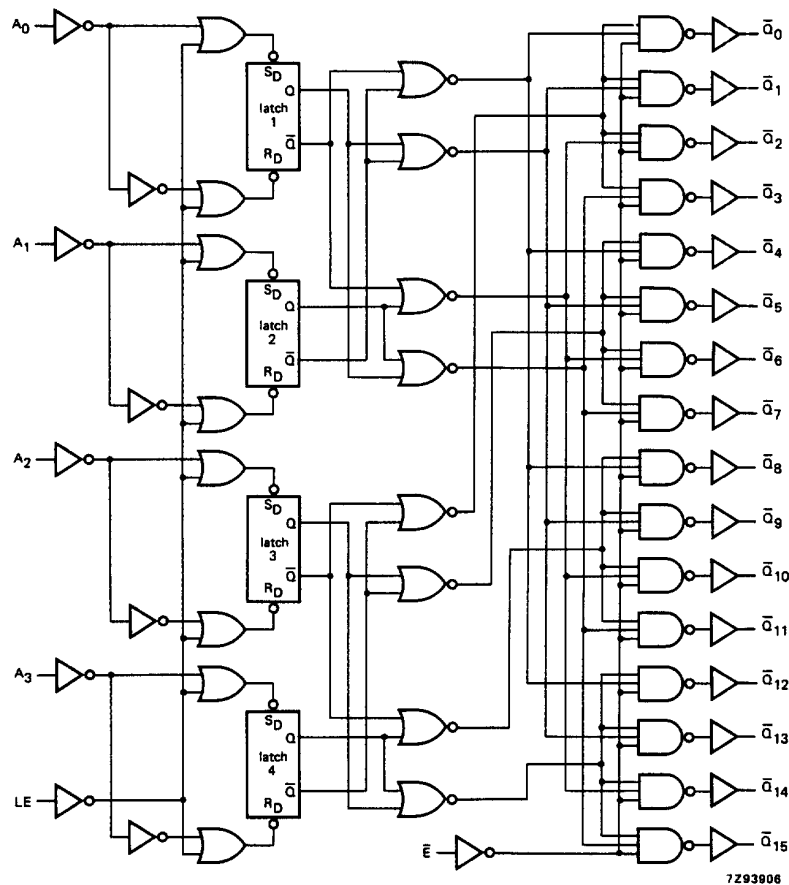


Fig.5 Logic diagram.

# 4-to-16 line decoder/demultiplexer with input latches; inverting

74HC/HCT4515

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER                                               | T <sub>amb</sub> (°C) |                 |                 |                 |                 |                 |                 | UNIT | TEST CONDITIONS        |           |
|-------------------------------------|---------------------------------------------------------|-----------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------|------------------------|-----------|
|                                     |                                                         | 74HC                  |                 |                 |                 |                 |                 |                 |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                                     |                                                         | +25                   |                 |                 | −40 to +85      |                 | −40 to +125     |                 |      |                        |           |
|                                     |                                                         | min.                  | typ.            | max.            | min.            | max.            | min.            | max.            |      |                        |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>A <sub>n</sub> to $\overline{Q}_n$ |                       | 80<br>29<br>23  | 250<br>50<br>43 |                 | 315<br>63<br>54 |                 | 375<br>75<br>64 | ns   | 2.0<br>4.5<br>6.0      | Fig.6     |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>LE to $\overline{Q}_n$             |                       | 66<br>24<br>19  | 225<br>45<br>38 |                 | 280<br>56<br>48 |                 | 340<br>68<br>58 | ns   | 2.0<br>4.5<br>6.0      | Fig.6     |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>$\overline{E}$ to $\overline{Q}_n$ |                       | 50<br>18<br>14  | 175<br>35<br>30 |                 | 220<br>44<br>37 |                 | 265<br>53<br>45 | ns   | 2.0<br>4.5<br>6.0      | Fig.6     |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                                  |                       | 19<br>7<br>6    | 75<br>15<br>13  |                 | 95<br>19<br>16  |                 | 110<br>22<br>19 | ns   | 2.0<br>4.5<br>6.0      | Fig.6     |
| t <sub>W</sub>                      | latch enable pulse width<br>HIGH                        | 75<br>15<br>13        | 14<br>5<br>4    |                 | 95<br>19<br>16  |                 | 110<br>22<br>19 |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |
| t <sub>su</sub>                     | set-up time<br>A <sub>n</sub> to LE                     | 90<br>18<br>15        | 28<br>10<br>8   |                 | 115<br>23<br>20 |                 | 135<br>27<br>23 |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |
| t <sub>h</sub>                      | hold time<br>A <sub>n</sub> to LE                       | 0<br>0<br>0           | −11<br>−4<br>−3 |                 | 0<br>0<br>0     |                 | 0<br>0<br>0     |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |

# 4-to-16 line decoder/demultiplexer with input latches; inverting

74HC/HCT4515

## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

### Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT          | UNIT LOAD COEFFICIENT |
|----------------|-----------------------|
| A <sub>n</sub> | 0.65                  |
| LE             | 1.40                  |
| $\overline{E}$ | 1.00                  |

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER                                               | T <sub>amb</sub> (°C) |      |      |           |      |             |      | UNIT | TEST CONDITIONS        |           |
|-------------------------------------|---------------------------------------------------------|-----------------------|------|------|-----------|------|-------------|------|------|------------------------|-----------|
|                                     |                                                         | 74HCT                 |      |      |           |      |             |      |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                                     |                                                         | +25                   |      |      | −40 to+85 |      | −40 to +125 |      |      |                        |           |
|                                     |                                                         | min.                  | typ. | max. | min.      | max. | min.        | max. |      |                        |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>A <sub>n</sub> to $\overline{Q}_n$ |                       | 30   | 55   |           | 69   |             | 83   | ns   | 4.5                    | Fig.6     |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>LE to $\overline{Q}_n$             |                       | 29   | 50   |           | 63   |             | 75   | ns   | 4.5                    | Fig.6     |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>$\overline{E}$ to $\overline{Q}_n$ |                       | 18   | 40   |           | 50   |             | 60   | ns   | 4.5                    | Fig.6     |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                                  |                       | 7    | 15   |           | 19   |             | 22   | ns   | 4.5                    | Fig.6     |
| t <sub>W</sub>                      | latch enable pulse width<br>HIGH                        | 16                    | 3    |      | 20        |      | 24          |      | ns   | 4.5                    | Fig.7     |
| t <sub>su</sub>                     | set-up time<br>A <sub>n</sub> to LE                     | 18                    | 9    |      | 23        |      | 27          |      | ns   | 4.5                    | Fig.7     |
| t <sub>h</sub>                      | hold time<br>A <sub>n</sub> to LE                       | 3                     | −2   |      | 3         |      | 3           |      | ns   | 4.5                    | Fig.7     |

# 4-to-16 line decoder/demultiplexer with input latches; inverting

74HC/HCT4515

## AC WAVEFORMS

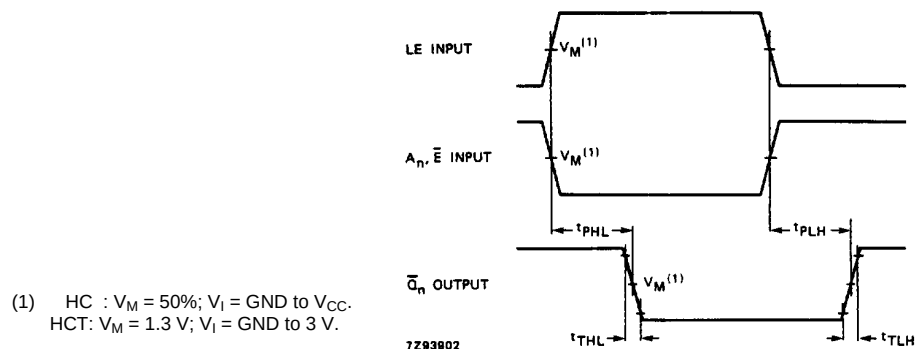


Fig.6 Waveforms showing the input ( $A_n$ , LE,  $\bar{E}$ ) to output ( $\bar{Q}_n$ ) propagation delays and the output transition times.

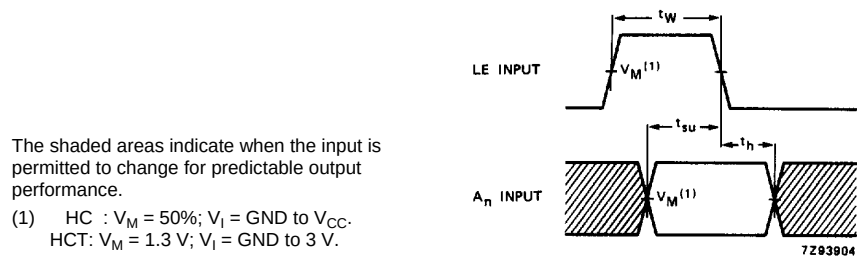


Fig.7 Waveforms showing the minimum pulse width of the latch enable input (LE) and the set-up and hold times for LE to  $A_n$ . Set-up and hold times are shown as positive values but may be specified as negative values.

## PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".



# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[NXP:](#)

[74HC4515D-T](#) [74HC4515N](#) [74HCT4515D](#) [74HCT4515D-T](#) [74HCT4515N](#) [74HC4515D,652](#) [74HC4515D,653](#)  
[74HC4515N,652](#) [74HCT4515D,652](#) [74HCT4515D,653](#) [74HCT4515N,652](#)