Data Sheet | April 12, 2007 | FN2920.10

2MHz, Super Chopper-Stabilized Operational Amplifier

The ICL7650S Super Chopper-Stabilized Amplifier offers exceptionally low input offset voltage and is extremely stable with respect to time and temperature. It is a direct replacement for the industry-standard ICL7650 offering ***improved*** input offset voltage, ***lower*** input offset voltage temperature coefficient, ***reduced*** input bias current, and ***wider*** common mode voltage range. All improvements are highlighted in ***bold italics*** in the Electrical Characteristics section. ***Critical parameters are guaranteed over the entire commercial temperature range.***

Intersil's unique CMOS chopper-stabilized amplifier circuitry is user-transparent, virtually eliminating the traditional chopper amplifier problems of intermodulation effects, chopping spikes, and overrange lockup.

The chopper amplifier achieves its low offset by comparing the inverting and non-inverting input voltages in a nulling amplifier, nulled by alternate clock phases. Two external capacitors are required to store the correcting potentials on the two amplifier nulling inputs; these are the only external components necessary.

The clock oscillator and all the other control circuitry is entirely self-contained. However the 14 lead version includes a provision for the use of an external clock, if required for a particular application. In addition, the ICL7650S is internally compensated for unity-gain operation.

Features

- *Guaranteed* Max Input Offset Voltage for *All* Temperature Ranges
- Low Long-Term and Temperature Drifts of Input Offset Voltage
- *Guaranteed* Max Input Bias Current 10pA
- *Extremely Wide* Common Mode Voltage Range. . . . . +3.5V to -5V
- *Reduced* Supply Current 2mA
- *Guaranteed* Minimum Output Source/Sink Current
- Extremely High Gain 150dB
- Extremely High CMRR and PSRR 140dB
- High Slew Rate 2.5V/µs
- Wide Bandwidth 2MHz
- Unity-Gain Compensated
- Clamp Circuit to Avoid Overload Recovery Problems and Allow Comparator Use
- Extremely Low Chopping Spikes at Input and Output
- *Improved, Direct* Replacement for Industry-Standard ICL7650 and other Second-Source Parts
- Pb-Free Plus Anneal Available (RoHS Compliant)

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ICL7650SCBA-1	7650S CBA-1	0 to +70	8 Ld SOIC	M8.15
ICL7650SCBA-1T	7650S CBA-1	0 to +70	8 Ld SOIC (Tape and Reel)	M8.15
ICL7650SCBA-1Z (Note)	7650S CBA-1Z	0 to +70	8 Ld SOIC	M8.15
ICL7650SCBA-1ZT (Note)	7650S CBA-1Z	0 to +70	8 Ld SOIC (Tape and Reel)	M8.15
ICL7650SCPA-1	7650S CPA-1	0 to +70	8 Ld PDIP	E8.3
ICL7650SCPA-1Z (Note)	7650S CPA-1Z	0 to +70	8 Ld PDIP* (Pb-free)	E8.3
ICL7650SCPD	ICL7650SCPD	0 to +70	14 Ld PDIP	E14.3
ICL7650SCPDZ	7650SCPDZ	0 to +70	14 Ld PDIP* (Pb-free)	E14.3

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications. NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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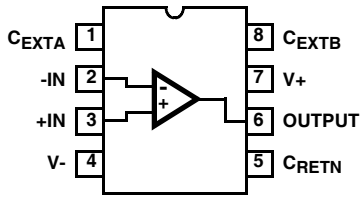
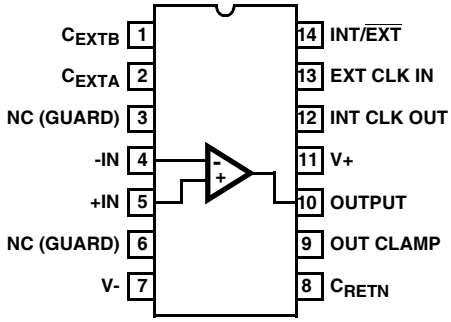
Pinouts

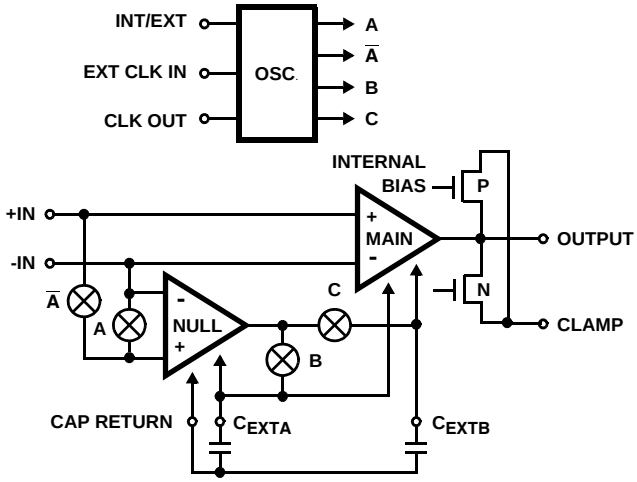
ICL7650S
(8 LD PDIP, SOIC)
TOP VIEW

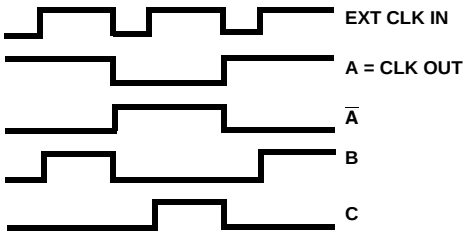


ICL7650S
(14 PDIP)
TOP VIEW



Functional Diagram





Absolute Maximum Ratings

Supply Voltage (V+ to V-). 18V
Input Voltage . . . . . (V+ +0.3) to (V- -0.3)
Voltage on Oscillator Control Pins . . . . . V+ to V-
Duration of Output Short Circuit. . . . . Indefinite
Current to Any Pin 10mA
While Operating (Note 1) 100µA

Operating Conditions

Temperature Range
ICL7650SC. . . . . 0°C to +70°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Lead PDIP Package*	110	N/A
14 Lead PDIP Package	90	N/A
8 Lead SOIC Package	160	N/A

Maximum Junction Temperature (Plastic Package) . . . . . .+150°C
Maximum Storage Temperature Range. . . . . -55°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp
*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Limiting input current to 100µA is recommended to avoid latchup problems. Typically 1mA is safe, however this is not guaranteed.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications V_{SUPPLY} = ±5V. See Test Circuit, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 3)	***V_{OS}***		+25	-	***±0.7***	***±5***	µV
			0 to +70	-	***±1***	***±8***	µV
Average Temperature Coefficient of Input Offset Voltage (Note 3)	***$\Delta V_{OS}/\Delta T$***		0 to +70	-	***0.02***	-	µV/°C
Change in Input Offset with Time	$\Delta V_{OS}/\Delta T$		+25	-	100	-	$nV/\sqrt{month}$
Input Bias Current |I(+)|, |I(-)|	***I_{BIAS}***		+25	-	4	10	pA
			0 to +70	-	***5***	***20***	pA
Input Offset Current |I(-), |I(+)|	***I_{OS}***		+25	-	***8***	***20***	pA
			0 to +70	-	***10***	***40***	pA
Input Resistance	R_{IN}		+25	-	10^{12}	-	Ω
Large Signal Voltage Gain (Note 3)	***A_{VOL}***	R_L = 10kΩ, V_O = ±4V	+25	***135***	***150***	-	dB
			0 to +70	***130***	-	-	dB
Output Voltage Swing (Note 4)	V_{OUT}	R_L = 10kΩ	+25	±4.7	±4.85	-	V
		R_L = 100kΩ	+25	-	±4.95	-	V
Common Mode Voltage Range (Note 3)	***CMVR***		+25	-5	***-5.2 to +4***	***3.5***	V
			0 to +70	-5	-	***3.5***	V
Common Mode Rejection Ratio (Note 3)	***CMRR***	CMVR = -5V to +3.5V	+25	***120***	***140***	-	dB
			0 to +70	***120***	-	-	dB
Power Supply Rejection Ratio	***PSRR***	V_S = ±3V to ±8V	+25	120	***140***	-	dB
Input Noise Voltage	e_N	R_S = 100Ω, f = DC to 10Hz	+25	-	2	-	μV_{P-P}
Input Noise Current	i_N	f = 10Hz	+25	-	0.01	-	$pA/\sqrt{Hz}$
Gain Bandwidth Product	GBWP		+25	-	2	-	MHz
Slew Rate	SR	C_L = 50pF, R_L = 10kΩ	+25	-	2.5	-	V/µs
Rise Time	t_R		+25	-	0.2	-	µs
Overshoot	OS		+25	-	20	-	%
Operating Supply Range	V+ to V-		+25	4.5	-	16	V
Supply Current	***I_{SUPP}***	No Load	+25	-	2	***3***	mA
			0 to +70	-	-	***3.2***	mA

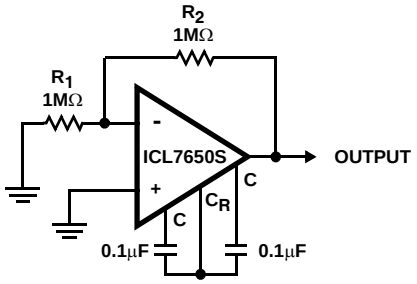
Electrical Specifications V_{SUPPLY} = ±5V. See Test Circuit, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
Output Source Current	$I_{O\ SOURCE}$		+25	2.9	4.5	-	mA
			0 to +70	2.3	-	-	mA
Output Sink Current	$I_{O\ SINK}$		+25	25	30	-	mA
			0 to +70	20	-	-	mA
Internal Chopping Frequency	f_{CH}	Pins 13 and 14 Open	+25	120	250	375	Hz
Clamp ON Current (Note 5)		R_L = 100kΩ	+25	25	70	-	µA
Clamp OFF Current (Note 5)		-4V ≤ V_{OUT} ≤ +4V	+25	-	***0.001***	***5***	nA
			0 to +70	-	-	***10***	nA

NOTES:

3. These parameters are guaranteed by design and characterization, but not tested at temperature extremes because thermocouple effects prevent precise measurement of these voltages in automatic test equipment.
4. OUTPUT CLAMP not connected. See typical characteristic curves for output swing vs clamp current characteristics.
5. See OUTPUT CLAMP under detailed description.
6. All significant improvements over the industry-standard ICL7650 are highlighted in ***bold italics.***

Test Circuit



Application Information

Detailed Description

AMPLIFIER

The functional diagram shows the major elements of the ICL7650S. There are two amplifiers, the main amplifier, and the nulling amplifier. Both have offset-null capability. The main amplifier is connected continuously from the input to the output, while the nulling amplifier, under the control of the chopping oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling connections, which are MOSFET gates, are inherently high impedance, and two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power-supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A_{VOL}.

Careful balancing of the input switches, and the inherent balance of the input circuit, minimizes chopper frequency charge injection at the input terminals, and also the feed forward-type injection into the compensation capacitor, which is the main cause of output spikes in this type of circuit.

INTERMODULATION

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite AC gain of the amplifier necessitates a small AC signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs frequency characteristics near the chopping frequency. These effects are substantially reduced in the ICL7650S by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to finite AC gain. Since that is the major error contribution to the ICL7650S, the intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

CAPACITOR CONNECTION

The null/storage capacitors should be connected to the CEXTA and CEXTB pins, with a common connection to the CRETN pin. This connection should be made directly by either a separate wire or PC trace to avoid injecting load current IR drops into the capacitive circuitry. The outside foil, where available, should be connected to CRETN.

OUTPUT CLAMP

The OUTPUT CLAMP pin allows reduction of the overload recovery time inherent with chopper-stabilized amplifiers. When tied to the inverting input pin, or summing junction, a current path between this point and the OUTPUT pin occurs just before the device output saturates. Thus uncontrolled input differentials are avoided, together with the consequent charge buildup on the correction-storage capacitors. The output swing is slightly reduced.

CLOCK

The ICL7650S has an internal oscillator, giving a chopping frequency of 200Hz, available at the CLOCK OUT pin on the 14 pin devices. Provision has also been made for the use of an external clock in these parts. The INT/$\overline{\text{EXT}}$ pin has an internal pull-up and may be left open for normal operation, but to utilize an external clock this pin must be tied to V- to disable the internal clock. The external clock signal may then be applied to the EXT CLOCK IN pin. An internal divide-by-two provides the desired 50% input switching duty cycle. Since the capacitors are charged only when EXT CLOCK IN is high, a 50% to 80% positive duty cycle is recommended, especially for higher frequencies. The external clock can swing between V+ and V-. The logic threshold will be at about 2.5V below V+. Note also that a signal of about 400 Hz, with a 70% duty cycle, will be present at the EXT CLOCK IN pin with INT/$\overline{\text{EXT}}$ high or open. This is the internal clock signal before being fed to the divider.

In those applications where a strobe signal is available, an alternate approach to avoid capacitor misbalancing during overload can be used. If a strobe signal is connected to EXT CLK IN so that it is low during the time that the overload signal is applied to the amplifier, neither capacitor will be charged. Since the leakage at the capacitor pins is quite low at room temperature, the typical amplifier will drift less than 10μV/s, and relatively long measurements can be made with little change in offset.

COMPONENT SELECTION

The two required capacitors, C_{EXTA} and C_{EXTB}, have optimum values depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1μF, and to maintain the same relationship between the chopping frequency and the nulling time constant this value should be scaled approximately in proportion if an external clock is used. A high quality film type capacitor such as mylar is preferred, although a ceramic or other lower-grade capacitor may prove suitable in many applications. For quickest settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1μV.

STATIC PROTECTION

All device pins are static-protected by the use of input diodes. However, strong static fields and discharges should be avoided, as they can cause degraded diode junction characteristics, which may result in increased input-leakage currents.

LATCHUP AVOIDANCE

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (PNPN) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 1mA to avoid latchup, even under fault conditions.

OUTPUT STAGE/LOAD DRIVING

The output circuit is a high-impedance type (approximately 18kΩ), and therefore with loads less than this value, the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17dB lower with a 1kΩ load than with a 10kΩ load. If the amplifier is used strictly for DC, this lower gain is of little consequence, since the DC gain is typically greater than 120dB even with a 1kΩ load. However, for wideband applications, the best frequency response will be achieved with a load resistor of 10kΩ or higher. This will result in a smooth 6dB/octave response from 0.1Hz to 2MHz, with phase shifts of less than 10° in the transition region where the main amplifier takes over from the null amplifier.

THERMO-ELECTRIC EFFECTS

The ultimate limitations to ultra-high precision DC amplifiers are the thermo-electric or Peltier effects arising in thermocouple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermoelectric voltages typically around 0.1μV/°C, but up to tens of mV/°C for some materials, will be generated. In order to realize the extremely low offset voltages that the chopper amplifier can provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially that caused by power-dissipating elements in the system. Low thermoelectric-efficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and good separation from surrounding heat-dissipating elements is advisable.

GUARDING

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the ICL7650S. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

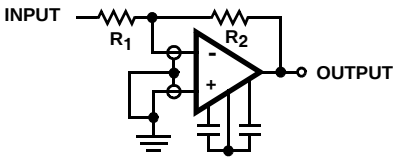


FIGURE 1A. INVERTING AMPLIFIER

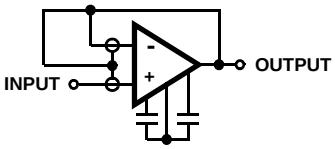
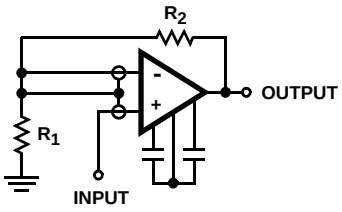


FIGURE 1B. FOLLOWER



NOTE: $\frac{R_1 R_2}{R_1 + R_2}$ SHOULD BE LOW IMPEDANCE FOR OPTIMUM GUARDING

FIGURE 1C. NON-INVERTING AMPLIFIER

FIGURE 1. CONNECTION OF INPUT GUARDS

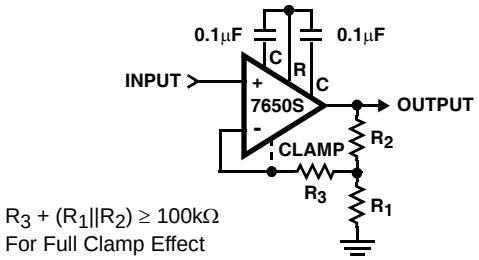
PIN COMPATIBILITY

The basic pinout of the 8-pin device corresponds, where possible, to that of the industry standard 8-pin devices, the LM741, LM101, etc. The null-storing external capacitors are connected to pins 1 and 8, usually used for offset null or compensation capacitors, or simply not connected. In the case of the OP-05 and OP-07 devices, the replacement of the offset-null pot, connected between pins 1 and 8 and V+, by two capacitors from those pins to pin 5, will provide easy compatibility. As for the LM108, replacement of the compensation capacitor between pins 1 and 8 by the two capacitors to pin 5 is all that is necessary. The same operation, with the removal of any connection to pin 5, will suffice for the LM101, μA748, and similar parts.

The 14-pin device pinout corresponds most closely to that of the LM108 device, owing to the provision of “NC” pins for guarding between the input and all other pins. Since this device does not use any of the extra pins, and has no provision for offset-nulling, but requires a compensation capacitor, some changes will be required in layout to convert it to the ICL7650S.

Typical Applications

Clearly the applications of the ICL7650S will mirror those of other op amps. Anywhere that the performance of a circuit can be significantly improved by a reduction of input-offset voltage and bias current, the ICL7650S is the logical choice. Basic non-inverting and inverting amplifier circuits are shown in Figures 2 and 3. Both circuits can use the output clamping circuit to enhance the overload recovery performance. The only limitations on the replacement of other op amps by the ICL7650S are the supply voltage (±8V Max) and the output drive capability (10kΩ load for full swing). Even these limitations can be overcome using a simple booster circuit, as shown in Figure 4, to enable the full output capabilities of the LM741 (or any other standard device) to be combined with the input capabilities of the ICL7650S. The pair form a composite device, so loop gain stability, when the feedback network is added, should be watched carefully.



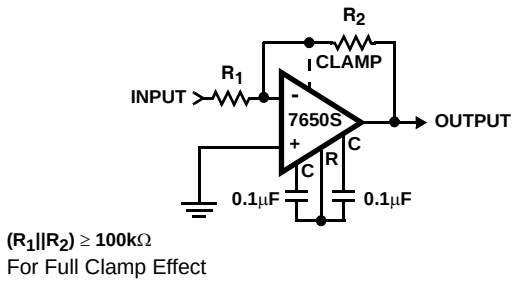
$R_3 + (R_1||R_2) \geq 100k\Omega$
For Full Clamp Effect

NOTE: $R_1||R_2$ indicates the parallel combination of R_1 and R_2.

FIGURE 2. NON INVERTING AMPLIFIER WITH OPTIONAL CLAMP

Figure 5 shows the use of the clamp circuit to advantage in a zero-offset comparator. The usual problems in using a chopper stabilized amplifier in this application are avoided, since the clamp circuit forces the inverting input to follow the input signal. The threshold input must tolerate the output clamp current $\approx V_{IN}/R$ without disturbing other portions of the system.

The pin configuration of the 14 pin dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration, but corresponds to that of the LM108).



NOTE: $R_1||R_2$ indicates the parallel combination of R_1 and R_2.

FIGURE 3. INVERTING AMPLIFIER WITH (OPTIONAL) CLAMP

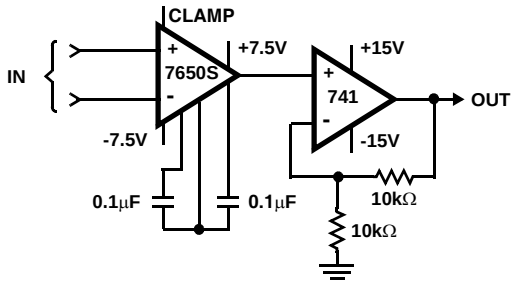


FIGURE 4. USING 741 TO BOOST OUTPUT DRIVE CAPACITY

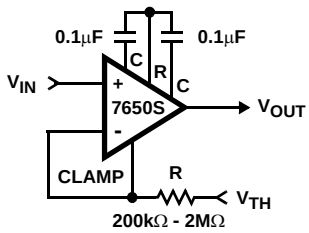
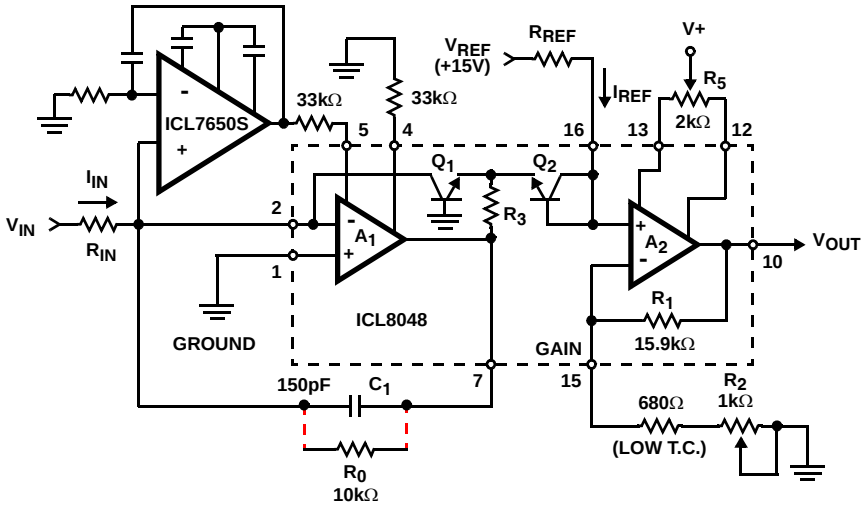


FIGURE 5. LOW OFFSET COMPARATOR



NOTE: For further Applications Assistance, see AN053.

FIGURE 6. ICL8048 OFFSET NULLED BY ICL7650S

Normal logarithmic amplifiers are limited in dynamic range in the voltage-input mode by their input-offset voltage. The built-in temperature compensation and convenience features of the ICL8048 can be extended to a voltage-input dynamic range of close to 6 decades by using the ICL7650S to offset-null the ICL8048, as shown in Figure 6. The same concept can also be used with such devices as the HA2500 or HA2600 families of op amps to add very low offset voltage capability to their very high slew rates and bandwidths. Note that these circuits will also have their DC gains, CMRR, and PSRR enhanced.

Typical Performance Curves

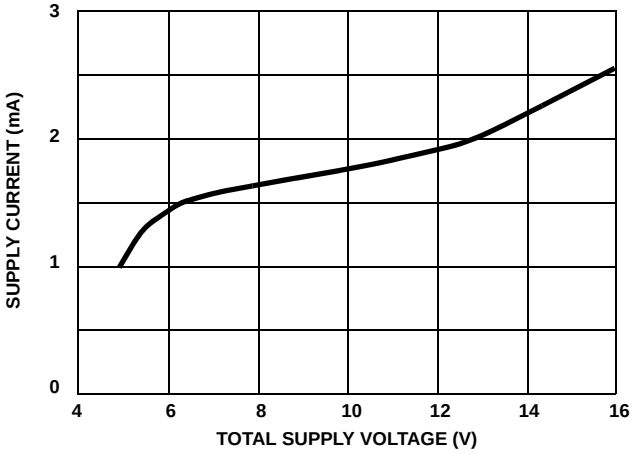


FIGURE 7. SUPPLY CURRENT vs SUPPLY VOLTAGE

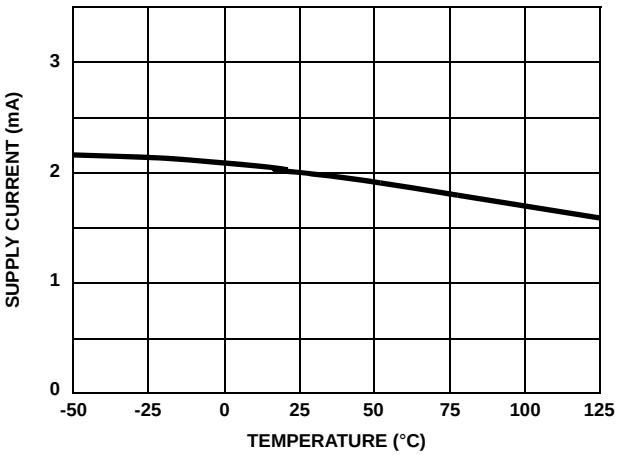


FIGURE 8. SUPPLY CURRENT vs AMBIENT TEMPERATURE

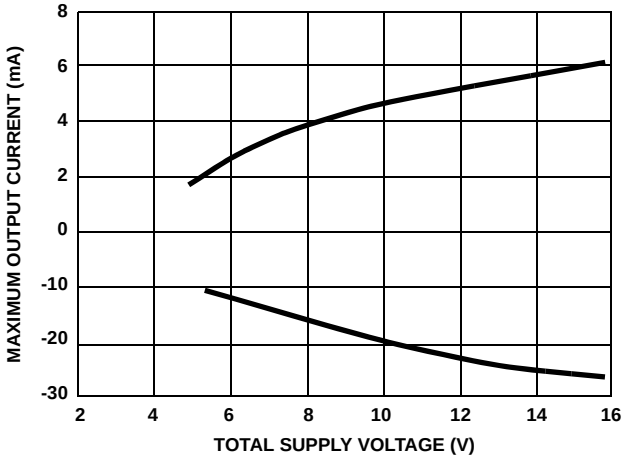


FIGURE 9. MAXIMUM OUTPUT CURRENT vs SUPPLY VOLTAGE

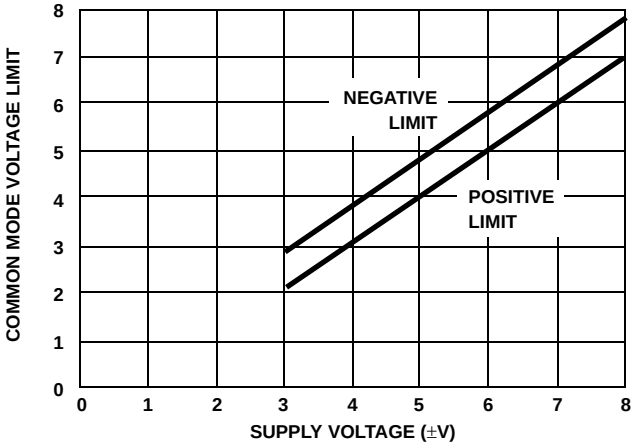


FIGURE 10. COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

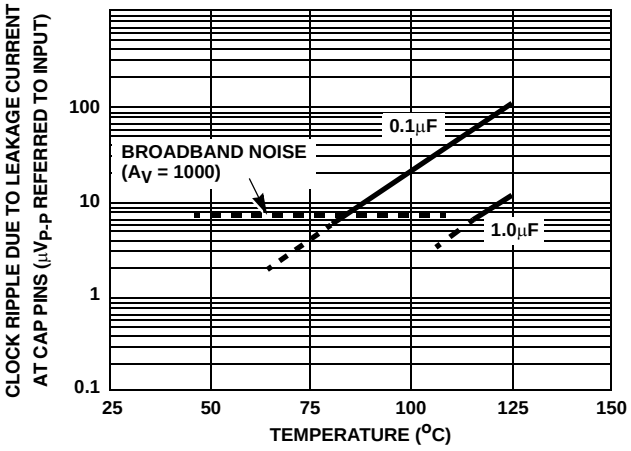


FIGURE 11. CLOCK RIPPLE REFERRED TO THE INPUT vs TEMPERATURE

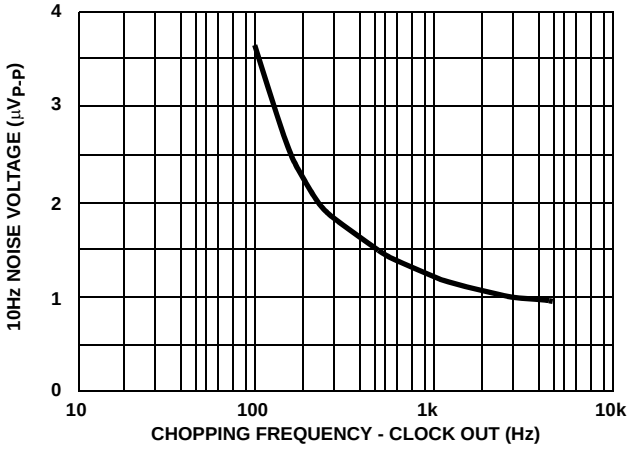


FIGURE 12. 10Hz NOISE VOLTAGE vs CHOPPING FREQUENCY

Typical Performance Curves (Continued)

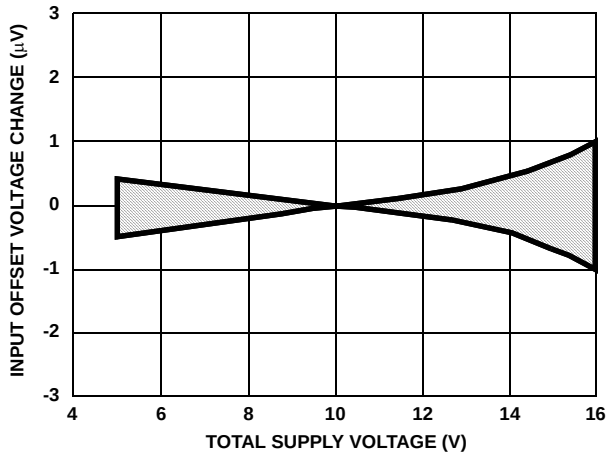


FIGURE 13. INPUT OFFSET VOLTAGE CHANGE vs SUPPLY VOLTAGE

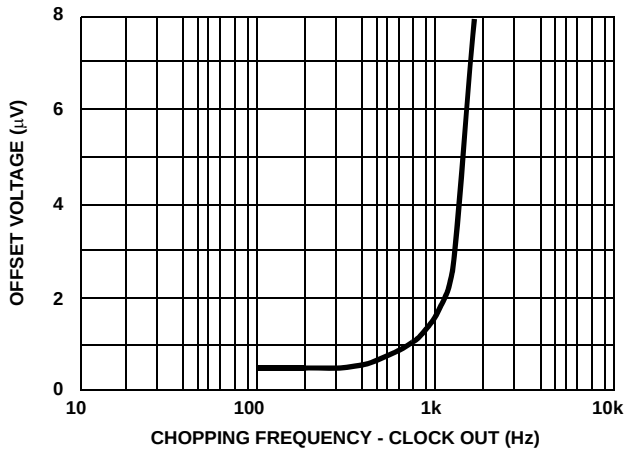


FIGURE 14. INPUT OFFSET VOLTAGE vs CHOPPING FREQUENCY

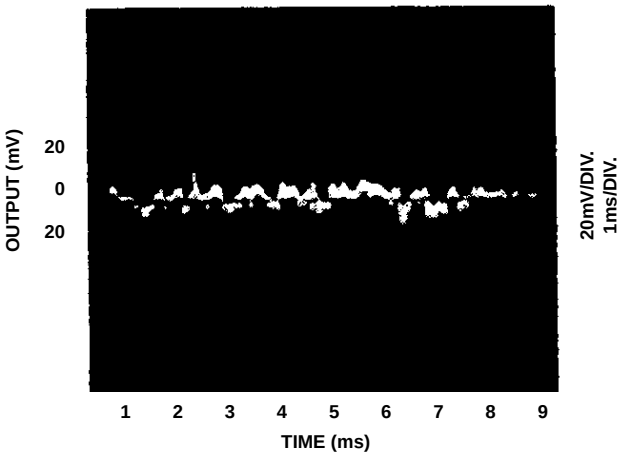


FIGURE 15. OUTPUT WITH ZERO INPUT; GAIN = 1000; BALANCED SOURCE IMPEDANCE = 10kΩ

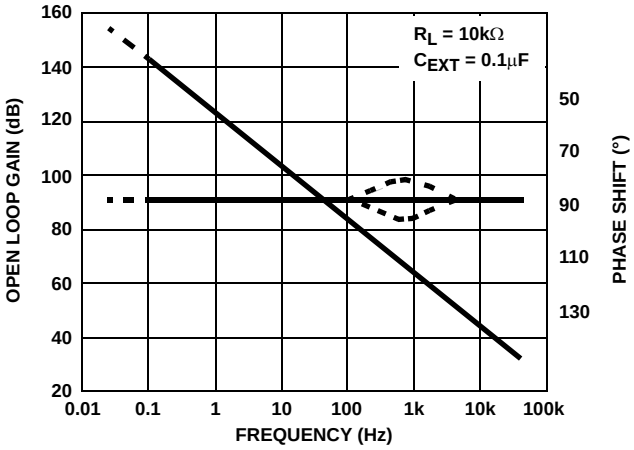


FIGURE 16. OPEN LOOP GAIN AND PHASE SHIFT vs FREQUENCY

Typical Performance Curves (Continued)

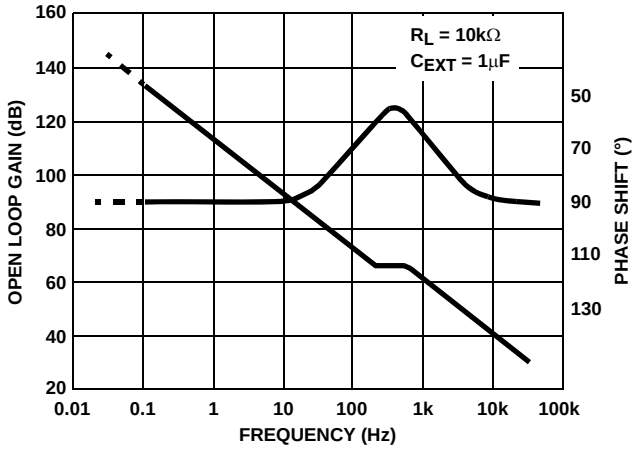
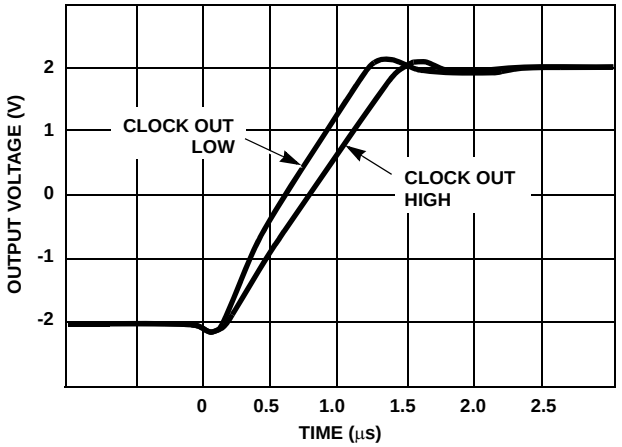
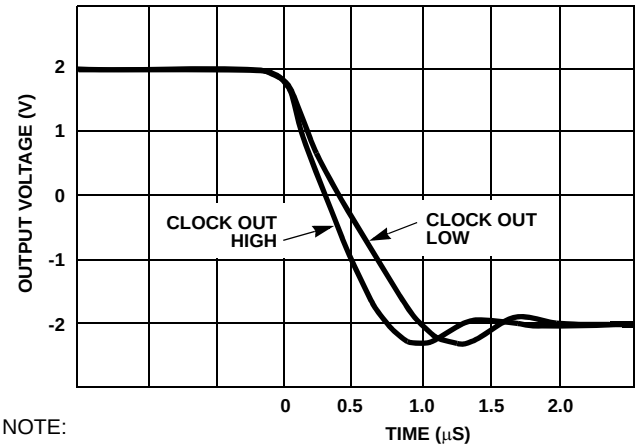


FIGURE 17. OPEN LOOP GAIN AND PHASE SHIFT vs FREQUENCY



NOTE: The two different responses correspond to the two phases of the clock.

FIGURE 18. VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE (NOTE)



NOTE:
The two different responses correspond to the two phases of the clock.

FIGURE 19. VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE (NOTE)

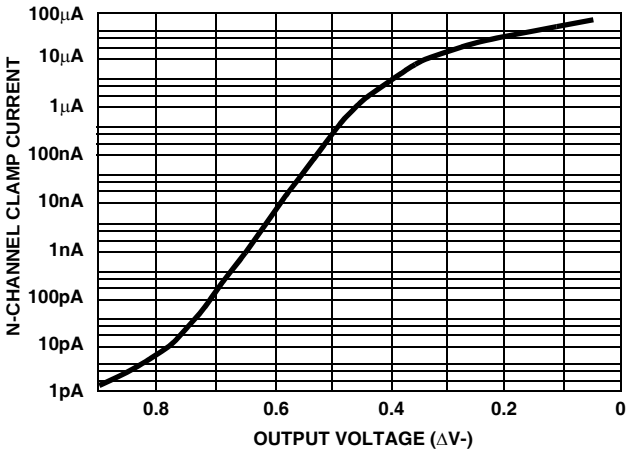


FIGURE 20. N-CHANNEL CLAMP CURRENT vs OUTPUT VOLTAGE

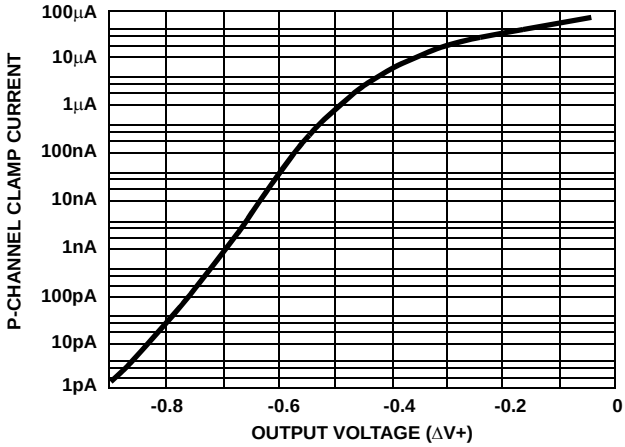
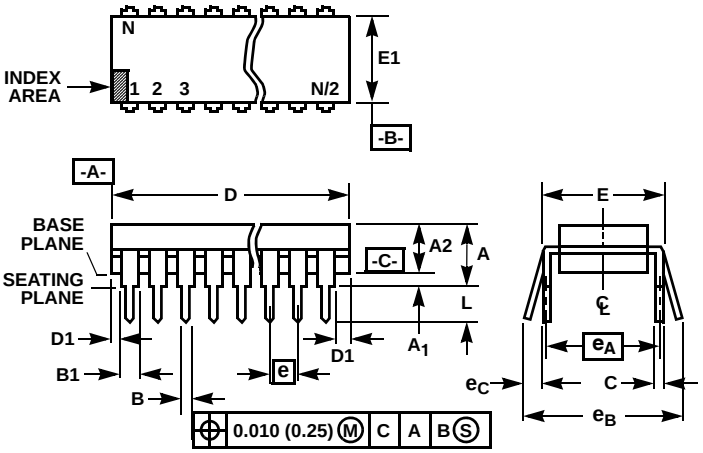


FIGURE 21. P-CHANNEL CLAMP CURRENT vs OUTPUT VOLTAGE

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

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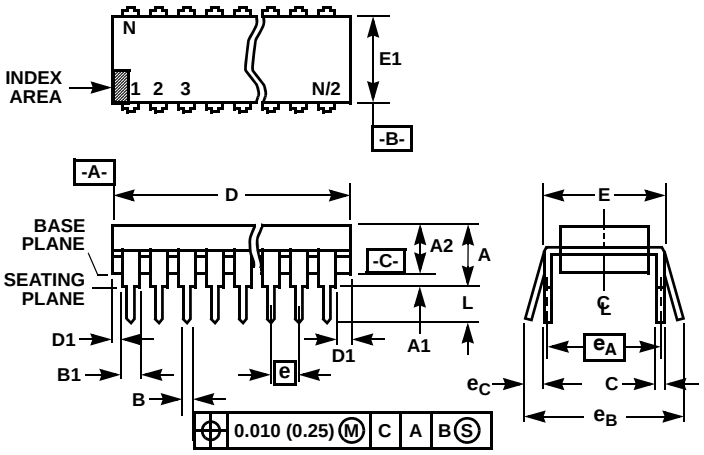
Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E14.3 (JEDEC MS-001-AA ISSUE D)
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

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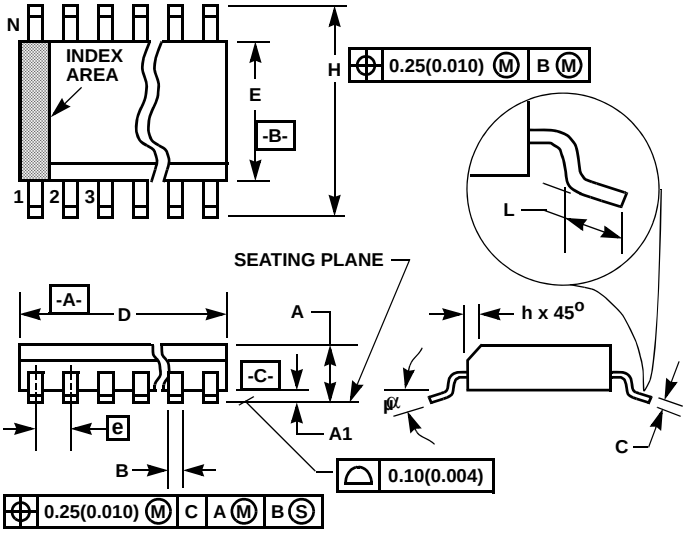
Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

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