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PowerLAN™ Dual-Cell Li-Ion Battery Monitor with PowerPump™ Cell Balancing

FEATURES

- Monitors One or Two Individual Cell Voltages, One Internal, and Two External Temperatures
- Part of a Complete Low-Cost Solution for Battery Packs of up to 12 Series and One or More Parallel Cells (When Used With bq78PL114).
- Advanced PowerPump™ Balancing
 Technology Equalizes Cells in Li-Ion Battery
 Packs, Resulting in Longer Run Time and Cell
 Life.
- PowerPump[™] Cell Balancing Transfers
 Charge From Cell to Cell During all Operating
 Conditions No Wasteful Current Bleeding or
 Associated Heat Buildup.
- Unique PowerLAN™ Isolated Communications Technology Permits Simultaneous Measurement of All Individual Cell Voltages in a Series String.
- Very Low Power Consumption:
 - <200 μA Active
 - <50 μA Standby
 - <1 μA Undervoltage Shutdown</p>
- Connects Directly to Cells, No Resistive Dividers
- Internal LDO Regulator for Support Circuitry
- Ultrasmall Footprint, 3-mm × 3-mm
- Millivolt Measurement Resolution Using Delta-Sigma A/D Converter
- Self-Calibrating Time Base No Crystal Required

APPLICATIONS

- Uninterruptible Power Supplies (UPS)
- Portable Medical and Test Equipment
- Electric Bikes and Mild-EV Battery Packs
- Multicell Series Strings ≥ 5S

RELATED DEVICES

- bq78PL114 Master Gateway Battery Controller
- bq76PL104 Quad-Cell Battery Monitor With PowerPump Cell Balancing* (*Note: bq76PL104 Available 2009.)

DESCRIPTION

The bq76PL102 PowerLAN dual-cell battery monitor is part of a complete scalable battery management system for use with arrays of up to 12 Li-lon rechargeable cells. The bq76PL102 connects to one or two cells in a series string, performs voltage and temperature monitoring of each individual cell, and reports these parameters over the PowerLAN communication network. Together with a bq78PL114 master-gateway battery controller, the bq76PL102 forms а complete battery monitoring management system for higher cell-count applications.

Partitioning of the battery monitor function on a per cell basis permits connection and measurement close to the cell. This results in superior accuracy and management over competing solutions. This scheme also facilitates the PowerPump cell balancing system, a technique which actively balances capacities of Li-lon batteries without the excessive heat or limitations of bleed-balancing techniques.

The bq76PL102 PowerPump cell balancing technology uses a charge-transfer methodology which does not bleed off excess energy as heat, but instead moves energy dynamically from cell to cell as needed. Balancing is performed during all battery operational modes — charge, discharge, and rest. Balancing is automatically coordinated between all cells on a PowerLAN system. PowerPump balancing technology results in longer run time and longer cell life.

The PowerLAN communications architecture has been engineered to provide robust communications in tough EMI/RFI environments while avoiding the excessive power draw, high parts count, and elevated cost of other solutions. PowerLAN permits easy scalability using series connections of bq76PL102 dual-cell battery monitors. High-cell-count battery systems of up to 12 series cells are easily constructed without complicated high-voltage cell measurement restrictions.

The bq76PL102 works with the bq78PL114 master-gateway battery controller and bq76PL104 quad-cell monitors*.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

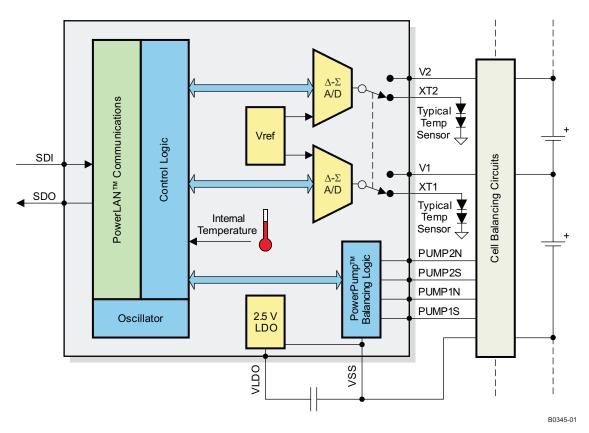


Figure 1. bq76PL102 Simplified Internal Block Diagram

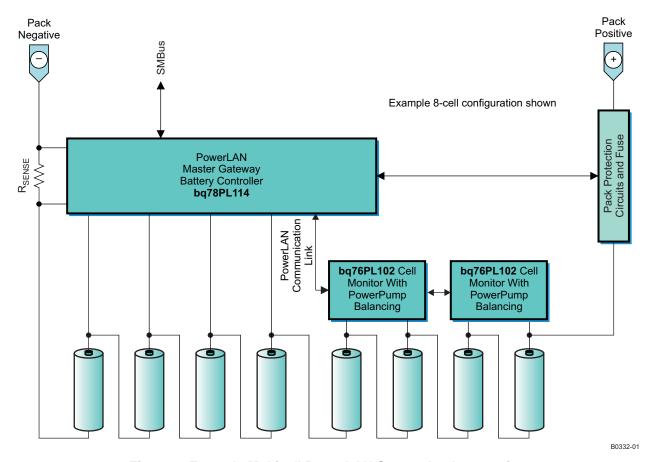


Figure 2. Example Multicell PowerLAN System Implementation

AVAILABLE OPTIONS

The bq76PL102 is currently available in a 3-mm square QFN-16 package, bq76PL102RGT, with a rated operational temperature range of -40°C to 85°C. (See Figure 5 for specific package information, dimensions, and tolerances.)

- Order bq76PL102RGTT for 250 quantity, tape and reel
- Order bq76PL102RGTR for 3000 quantity, tape and reel

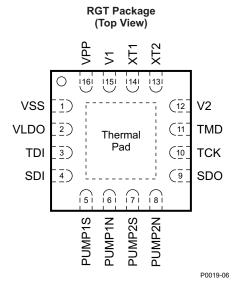


Figure 3. bq76PL102 Pinout (Top View)

CAUTION:

This device is subject to damage from Electrostatic Discharge (ESD). The device should be stored and handled using appropriate ESD precautions to prevent damage to the internal circuitry.

PIN FUNCTIONS

PIN		I/O ⁽¹⁾	DESCRIPTION ⁽²⁾		
NAME	NO.	1/0(1)	DESCRIPTION**		
PUMP1N	6	OD	Charge-balance gate drive for cell 1 north		
PUMP1S	5	OD	Charge-balance gate drive for cell 1 south		
PUMP2N	8	OD	Charge-balance gate drive cell 2 north		
PUMP2S	7	OD	Charge-balance gate drive cell 2 south		
SDI	4	I	PowerLAN serial data input from lower south, downstream part		
SDO	9	0	PowerLAN serial data output to north, upstream part		
XT1	14	IA	External temperature sensor 1 input (calibrated 50 μA)		
XT2	13	IA	External temperature sensor 2 input (calibrated 50 μA)		
TCK	10	NC	Do not connect		
TDI	3	NC	o not connect		
TMD	11	NC	Do not connect		
V1	15	IA	Midpoint cell connection (cell 1 positive and cell 2 negative)		
V2	12	P, IA	Connect to most-positive cell voltage (cell 2 positive)		
VLDO	2	Р	Low-dropout regulator output – connect to VPP (bypass with 4.7 μF capacitor)		
VPP	16	Р	Connect to VLDO		
VSS	VSS 1 P Connect to most-negative cell voltage (cell 1 negative)		Connect to most-negative cell voltage (cell 1 negative)		
	_	Р	Thermal pad – connect to VSS		

⁽¹⁾ I - input, IA - analog input, O - output, OD - open-drain output, P - power, NC - no connect

⁽²⁾ Cell numbering convention is from more-negative (cell 1) to more-positive (cell 2) and is locally referenced.



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNITS
T _A	Operating free-air temperature (ambient)	-40 to 85	°C
T _{stg}	Storage temperature	-65 to 150	°C
Voltage on SDO	Note: not VSS-referenced	$(V1 - 0.5)$ to $(V2 + 0.5)^{(2)}$	V
Voltage on SDI	Limited by lower cell voltage	$(VSS - 0.5)$ to $(V1 + 0.5)^{(2)}$	V
Voltage on V1 (V1 – VSS) ⁽²⁾	Maximum cell voltage	-0.5 to 5	V
Voltage on V2 (V2 – V1) (2)	Maximum cell voltage (not VSS-referenced)	-0.5 to 5	V
Voltage on XT1 or XT2	With respect to VSS	(VSS – 0.5) to (V1 + 0.5)	V
ESD tolerance	JEDEC, JESD22-A114 human-body model, R = 1500 Ω , C = 100 pF	2	kV
Lead temperature, soldering	Total time < 3 seconds	< 300	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is note implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

 $T_A = -40$ °C to 85°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
DC CHAP	DC CHARACTERISTICS						
v (1)	Cell voltage input	Two cell configuration	2.5	3.6	4.5	V	
V _{CELL} ⁽¹⁾		One cell configuration	2.5	3.6	4.5		
I _{DD2}	Operating current (cell 2)	Measuring, reporting, or balancing		250		μΑ	
I _{STBY}	Standby-mode current (cell 2)	Idle		50		μΑ	
I _{UVM} ⁽²⁾	Cell low-voltage-mode current (cell 2)	V1 < 2.7 V		1		μΑ	
I _{DD1}	Quiescent current (Cell 1)	All modes		3		μΑ	
V _{OL}	General I/O characteristics	I _{OL} < 1.0 mA	0		0.5	V	
V _{OH}	General I/O characteristics	I _{OH} < -1.0 mA	V _{LDO} - 0.1			V	
V _{IL}	General I/O characteristics				0.25 V _{LDO}	V	
V _{IH}	General I/O characteristics		0.75 V _{LDO}			V	
CELL VO	LTAGE MEASUREMENT CHARACTERIS	TICS					
	V1 measurement range		2.5		4.5	V	
	V2 measurement range		1.6		4.5	V	
	Analog resolution			<1		mV	
	Accuracy (After calibration)	25°C		±5		mV	
	Accuracy (After calibration)	0°C to 60°C		±10		mV	
	Conversion time ⁽³⁾				80	ms	
INTERNAL TEMPERATURE MEASUREMENT CHARACTERISTICS							
	Measurement range		-30		85	°C	
	Resolution			0.1		°C	
	Accuracy (after calibration)	0°C to 85°C		±2		°C	

⁽¹⁾ Device remains operational to 1.85 V with reduced accuracy and performance.

⁽²⁾ Cell numbering convention is from most negative (Cell 1) to most positive (Cell 2) and is locally referenced.

⁽²⁾ Condition forced by bq78PL114 command and when V1 < 2.7 V.

³⁾ Does not include delay due to internode timing delays.

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TEXAS INSTRUMENTS

ELECTRICAL CHARACTERISTICS (continued)

 $T_A = -40$ °C to 85°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
EXTERNAL TEMPERATURE SENSOR(s) TYPICAL CHARACTERISTICS (4)						
Measurement range ⁽⁵⁾		-40		90	°C	
Resolution			0.2		°C	
Accuracy ⁽⁶⁾	25°C		±1		°C	
Accuracy	0°C to 60°C		±2		°C	

- (4) Typical for dual-diode (MMBD4148 or equivalent) external sensor using recommended circuit.
- 5) Range of diode sensors may exceed operation limits of IC and battery cells.
- (6) Typical behavior after calibration; final result depends on specific component characteristics.

FEATURE SET

The bq76PL102 dual-cell li-ion battery monitor with PowerPump balancing implements battery voltage measurement, temperature measurement, and balancing for one or two Li-lon cells in series, and any number in parallel (limited by other design considerations).

Functions include:

- Simultaneous, synchronous measurement of all cell voltages in a series string
- Asynchronous reporting of most-recent measurements for each cell
- Fully independent measurements on a cell-by-cell basis
- PowerPump cell balancing using charge transfer from cell to cell
- PowerLAN isolated communications to other bq76PL102 devices or bq78PL114 master-gateway battery-management controller
- Low-power operation

OPERATION

Cell-Voltage Measurement

Voltage measurements are made using one-per-cell precision delta-sigma analog-to-digital converters (ADC). An internal calibrated band-gap voltage reference is provided with each part. Measurements are performed when commanded by the bq78PL114 master-gateway battery-management controller via the one-wire PowerLAN serial communications bus. This allows all cells to be measured at exactly the same time under the same load conditions.

Cell-Temperature Measurement

Temperature measurements can be obtained using one internal and up to two external sensors. Each external sensor consists of one (or two for increased accuracy) series-connected diodes and a capacitor for filtering. The use of dual diodes in a single SMT package is recommended (MMBD4148SE or equivalent). The diode can be located up to 6 inches (15.c cm) from the circuit board. The RF filter capacitor should be co-located very close to the diode to minimize unwanted noise coupling.

The temperature measurement subsystem uses the same dual ADCs that are used for measuring voltages. Temperature measurements are fully independent of voltage readings, and are ordinarily interleaved at a fractional rate of the voltage readings by commands from the bq78PL114 master-gateway battery-management controller.

Cell Balancing

Balancing is provided among any number of supported cells. The bq76PL102 and PowerLAN family of master-gateway battery controllers is optimized for designs using more than four cells in series.

The patented PowerPump reactive cell balancing dramatically increases the useful life of battery systems by eliminating the cycle life fade of multicell batteries due to cell imbalance. PowerPump efficiently transfers charge from cell to cell, rather than simply bleeding off charging energy as heat. Charge is moved from higher-capacity

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cells to lower-capacity ones, and can be moved as needed between any number of series cell elements. Balancing is performed during all battery operational modes – charge, discharge, and rest. Compared to resistive bleed balancing, virtually no energy is lost as heat. The actual balance current is externally scalable with component selection and can range from 10 mA to 1 A (100 mA typical) depending on application or cell requirements. (See the reference schematic, Figure 7.)

Algorithms for cell balancing are centrally coordinated by the bq78PL114 PowerLAN master-gateway battery-management controller and directed across the array of bq76PL102 dual-cell Li-lon battery monitors. Balancing is done in both directions by the bq76PL102s within the cell stack array: *north* or up the cell stack and *south* or down the cell stack. Each bq76PL102 node provides the circuitry to transfer (pump) the charge from cell to cell to provide balancing. The balancing algorithm is implemented in the bq78PL114 master-gateway battery controller, and commands are communicated to the bq76PL102s via the PowerLAN communications link. By tracking the balancing required by individual cells, overall battery safety is enhanced – often allowing early detection of internal micro-shorts or other cell failures.

Cell balancing *pumping*, or charge transfer from one cell to another, is accomplished using a circuit that forms a simple flyback converter under control of the bq76PL102, which is in turn controlled by the master gateway. The outputs of PUMP*nd* (*cell number, direction*) control MOSFET transistors which charge an inductor from one cell and then discharge the inductor into an adjacent cell through the intrinsic body diode of the other MOSFET.

- PUMP1S: Pumps charge from cell 1 to the next lower cell (closer to battery negative). This signal is unused
 by the first or lowest cell in the string.
- PUMP1N: Pumps charge from cell 1 to cell 2.
- PUMP2S: Pumps charge from cell 2 to cell 1
- **PUMP2N:** Pumps charge from cell 2 to the next higher cell in a pack (closer to battery positive). This signal is unused by the highest cell in the string.

PowerLAN Communications

PowerLAN communications technology is a patented serial network and protocol designed specifically for battery management in a multicell environment. PowerLAN is used to initiate and report measurements of cell voltage and temperature, as well as control cell balancing. Using only a capacitor, PowerLAN isolates voltages from adjacent bq76PL102 parts to permit high-voltage stack assemblies without compromising precision and accuracy. PowerLAN is expandable to support up to 12 cells in series, with each bq76PL102 handling two series cells. PowerLAN provides high ESD standoff and high immunity to noise generated by nearby digital circuitry or switching currents. Each bq76PL102 has both a PowerLAN serial input and serial output pin. Received data is buffered and retransmitted, permitting high numbers of nodes without loss of signal fidelity. Signals are capacitor-coupled between nodes to provide high dc isolation.

Operations Modes

The bq76PL102 normally operates in one of two modes: active or standby. The bq76PL102 is normally in standby mode and consumes typically less than 50 μ A. The low-dropout regulator output is still functional in this mode, as are internal system protection functions (undervoltage, communications timeout, etc.)

When a PowerLAN communications event occurs, then the bq76PL102 transitions to active mode and power consumption increases to 200 A typically. The bq76PL102 stays in this mode to complete any measurements or cell-balancing pumping operations. Once activity in this mode ceases, the return to standby is automatic, thus reducing overall power consumption.

An undervoltage ultralow-power-consumption mode is also available when initiated by the bq78PL114 master-gateway battery controller and when the cell voltages drop below a preset threshold. This mode is used to preserve battery capacity during long periods of non-use and therefore has a power consumption of approximately 1 μ A.

Note that cell balancing currents are external to the bq76PL102 and may be sized according to the needs of the application (typically 10 mA to 1 A). These currents are fixed by the cell-balancing circuitry and only enabled or disabled by the bq76PL102 (under control of the bq78PL114) to achieve the necessary cell-balance operations.

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COMPLEMENTARY PRODUCTS

PowerLAN Master Gateway Battery Controller

The bq78PL114 master-gateway battery-management controller with PowerPump cell balancing from Texas Instruments is the central controller for a complete multicell battery system.

This advanced master-gateway battery controller works with up to 12 series cells monitored by bq76PL102 or bq76PL104* (*available 2009) cell monitors to provide battery voltage, temperature, current and safety monitoring; state-of-charge and state-of-health information; system-wide internal PowerLAN communications; as well as external communications of battery parameters via the industry-standard SMBus interface.



PowerLAN Quad-Cell Battery Monitor* (Available 2009*)

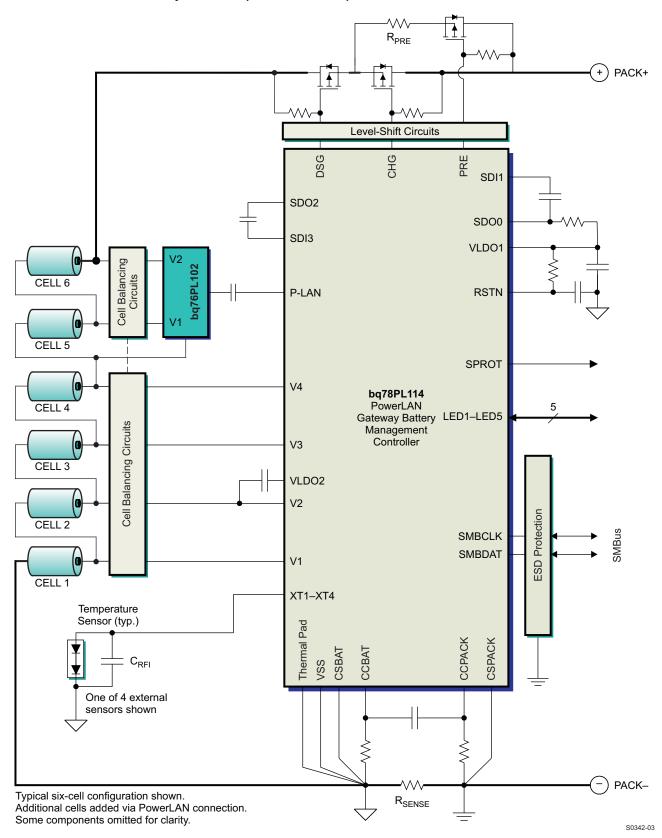


Figure 4. bq78PL114 Simplified 6-Cell Gateway Controller Circuit With bq76PL102

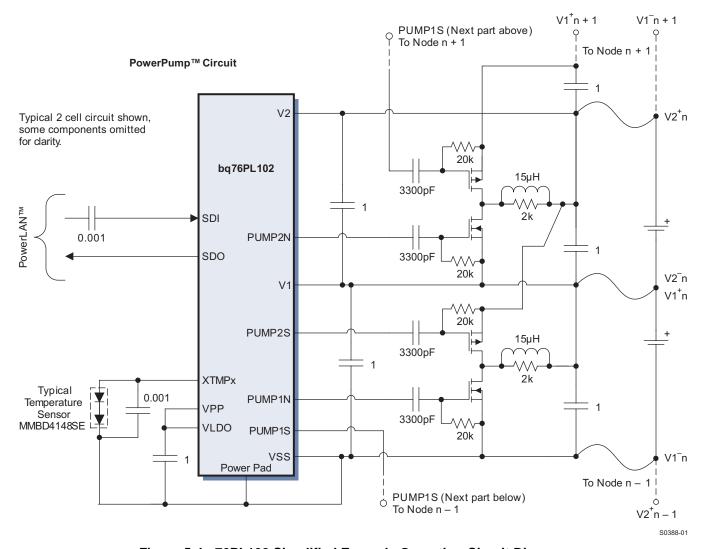


Figure 5. bq76PL102 Simplified Example Operating-Circuit Diagram



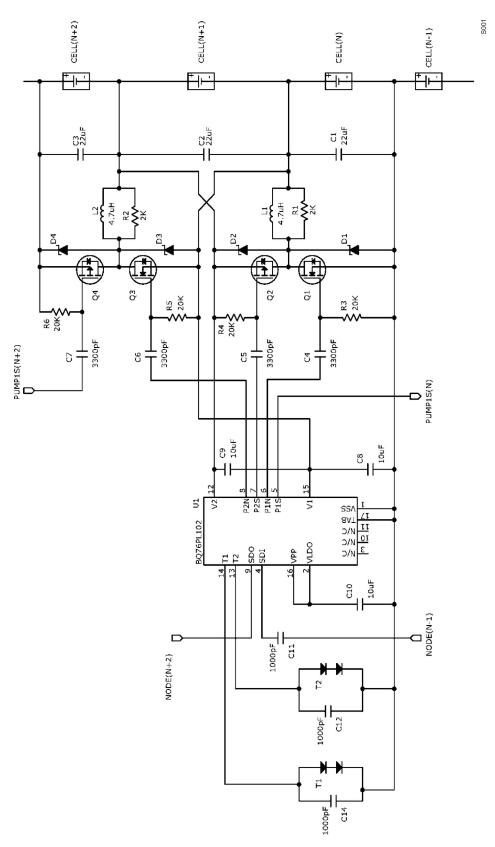


Figure 6. Higher-Balancing-Current bq76PL102 Operating-Circuit Diagram

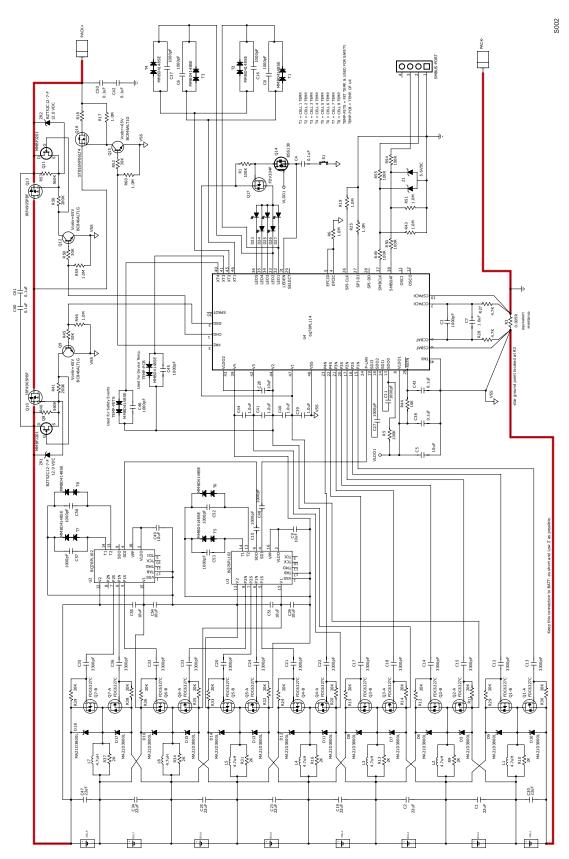
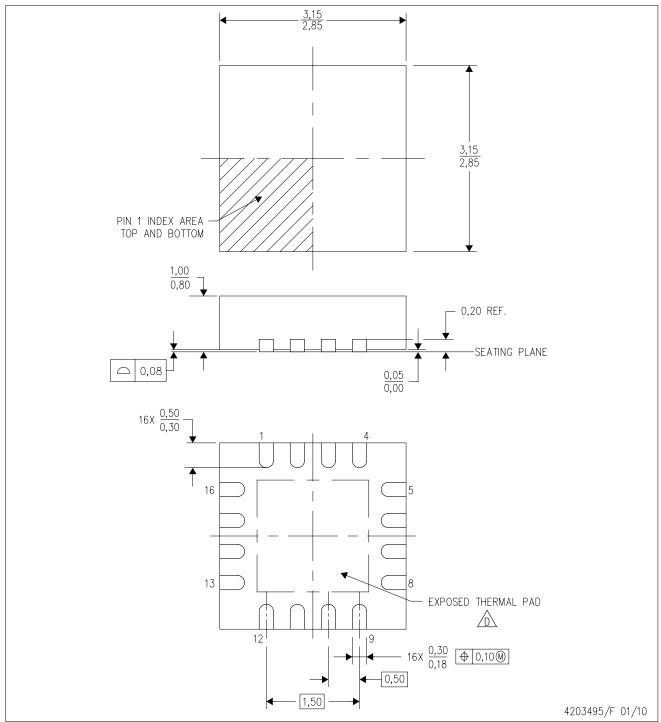


Figure 7. Reference Schematic

RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No-leads (QFN) package configuration.

The package thermal pad must be soldered to the board for thermal and mechanical performance.

See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

E. Falls within JEDEC MO-220.



THERMAL PAD MECHANICAL DATA



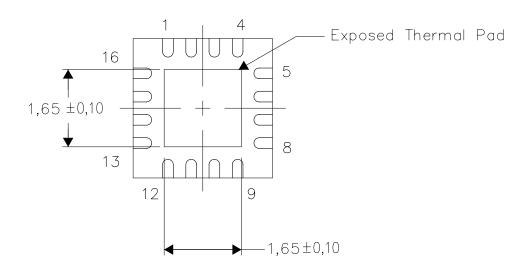
RGT (S-PVQFN-N16)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No—Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No—Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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