

November 2009

# FSA2269 / FSA2269TS — Low-Voltage Dual-SPDT (0.4 $\Omega$ ) Analog Switch with Negative Swing Audio Capability

### **Features**

- 0.4Ω Typical On Resistance (R<sub>ON</sub>) for +3.0V Supply
- 0.25Ω Maximum R<sub>ON</sub> Flatness for +3.0V Supply
- -3db Bandwidth: > 50MHz
- Low-I<sub>CCT</sub> Current Over an Expanded Control Input Range
- Packaged in 10-Lead MicroPak™ and UMLP
- Power-Off Protection on Common Ports
- Broad V<sub>CC</sub> Operating Range: 1.65 to 4.3V
- Noise Immunity Termination Resistors in FSA2269TS

## **Applications**

- Cell Phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box

## **Description**

The FSA2269 is a high-performance, dual Single-Pole Double-Throw (SPDT) analog switch with negative swing audio capability. The FSA2269 features ultra-low  $R_{ON}$  of  $0.4\Omega$  (typical) at 3.0V  $V_{CC}$ . The FSA2269 operates over a wide  $V_{CC}$  range of 1.65V to 4.3V, is fabricated with submicron CMOS technology to achieve fast switching speeds, and is designed for break-before-make operation. The select input is TTL-level compatible.

The FSA2269 features very low quiescent current even when the control voltage is lower than the  $V_{\rm CC}$  supply. This feature suits mobile handset applications by allowing direct interface with baseband processor general-purpose I/Os with minimal battery consumption.

The FSA2269TS includes termination resistors that improve noise immunity during overshoot excursions, off-isolation coupling, or "pop-minimization."

### **IMPORTANT NOTE:**

For additional information, please contact <a href="mailto:analogswitch@fairchildsemi.com">analogswitch@fairchildsemi.com</a>.

# **Ordering Information**

_						
Part Number	Top Mark	© Eco Status	Package Description			
FSA2269L10X HL RoHS 10-Lead, MicroPak, JEDEC MO-255, 1.6 x 2.1mm						
FSA2269UMX	HP	Green	10-Lead, Quad Ultrathin Molded Leadless Package (UMLP), 1.4 x 1.8mm, 0.4 mm pitch			
FSA2269TSL10X	HU	10-Lead, MicroPak, JEDEC MO-255, 1.6 x 2.1mm				
TESAZZNYISHIVIX I HI I GREEN I			10-Lead, Quad Ultrathin Molded Leadless Package(UMLP), 1.4 x 1.8mm, 0.4mm pitch			

For Fairchild's definition of Eco Status, please visit: <a href="http://www.fairchildsemi.com/company/green/rohs\_green.html">http://www.fairchildsemi.com/company/green/rohs\_green.html</a>.

# **Analog Symbols**

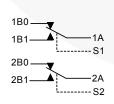


Figure 1. FSA2269

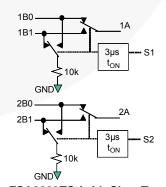
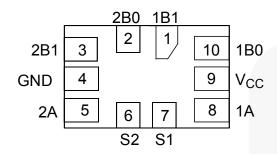


Figure 2. FSA2269TS (with Slow Turn On)

# **Pin Configuration**





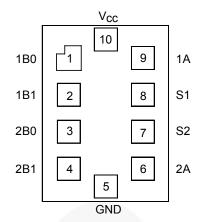


Figure 4. 10-Pin MicroPak™ (Top Through View)

# **Pin Descriptions**

Pin # UMLP	Pin # Micropak	Name	Description		
1	2	1B1	Data Ports		
2	3	2B0	Data Ports		
3	4	2B1	Data Ports		
4	5	GND	Ground		
5	6	2A	Switch Select Pins		
6	7	S2	Switch Select Pins		
7	8	S1	Switch Select Pins		
8	9	1A	Data Ports		
9	10	V <sub>CC</sub>	Supply Voltage		
10	1	1B0	Data Ports		

# **Truth Table**

Control Input, Sn	Function
LOW Logic Level	nB0 connected to nA (FSA2269/2269TS); nB1 terminated to GND (FSA2269TS only)
HIGH Logic Level	nB1 connected to nA(FSA2269/2269TS); nB0 terminated to GND (FSA2269TS only)

# **Absolute Maximum Ratings**

Stresses exceeding the absolute maximum ratings may damage the device. Functional operation above the recommended operating conditions is not implied. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. Absolute maximum ratings are stress ratings only.

Symbol		Parameter			Min.	Max.	Unit
V <sub>CC</sub>	Supply Voltage				-0.5	5.5	V
$V_{SW}$	Switch I/O Voltage <sup>(1)</sup>	1B0, 1B1, 2B0, 2B	31, 1A, 2	2A Pins	V <sub>CC</sub> -4.6V	V <sub>CC</sub> +0.3V	V
V <sub>CNTRL</sub>	Control Input Voltage <sup>(1)</sup>	S1, S2			-0.5	V <sub>CC</sub> +0.3V	V
I <sub>IK</sub>	Input Clamp Diode Current					- 50	mA
I <sub>SW</sub>	Switch I/O Current (Continuous)					350	mA
ISWPEAK	Peak Switch Current	Pulsed at 1ms Du	ration, <	10% Duty Cycle		500	mA
T <sub>STG</sub>	Storage Temperature Range				-65	+150	°C
TJ	Maximum Junction Temperature	e				+150	°C
TL	Lead Temperature		Solde	ering, 10 Seconds		+260	°C
MSL	Moisture Sensitivity Level (JEDI	EC J-STD-020A)			1	Level	MSL
			I/O to	GND	\	12	kV
ESD	Human Body Model (JEDEC: J	ESD22-A114)	Powe	er to GND		8	kV
ESD			All O	ther Pins		7	kV
	Charged Device Model (JEDEC	: JESD22-C101)				2	kV

#### Note

1. Input and output negative ratings may be exceeded if input and output diode current ratings are observed.

# **Recommended Operating Conditions**

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	1.65V	4.3	V
V <sub>S1, S2</sub>	Control Input Voltage	٥V	Vcc	V
$V_{SW}$	Switch I/O Voltage	V <sub>CC</sub> -4.6	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature	-40°C	+85	°C

### **DC Electrical Characteristics**

All typical values are at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V <sub>cc</sub> (V)	٦	Γ <sub>A</sub> =+25 <sup>0</sup>	C	T <sub>A</sub> =-40 to +85°C		Unit	
				Min.	Тур.	Max.	Min.	Max.		
			3.60 to 4.30				1.70			
			3.00 to 3.60				1.50			
$V_{IH}$	Input Voltage High		2.70 to 3.00				1.35		V	
			2.30 to 2.70				1.30		v	
			1.65 to 1.95				0.90			
			3.60 to 4.30					0.7	V	
VII	Input Voltage Low		2.70 to 3.60					0.5		
▼ IL	input voltage zon		2.30 to 2.70					0.4	V	
			1.65 to 1.95					0.4		
$I_{\text{IN}}$	Control Input Leakage (S1,S2)	V <sub>IN</sub> =0 to V <sub>CC</sub>	1.65 to 4.30				-0.5	0.5	μΑ	
I <sub>NO(0FF)</sub> , I <sub>NC(OFF)</sub>	Off Leakage Current of Port nB0 and nB1 (FSA2269 only)	nA=0.5V, V <sub>CC</sub> -0.5V nB0 or nB1=V <sub>CC</sub> - 0.5V, 0.5V, or Floating Figure 6	1.95 to 4.30	-50		50	-250	250	nA	
I <sub>NC(OFF)</sub>	Off Leakage Current of Port nB0 and nB1 (FSA2269TS)	nA=0.5V, V <sub>CC</sub> –0.5V nB0 or nB1=0V or Floating Figure 6	1.95 to 4.30	-2		2	-6	6	μΑ	
I <sub>A(ON)</sub>	On Leakage Current of Port nA	nA=0.5V, $V_{\rm CC}$ –0.5V nB0 or nB1= $V_{\rm CC}$ – 0.5V, 0.5V, or Floating Figure 7	1.95 to 4.30	-20		20	-150	150	nA	
	Power-Off Leakage Current (Common Port Only 1A, 2A) (FSA2269)	Common Port (1A, 2A), V <sub>IN</sub> =0V to 4.3V, V <sub>CC</sub> =0V nB0, nB1=Floating	0V					±1	μΑ	
I <sub>OFF</sub>	Power-Off Leakage Current (Common Port Only 1A, 2A) (FSA2269TS)	Common Port (1A, 2A), V <sub>IN</sub> =0V to 4.3V, V <sub>CC</sub> =0V nB0, nB1=0V or Floating	0V					±45	μΑ	
		I <sub>ON</sub> =100mA, nB0 or nB1=0.7V, 3.6V, 4.3V Figure 5	4.30		0.30					
	Switch On	I <sub>ON</sub> =100mA, nB0 or nB1=0.7V, 3.6V, 4.3V Figure 5	3.00		0.40			0.80		
R <sub>ON</sub>	Resistance <sup>(2,5)</sup>	I <sub>ON</sub> =100mA, nB0 or nB1=0V, 0.7V, 1.6V, 2.3V, Figure 5	2.30		0.52			(F	Ω	
		I <sub>ON</sub> =100mA, nB0 or nB1=0V, 0.7V, 1.65V Figure 5	1.65		1.00					
	On Danistana		4.30		0.04			0.13		
$\Delta R_{ON}$	On Resistance Matching Between	I <sub>ON</sub> =100mA, nB0 or	3.00		0.06			0.13	Ω	
△i <b>≀</b> ON	Channels <sup>(3)</sup>	nB1=0.7V	2.30		0.12				1 32	
			1.65		1.00					

# DC Electrical Characteristics (Continued)

All typical values are at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V <sub>cc</sub> (V)	T <sub>A</sub> =+25°C			T <sub>A</sub> =-4	Unit	
			,	Min.	Тур.	Max.	Min.	Max.	
			4.30					0.25	
<sub>D</sub>	On Resistance	I <sub>OUT</sub> =100mA, nB0 or	3.00					0.25	Ω
R <sub>FLAT(ON)</sub>	Flatness <sup>(4)</sup>	nB1=0V to V <sub>CC</sub>	2.30		0.5				12
			1.65		0.6				
R <sub>TERM</sub>	Internal Termination Resistors <sup>(5)</sup>				10				kΩ
Icc	Quiescent Supply Current	V <sub>IN</sub> =0 or V <sub>CC</sub> , I <sub>OUT</sub> =0	4.30	-100		100	-500	500	nA
l	Increase in I <sub>CC</sub> per	Input at 2.6V	4.30		3.0			10.0	
Ісст	Input	Input at 1.8V	4.30		7.0			15.0	μA

### Notes:

- On resistance is determined by the voltage drop between A and B pins at the indicated current through the switch.
- $\Delta$  R<sub>ON</sub>=R<sub>ON max</sub> R<sub>ON min</sub> measured at identical Vcc, temperature, and voltage. Flatness is defined as the difference between the maximum and minimum value of on resistance (R<sub>ON</sub>) over the specified range of conditions.
- Guaranteed by characterization, not production tested.

# **AC Electrical Characteristics**

All typical value are for  $V_{CC}$ =3.3V,  $V_{BUS}$ =5.0V at 25°C unless otherwise specified.

Symbol Parameter		Conditions	Conditions V <sub>cc</sub> (V)		T <sub>A</sub> =+25°C			10 to 5°C	Unit	Figure		
			100 (1)	Min.	. Typ. Max. I	Min.	Max.		ga 0			
		nB0 or	3.60 to 4.30			55	15	60				
	Turn-On Time	nB1=1.5V,	2.70 to 3.60			60	15	65	j	Figure 8		
	FSA2269	FSA2269	FSA2269	$R_L=50\Omega$ ,	2.30 to 2.70			100	15	110	ns	Figure 9
		C <sub>L</sub> =35pF	1.65 to 1.95		70							
t <sub>ON</sub>		nB0 or	3.60 to 4.30			3.5	0.5	4.0				
	Turn-On Time	nB1=1.5V,	2.70 to 3.60			4.5	0.5	5.0	Ì	Figure 8		
	FSA2269TS	R <sub>L</sub> =50Ω,	2.30 to 2.70			6.0	0.5	7.0	μs	Figure 9		
		C <sub>L</sub> =35pF	1.65 to 1.95		8.0				ĺ			
	-/	nB0 or	3.60 to 4.30			50	5	55				
	Turn-Off Time	nB1=1.5V,	2.70 to 3.60			55	5	60		Figure 8		
	FSA2269	R <sub>L</sub> =50Ω,	2.30 to 2.70			60	5	65	ns	Figure 9		
. /		C <sub>L</sub> =35pF	1.65 to 1.95		40				ĺ			
t <sub>OFF</sub>		nB0 or	3.60 to 4.30			45	5	50				
	Turn-Off Time	nB1=1.5V.	2.70 to 3.60			50	5	55	55	Figure 8		
	FSA2269TS	FSA2269TS	R <sub>L</sub> =50Ω,	2.30 to 2.70			55	5	60	ns	Figure 9	
		C <sub>L</sub> =35pF	1.65 to 1.95		50				7			
		nB0 or	3.60 to 4.30		3		1					
	Break-Before-	nB1=1.5V,	2.70 to 3.60		5		2		]	Figure		
t <sub>BBM</sub>	Make Time FSA2269	R <sub>L</sub> =50Ω,	2.30 to 2.70		10		2		ns	10		
	1 3/2209	C <sub>L</sub> =35pF	1.65 to 1.95		5		2		1			
		nB0 or	3.60 to 4.30		1.5		1.0					
	Break-Before-	nB1=1.5V,	2.70 to 3.60		3.0		1.5			Figure		
t <sub>BBM</sub>	Make Time FSA2269TS	R <sub>L</sub> =50Ω,	2.30 to 2.70		4.0		2.5		ns	10		
	1 0/220910	C <sub>L</sub> =35pF	1.65 to 1.95		5.0		3.0		1			
Q	Charge Injection	$C_L$ =1.0nF, $V_S$ =0V, $R_S$ =0 $\Omega$	1.65 to 4.30		25				рС	Figure 14		
OIRR	Off Isolation	$f=100kHz$ , $R_L=50\Omega$ , $C_L=0pF$	1.65 to 4.30		-70				dB	Figure 12		
Xtalk	Crosstalk	$f=100kHz$ , $R_L=50\Omega$ , $C_L=0pF$	1.65 to 4.30		-70				dB	Figure 13		
BW	-3db Bandwidth	$R_L=50\Omega$ , $C_L=0$ pF	1.65 to 4.30		>50				MHz	Figure 11		
THD	Total Harmonic Distortion	$\begin{array}{l} \text{f=20Hz to} \\ \text{20kHz}, \\ \text{R}_{\text{L}}\text{=}32\Omega, \\ \text{V}_{\text{IN}}\text{=}2\text{V}_{\text{pp}} \\ \text{V}_{\text{BIAS}}\text{=}0\text{V} \end{array}$	1.65 to 4.30		.06				%	Figure 17		

# Capacitance

Symbol	Parameter	Conditions	V (\( \)		T <sub>A</sub> =+25°0	<b>C</b>	Unit	Figure	
Symbol	Farameter	Conditions	V <sub>CC</sub> (V)	Min.	Тур.	Max.	Unit	rigure	
C <sub>IN</sub>	Control Pin Input Capacitance	f=1MHz	0		2.5		pF	Figure 15	
C <sub>OFF</sub>	B Port Off Capacitance	f=1MHz	3.3		30		pF	Figure 15	
C <sub>ON</sub>	A Port On Capacitance	f=1MHz	3.3		120		pF	Figure 16	

# **Test Diagrams**

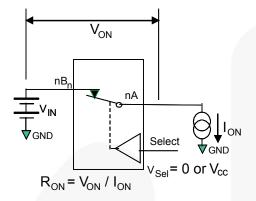
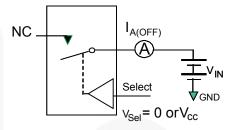


Figure 5. On Resistance



\*\*Each switch port is tested separately.

Figure 6. Off Leakage

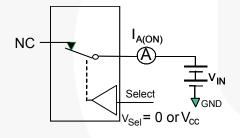


Figure 7. On Leakage

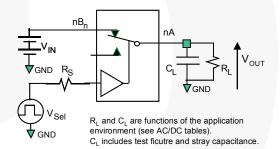


Figure 8. Test Circuit Load

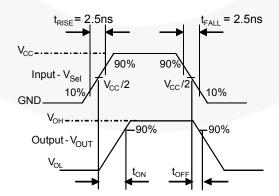


Figure 9. Turn-On / Turn-Off Waveforms

### Test Diagrams (Continued)

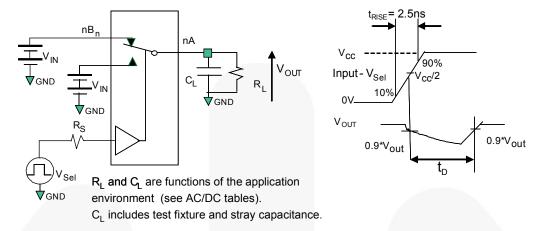


Figure 10. Break-Before-Make Interval Timing

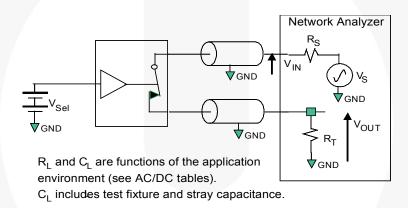


Figure 11. Bandwidth

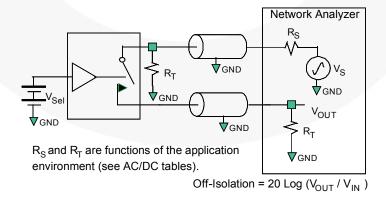


Figure 12. Channel Off Isolation

### Test Diagrams (Continued)

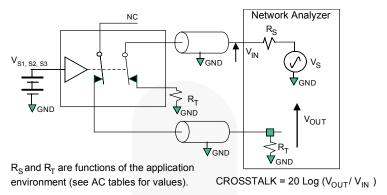


Figure 13. Adjacent Channel Crosstalk

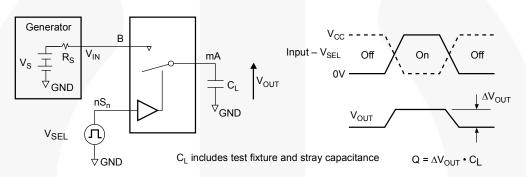
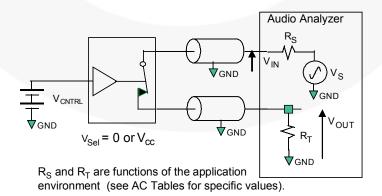


Figure 14. Charge Injection Test



Figure 15. Channel Off Capacitance

Figure 16. Channel On Capacitance



**Figure 17. Total Harmonic Distortion** 

# **Physical Dimensions**

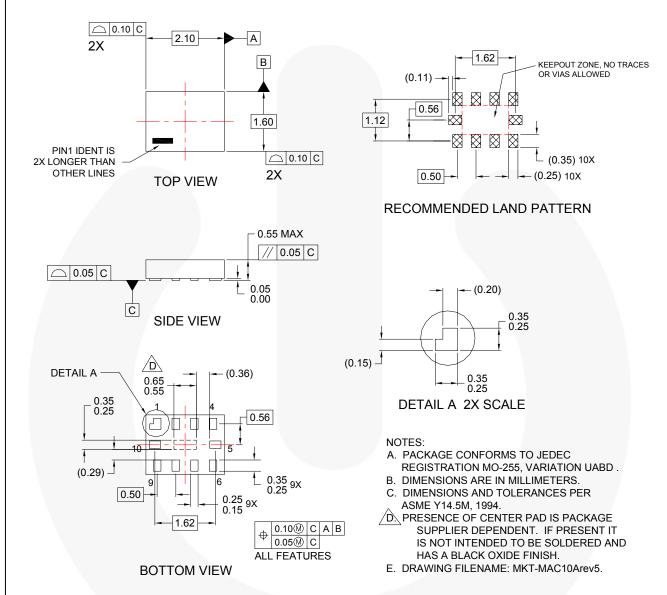
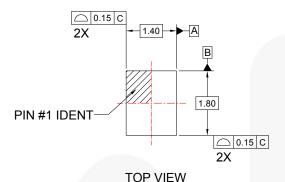


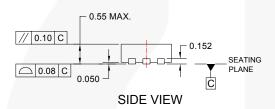
Figure 18. 10-Lead MicroPak™

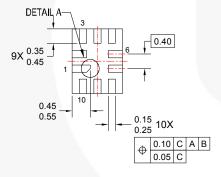
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# **Physical Dimensions**



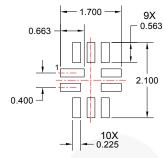




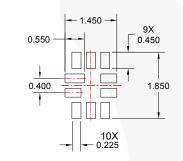
**BOTTOM VIEW** 

### NOTES:

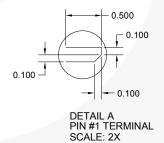
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- B. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- C. DRAWING FILENAME: UMLP10Arev2



RECOMMENDED LAND PATTERN



OPTIONAL MINIMIAL TOE LAND PATTERN



### Figure 19. 10-Lead, Quad Ultrathin Molded Leadless Package (UMLP)

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Programmable Active Droop™

QS™ Quiet Series™ RapidConfigure™

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SMART START™
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SuperSOT™.8
SuperSOT™.8
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### PRODUCT STATUS DEFINITIONS

### **Definition of Terms**

Datasheet Identification	Product Status	Definition					
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.					
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.					
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.					
Obsolete Not In Production		Datasheet contains specifications on a product that is discontinued by Fairchild Semiconduc The datasheet is for reference information only.					

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