SLAS353 − DECEMBER 2001

16-BIT, SINGLE CHANNEL, PARALLEL INPUT DIGITAL-TO-ANALOG CONVERTER WITH RAIL-TO-RAIL VOLTAGE OUTPUT

FEATURES

- **Micropower Operation: 250 μA at 5 V AV_{DD}**
- **Power-On Reset to Min-Scale**
- **16-Bit Monotonic**
- **Settling Time: 10 μs to ±0.003% FSR**
- **16-Bit Parallel Interface**
- **On-Chip Output Buffer Amplifier With Rail-to-Rail Operation**
- **Hardware Reset to Min-Scale or Mid-Scale**
- **Double-Buffered Architecture**
- **Asynchronous LDAC Control**
- **Data Readback Support**
- **1.8 V Compatible Digital Interface:**
  - **DV_{DD} = 1.8 V−5.5 V**
- **Wide Analog Supply Range:**
  - **AV_{DD} = 2.7 V−5.5 V**
- **32-Lead 5 mm × 5 mm TQFP Package**

APPLICATIONS

- **Process Control**
- **Data Acquisition Systems**
- **Closed-Loop Servo Control**
- **PC Peripherals**
- **Portable Instrumentation**

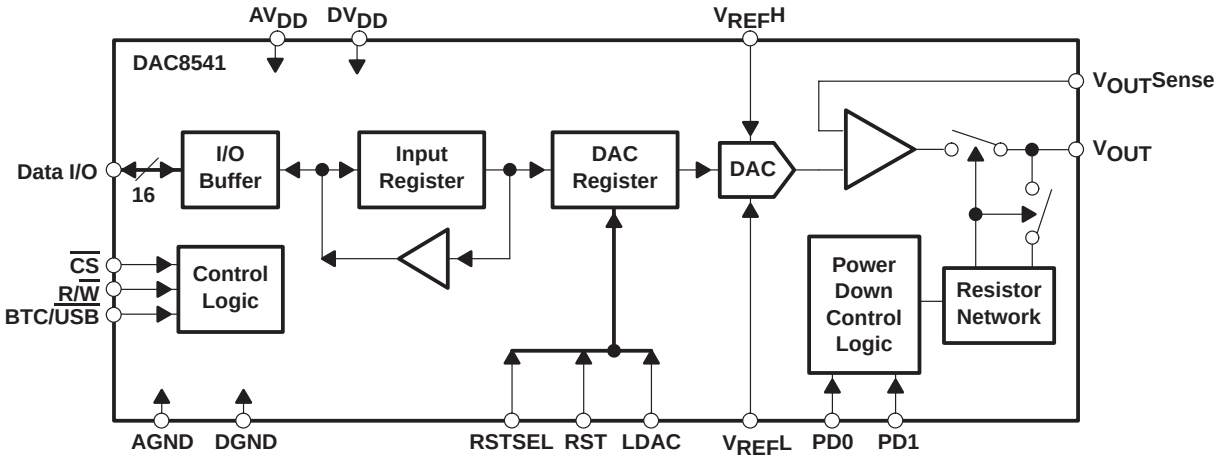
DESCRIPTION

The DAC8541 is a low-power, single channel, 16-bit, voltage output DAC. Its on-chip precision output amplifier allows rail-to-rail voltage swing to be achieved at the output. The DAC8541 utilizes a 16-bit parallel interface and features additional powerdown function pins as well as hardware-enabled, asynchronous DAC updating and reset capability.

The DAC8541 requires an external reference voltage to set the output range of the DAC. The device incorporates a power-on-reset circuit that ensures that the DAC output powers up at min-scale and remains there until a valid write takes place to the device. In addition, the DAC8541 contains a power-down feature, accessed via two hardware pins, that when enabled reduces the current consumption of the device to 200 nA at 5 V.

The low power consumption of this device in normal operation makes it ideally suited for use in portable battery operated equipment applications. The power consumption is 1.2 mW at AV_{DD} = 5 V reducing to 1 μW in power-down mode.

The DAC8541 is available in a 32-lead TQFP package with an operating temperature range of −40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

AVAILABLE OPTIONS

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	T_A	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
DAC8541	32-TQFP	PBS	−40°C to 85°C	E41Y	DAC8541Y/250	Tape and Reel
					DAC8541Y/2K	

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

AV_{DD} to AGND . . . . . −0.3 V to 6 V
DV_{DD} to DGND . . . . . −0.3 V to 6 V
Digital input voltage to DGND . . . . . −0.3 V to DV_{DD} + 0.3 V
V_{OUT} to AGND . . . . . −0.3 V to AV_{DD} + 0.3 V
Operating temperature range . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Junction temperature, T_J max . . . . . 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

electrical characteristics, DV_{DD} = 1.8 V to 5.5 V; AV_{DD} = 2.7 V to 5.5 V; R_L = 2 kΩ to AGND; C_L = 200 pF to AGND; all specifications –40°C to 85°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE (see Note 1)					
Resolution		16			Bits
Relative accuracy				±0.098	%FSR
Differential nonlinearity	16-Bit monotonic			±1	LSB
Zero code error	All zeroes loaded to DAC register		5	20	mV
Full-scale error	All ones loaded to DAC register		–0.15	–0.8	%FSR
Gain error				±0.8	%FSR
Zero code error drift			±20		µV/°C
Gain temperature coefficient			±5		ppm of FSR/°C
OUTPUT CHARACTERISTICS (see Note 2)					
Output voltage range		$2\times V_{REF}L$		$V_{REF}H$	V
Output voltage settling time (full scale)	R_L = 2 kΩ; 0 pF < C_L < 200 pF		8	10	µs
	R_L = 2 kΩ; C_L = 500 pF		12		
Slew rate			1		V/µs
Capacitive load stability	R_L = ∞		470		pF
	R_L = 2 kΩ		1000		
Digital-to-analog glitch impulse	1 LSB change around major carry (see Note 3)		20		nV−s
Digital feedthrough			0.5		nV−s
DC output impedance			1		Ω
Short circuit current	AV_{DD} = 5 V		50		mA
	AV_{DD} = 3 V		20		
Power-up time	Coming out of power-down mode, AV_{DD} = 5 V		2.5		µs
	Coming out of power-down mode, AV_{DD} = 3 V		5		

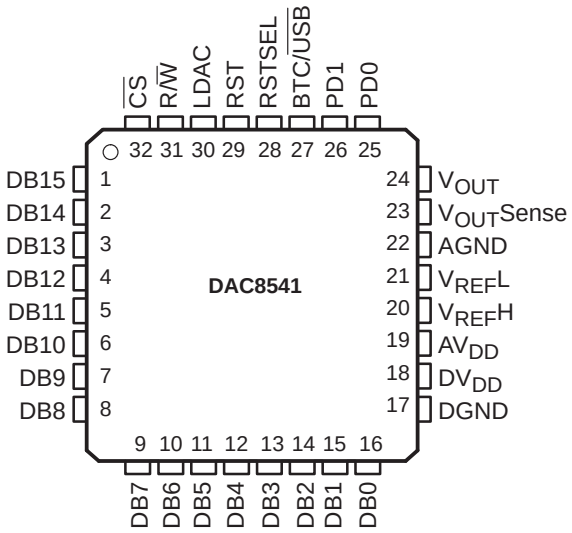
NOTES: 1. Linearity calculated using a reduced code range of 485 to 64714. Output unloaded.
2. Assured by design and characterization, not production tested.
3. Specification for code changes at each N x 4096 code boundary.

electrical characteristics, DV_{DD} = 1.8 V to 5.5 V; AV_{DD} = 2.7 V to 5.5 V; R_L = 2 kΩ to AGND; C_L = 200 pF to AGND; all specifications –40°C to 85°C (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE INPUT					
Reference current	AV_{DD} = $V_{REF}H$ = 5 V, $V_{REF}L$ = AGND		50	75	µA
	AV_{DD} = $V_{REF}H$ = 3.6 V, $V_{REF}L$ = AGND		35	60	
$V_{REF}H$ input range	$V_{REF}H > V_{REF}L$	0		AV_{DD}	V
$V_{REF}L$ input range		−100	AGND	100	mV
Reference input impedance			100		kΩ
LOGIC INPUTS (see Note 2)					
Input current				±1	µA
$V_{IN}L$, input low voltage	DV_{DD} = 1.8 V to 5.5 V			0.3×DV_{DD}	V
$V_{IN}H$, input high voltage	DV_{DD} = 1.8 V to 5.5 V	0.7×DV_{DD}			V
Pin input capacitance				3	pF
POWER REQUIREMENTS					
DV_{DD}		1.8		5.5	V
DI_{DD}	DAC active and excluding load current, V_{IH} = DV_{DD} and V_{IL} = DGND		0.2	1.0	µA
AV_{DD}		2.7		5.5	V
AI_{DD} (normal operation)	DAC active and excluding load current, V_{IH} = DV_{DD} and V_{IL} = DGND				µA
AV_{DD} = 3.6 V to 5.5 V			250	400	
AV_{DD} = 2.7 V to 3.6 V			240	390	
AI_{DD} (all power-down modes)	V_{IH} = DV_{DD} and V_{IL} = DGND				µA
AV_{DD} = 3.6 V to 5.5 V			0.2	1	
AV_{DD} = 2.7 V to 3.6 V			0.05	1	
POWER EFFICIENCY					
I_{OUT}/AI_{DD}	$I_{(LOAD)}$ = 2 mA, AV_{DD} = +5 V		89%		

NOTE 2; Assured by design and characterization, not production tested.

PBS PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DB15−DB0	1−16	I/O	Data input/output, (pin 1-MSB: pin 16-LSB)
DGND	17	I	Digital ground
DV_{DD}	18	I	Digital supply input, 1.8 V to 5.5 V
AV_{DD}	19	I	Analog power supply input, 2.7 V to 5.5 V
$V_{REF}H$	20	I	Positive reference voltage input (referenced to AGND)
$V_{REF}L$	21	I	Negative reference voltage input (referenced to AGND), nominally $V_{REF}L$ = AGND
AGND	22	I	Analog ground
V_{OUT}Sense	23	I	Analog output sense. The feedback terminal of the output amplifier.
V_{OUT}	24	O	Analog output voltage from DAC. The output amplifier has rail-to-rail operation.
PD0	25	I	Powerdown control bit 0
PD1	26	I	Powerdown control bit 1
BTC/$\overline{USB}$	27	I	Data input format: binary twos complement or unipolar straight binary
RSTSEL	28	I	Reset V_{OUT} on active RST to min-scale (RSTSEL = 0) or mid-scale (RSTSEL = 1)
RST	29	I	V_{OUT} reset to min-scale or mid-scale, rising edge (Does not reset input register data.)
LDAC	30	I	Asynchronous load command, rising edge
R/$\overline{W}$	31	I	Read/Write control input
$\overline{CS}$	32	I	Chip select, active low

timing characteristics, DV_{DD} = 1.8 V to 5.5 V; AV_{DD} = 2.7 V to 5.5 V; R_L = 2 kΩ to AGND; C_L = 200 pF to AGND; all specifications –40°C to 85°C (unless otherwise noted)

		MIN	TYP	MAX	UNIT
t_{w1}	Pulse width: $\overline{CS}$ low for valid write	20			ns
t_{su1}	Setup time: R/$\overline{W}$ low before $\overline{CS}$ falling (see Note 4)	0			ns
t_{su2}	Setup time: data in valid before $\overline{CS}$ falling	0			ns
t_{h1}	Hold time: R/$\overline{W}$ low after $\overline{CS}$ rising (see Note 4)	10			ns
t_{h2}	Hold time: data in valid after $\overline{CS}$ rising	15			ns
t_{w2}	Pulse width: $\overline{CS}$ low for valid read	40			ns
t_{su3}	Setup time: R/$\overline{W}$ high before $\overline{CS}$ falling	30			ns
t_{d1}	Delay time: data out valid after $\overline{CS}$ falling		60	80	ns
t_{h3}	Hold time: R/$\overline{W}$ high after $\overline{CS}$ rising	10			ns
t_{h4}	Hold time: data out valid after $\overline{CS}$ rising	5		20	ns
t_{su4}	Setup time: LDAC rising after $\overline{CS}$ falling (see Note 4)	10			ns
t_{d2}	Delay time: $\overline{CS}$ low after LDAC rising	50			ns
t_{w3}	Pulse width: LDAC low	40			ns
t_{w4}	Pulse width: LDAC high	40			ns
t_{w5}	Pulse width: $\overline{CS}$ high (see Note 4)	80			ns
t_{su5}	Setup time: RSTSEL valid before RST rising	0			ns
t_{h5}	Hold time: RSTSEL valid after RST rising	20			ns
t_{w6}	Pulse width: RST low	40			ns
t_{w7}	Pulse width: RST high	40			ns
t_S	V_{OUT} Settling time (settling time for a full scale code change)			10	µs

NOTE 4: Simplified operation: $\overline{CS}$ and W/$\overline{R}$ can be tied low if the DAC8541 is the only device on the bus and *Read* operation is not needed. In this case, LDAC is still required to update the output of the DAC and $t_{su(4)}$ is from *Data In Valid* to *LDAC Rising*.

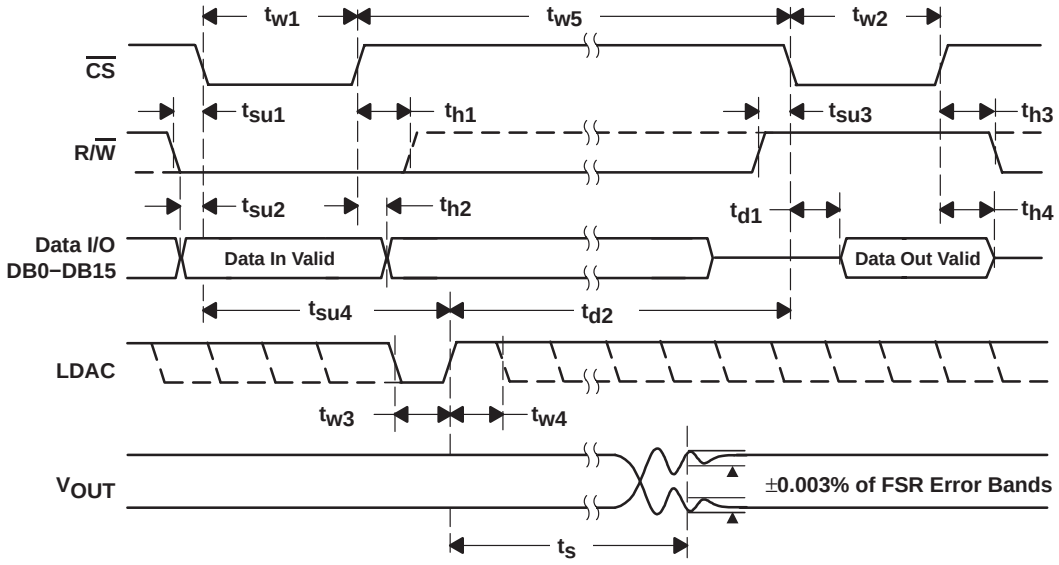


Figure 1. Data Read/Write Timing

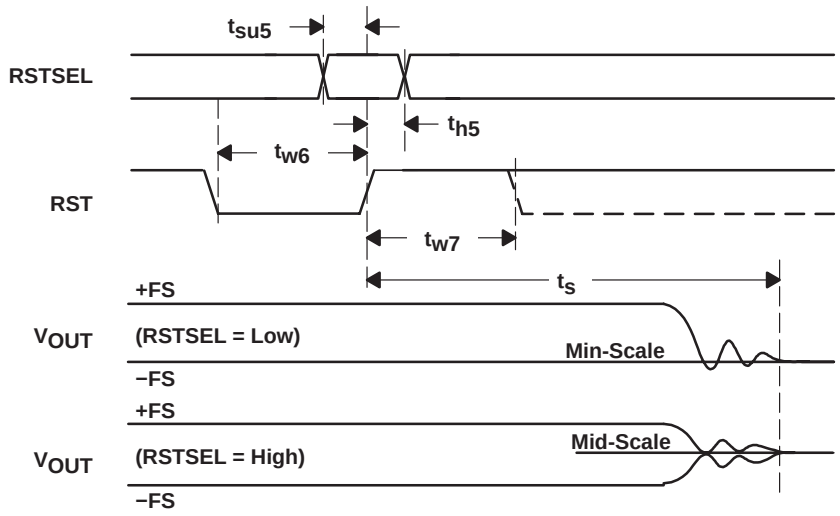


Figure 2. Reset Timing

TYPICAL CHARACTERISTICS

This condition applies to all typical characteristics: $V_{REF}H = AV_{DD}$, $V_{REF}L$ = AGND, T_A = 25°C (unless otherwise noted)

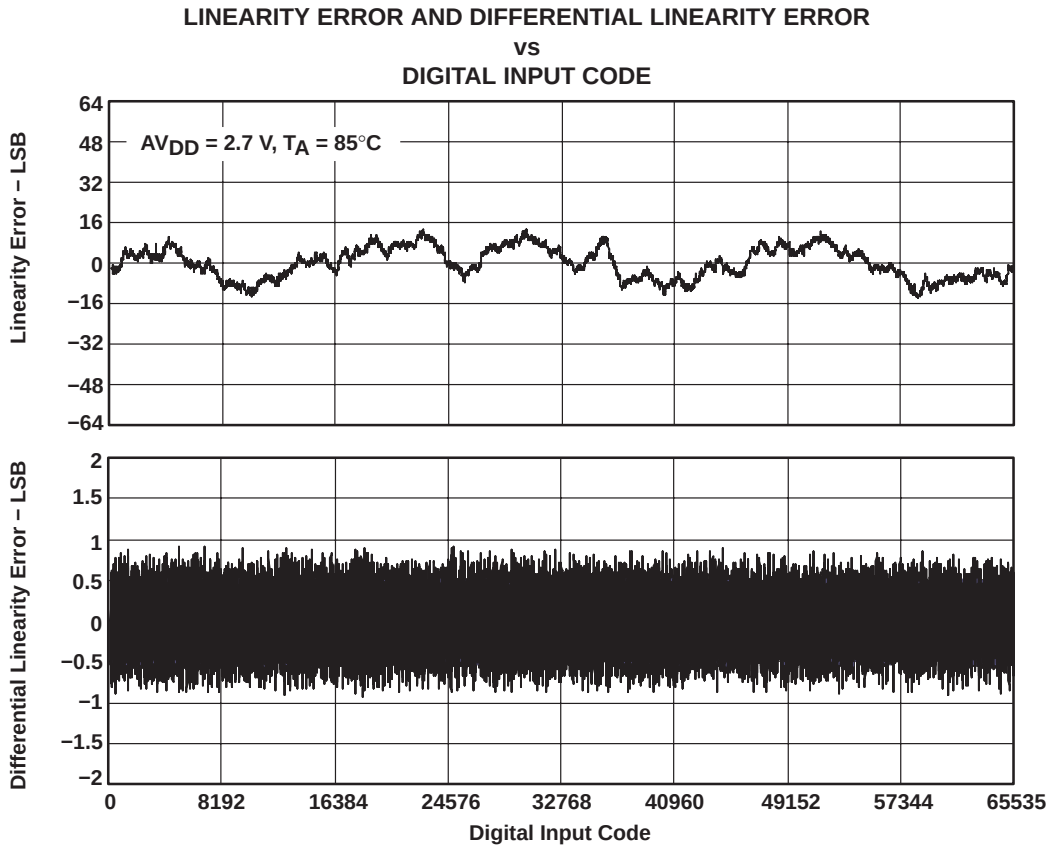


Figure 3

TYPICAL CHARACTERISTICS

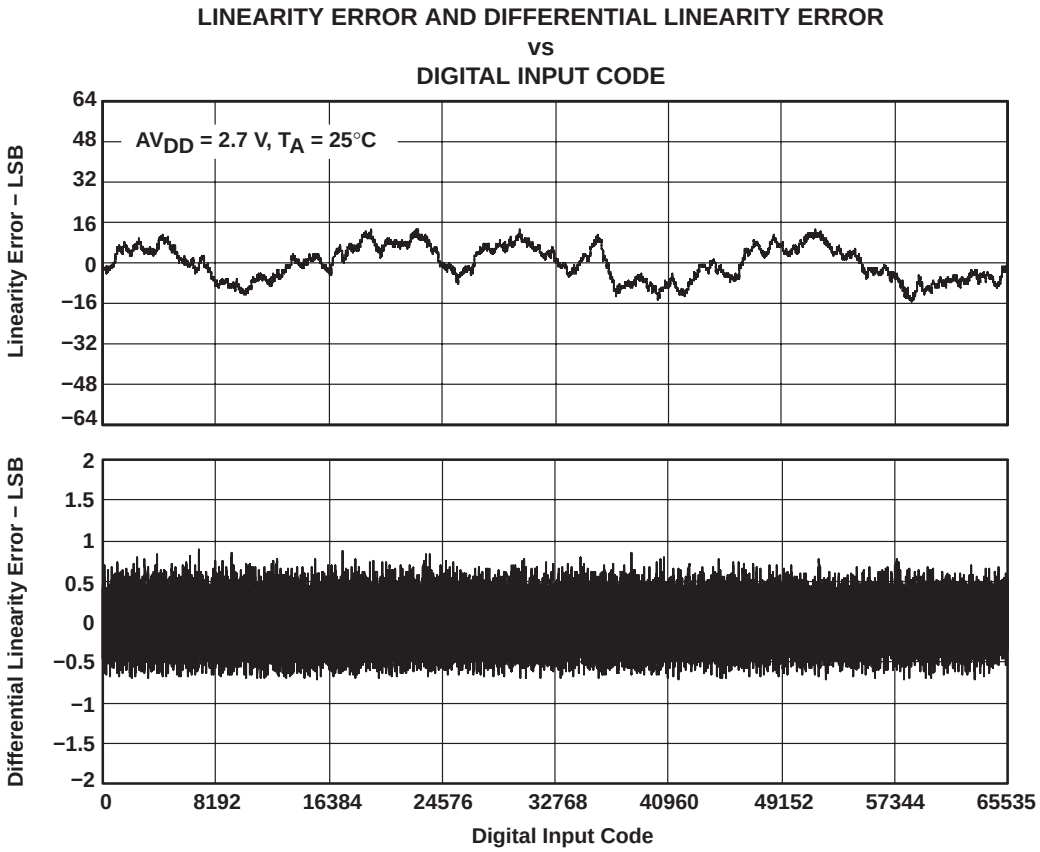


Figure 4

TYPICAL CHARACTERISTICS

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

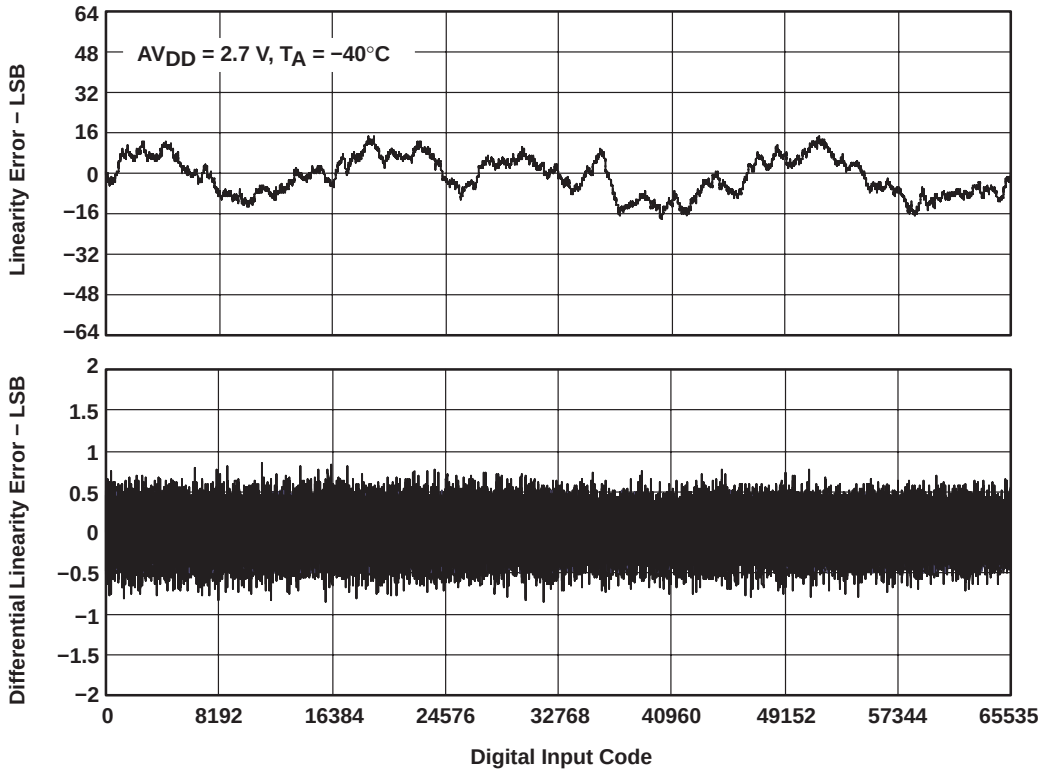


Figure 5

TYPICAL CHARACTERISTICS

ZERO-SCALE ERROR vs FREE-AIR TEMPERATURE

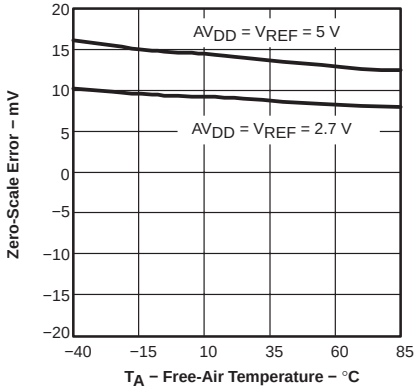


Figure 6

FULL-SCALE ERROR vs FREE-AIR TEMPERATURE

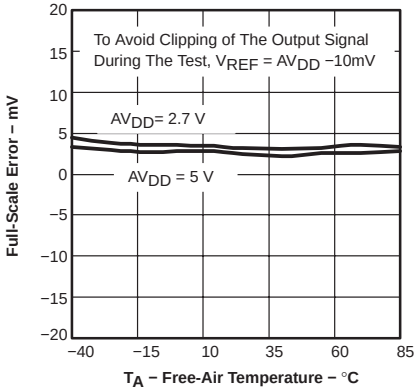


Figure 7

OUTPUT VOLTAGE vs DRIVE CURRENT CAPABILITY

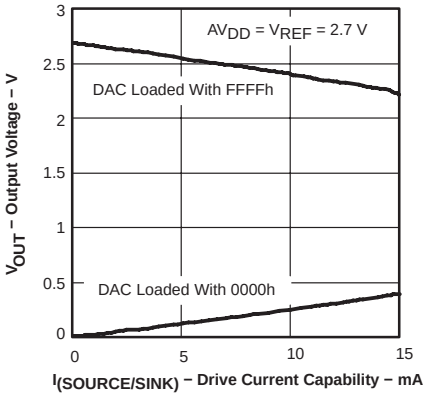


Figure 8

OUTPUT VOLTAGE vs DRIVE CURRENT CAPABILITY

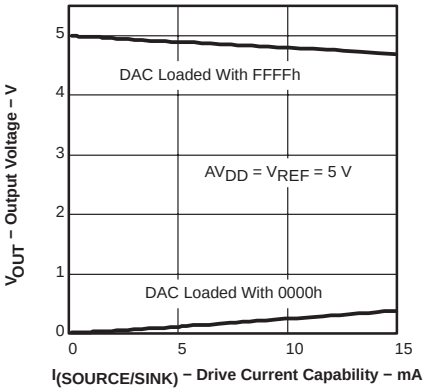


Figure 9

ANALOG SUPPLY CURRENT vs ANALOG SUPPLY VOLTAGE

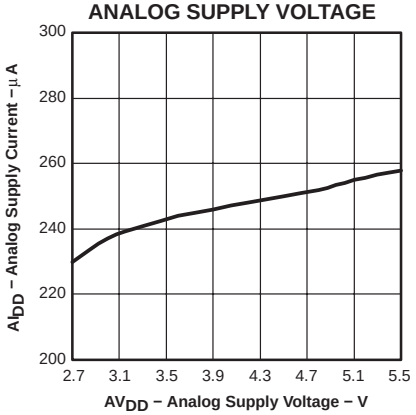


Figure 10

AIDD HISTOGRAM

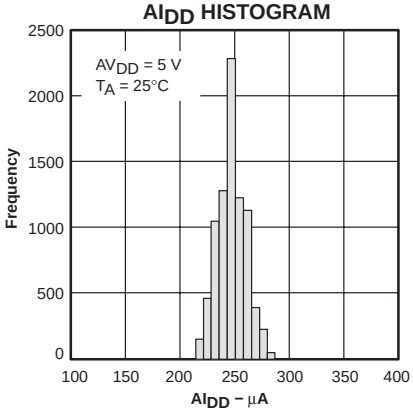


Figure 11

TYPICAL CHARACTERISTICS

AI_{DD} HISTOGRAM

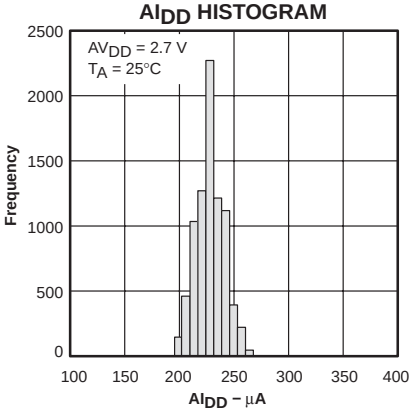


Figure 12

ANALOG SUPPLY CURRENT vs DIGITAL INPUT CODE

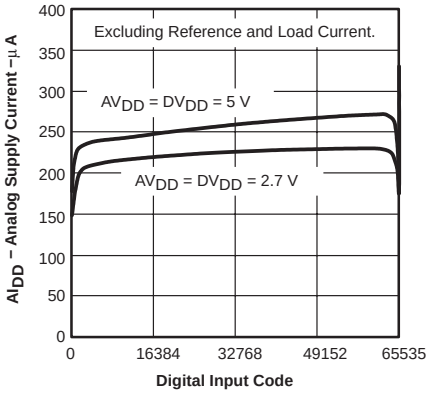


Figure 13

ANALOG SUPPLY CURRENT vs FREE-AIR TEMPERATURE

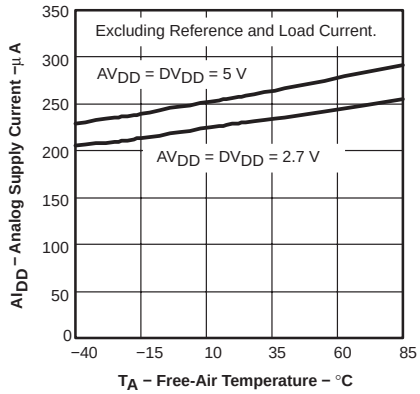


Figure 14

POWER-DOWN CURRENT vs SUPPLY VOLTAGE

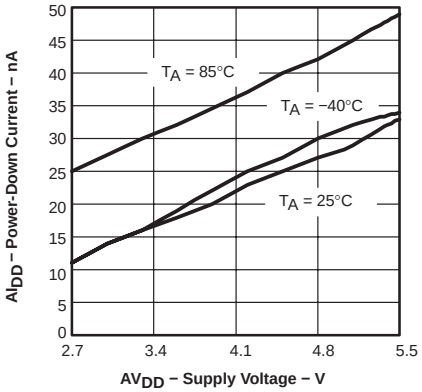


Figure 15

DIGITAL SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

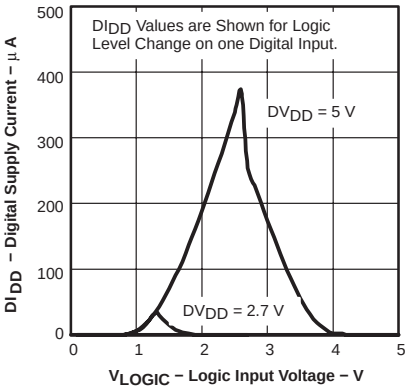


Figure 16

POWER-ON RESET TO 0 V

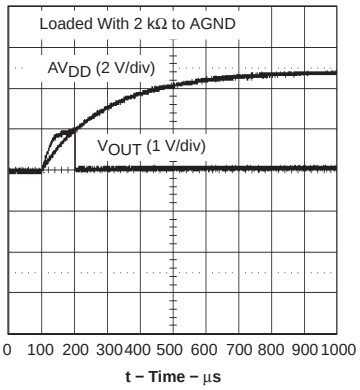


Figure 17

TYPICAL CHARACTERISTICS

EXITING POWER-DOWN

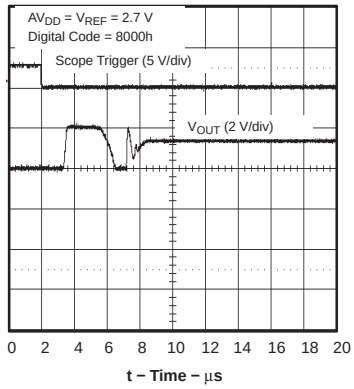


Figure 18

MAJOR CARRY CODE CHANGE GLITCH

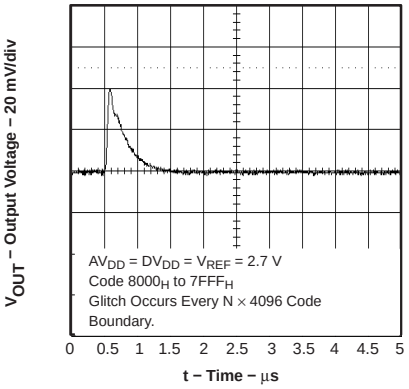


Figure 19

MAJOR CARRY CODE CHANGE GLITCH

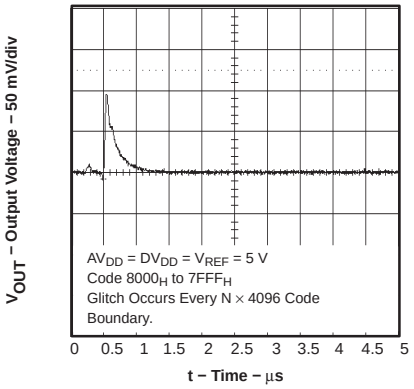


Figure 20

FULL-SCALE SETTLING TIME

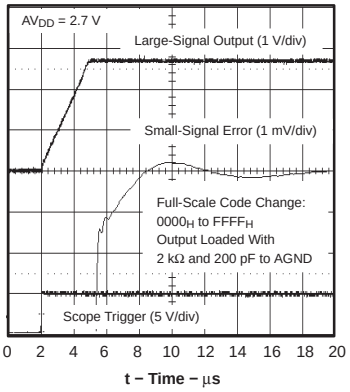


Figure 21

FULL-SCALE SETTLING TIME

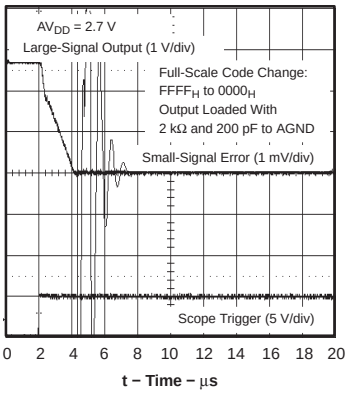


Figure 22

HALF-SCALE SETTLING TIME

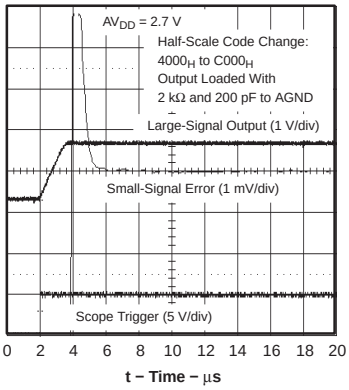


Figure 23

TYPICAL CHARACTERISTICS

HALF-SCALE SETTLING TIME

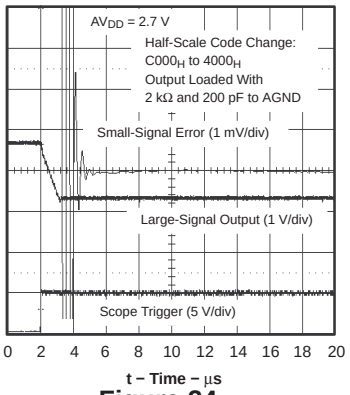


Figure 24

FULL-SCALE SETTLING TIME

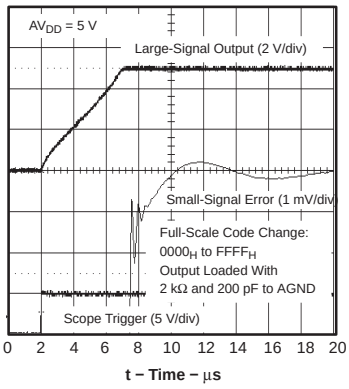


Figure 25

FULL-SCALE SETTLING TIME

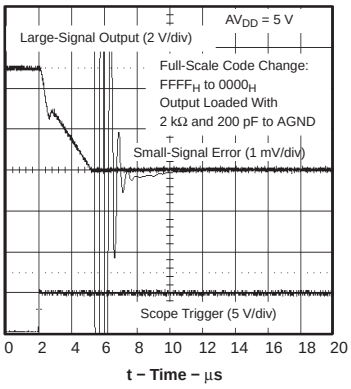


Figure 26

HALF-SCALE SETTLING TIME

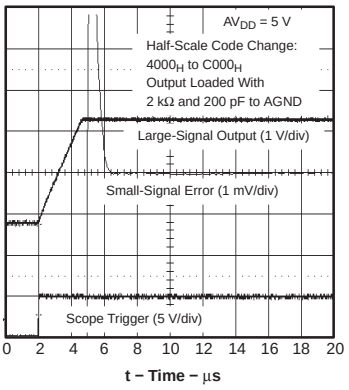


Figure 27

HALF-SCALE SETTLING TIME

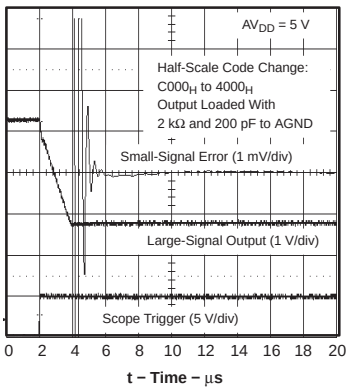


Figure 28

THEORY OF OPERATION

D/A section

The architecture of the DAC8541 consists of a string DAC followed by an output buffer amplifier. Figure 29 shows a generalized block diagram of the DAC architecture.

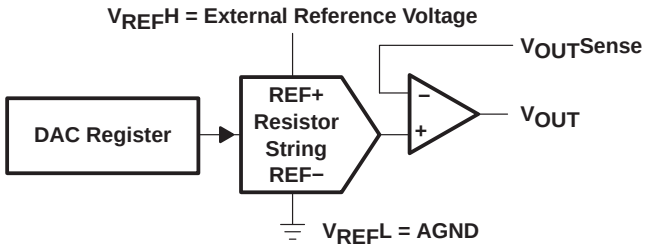


Figure 29. Generalized DAC Architecture

The input coding to the DAC8541 is set by the BTC/$\overline{\text{USB}}$ input to the device. When this input is high, the input code is binary 2s complement. If the input is low, the format is unipolar straight binary, in which case the ideal output voltage is given by:

$$V_{OUT} = V_{REF}H \times \frac{D}{65536}$$

Where D = the decimal equivalent of the binary code that is loaded to the DAC register, which can range from 0 to 65535 and $V_{REF}L$ = AGND.

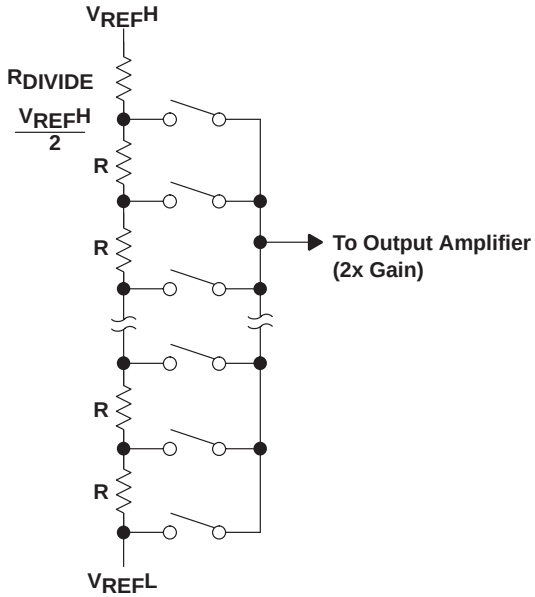


Figure 30. Typical Resistor String

THEORY OF OPERATION

resistor string

The resistor string section is shown in Figure 30. It is simply a string of resistors, each of which has a value of R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off. This voltage is then presented to the output amplifier by closing one of the switches connecting the string to the amplifier. The negative tap of the resistor string, $V_{REF}L$, can be tied to AGND or a small voltage can be applied in order to make minor adjustments to the offset seen at the V_{OUT} pin. (This is discussed in more detail in the *voltage reference inputs* section.)

output amplifier

The output buffer amplifier is capable of generating near rail-to-rail voltages on its output, which gives an output range of 0 V to AV_{DD} (offset and gain errors affect the absolute V_{OUT} range). It is also capable of driving a load of 2 kΩ in parallel with 1000 pF to AGND while remaining stable. The source and sink capabilities of the output amplifier can be seen in the typical curves. The slew rate of the DAC8541 is typically 1 V/μs with a typical full-scale settling time of 8 μs.

For additional functionality, the inverting input of the output amplifier is brought out via the V_{OUT}Sense pin. This allows for better accuracy in critical applications by tying the V_{OUT}Sense and V_{OUT} together directly at the load. Other signal conditioning circuitry may also be connected between these points for specific applications.

parallel interface

The DAC8541 provides a 16-bit parallel interface and supports both writing to and reading from the DAC input register. (See the *timing characteristics* section for detailed information for a typical write or read command.)

In addition to the data, $\overline{CS}$, and R/$\overline{W}$ inputs, the DAC8541's interface also provides powerdown, LDAC, data format, and reset/reset-select control. Tables 1 and 2 show the control signal actions and data format, respectively. These features are discussed in more detail in the remaining sections.

Table 1. DAC8541 CONTROL SIGNAL SUMMARY

$\overline{CS}$	R/$\overline{W}$	BTC/$\overline{USB}$	LDAC	RST	RSTSEL	PD1	PD0	ACTION
H	X	X	X	X	X	X	X	Device data I/O is disabled on the bus.†
↓	L	X	X	H,L	X	L	L	Write initiated, present input data to the bus.
↓	H	X	X	H,L	X	L	L	Read initiated, data from input register is presented to data bus.
↑	X	X	X	H,L	X	L	L	Input data is latched when writing to the device.
X	X	X	↑	H,L	X	L	L	Data from input register is transferred to DAC register and V_{OUT} is updated.
X	X	L	X	X	X	X	X	Input/output data format is unipolar straight binary.
X	X	H	X	X	X	X	X	Input/output data format is binary 2s complement.
X	X	X	X	↑	L	L	L	DAC register and V_{OUT} reset to min-scale. (If DAC is powered down during reset, DAC register resets and V_{OUT} will settle to min-scale upon power up.)
X	X	X	X	↑	H	L	L	DAC register and V_{OUT} reset to mid-scale. (If DAC is powered down during reset, DAC register resets and V_{OUT} will settle to mid-scale upon power up.)
X	X	X	X	X	X	L	H	Powerdown device, V_{OUT} impedance equals 1 kΩ to AGND
X	X	X	X	X	X	H	L	Powerdown device, V_{OUT} impedance equals 100 kΩ to AGND
X	X	X	X	X	X	H	H	Powerdown device, V_{OUT} impedance equals high impedance

† Only disables 16-bit data I/O interface. Other control lines remain active.

THEORY OF OPERATION

data format

Table 2 details the input data format of the DAC8541. Two data I/O formats are available to the host interface. These two formats are binary 2s complement (BTC) and unipolar straight binary (USB). The BTC/$\overline{\text{USB}}$ input pin controls the format used by the DAC. The data format selected by the BTC/$\overline{\text{USB}}$ input is used for data written into the device as well as data that is read back from the DAC8541. (Refer to Table 1 and Figure 1 for additional information for performing read and write operations.)

Table 2. DAC8541 Data Format

BTC/$\overline{\text{USB}}$ = 0		BTC/$\overline{\text{USB}}$ = 1	
UNIPOLAR STRAIGHT BINARY		BINARY 2s COMPLEMENT	
DIGITAL INPUT	ANALOG OUTPUT	DIGITAL INPUT	ANALOG OUTPUT
0x0000h	Min-scale	0x8000h	Min-scale
0x0001h	Min-scale + 1 LSB	0x8001h	Min-scale + 1 LSB
• •	• •	• •	• •
0x8000h	Mid-scale	0x0000h	Mid-scale
0x8001h	Mid-scale + 1 LSB	0x0001h	Mid-scale + 1 LSB
• •	• •	• •	• •
0xFFFFh	Full Scale	0x7FFFh	Full Scale

LDAC function

The DAC8541 is designed using a double-buffered architecture. A write command transfers data from the data input pins into the input register. The data is held in the input register until a rising edge is detected on the LDAC input. This rising edge signal transfers the data from the input register to the DAC register. Upon issuance of the rising LDAC edge, the output of the DAC8541 begins settling to the newly written data value presented to the DAC register.(Data in the input register is not changed when an LDAC command is given.)

RST and RSTSEL

The RST and RSTSEL inputs control the reset of the DAC register and consequently, the DAC output. The reset command is edge triggered by a low-to-high transition on the RST pin. Once a rising edge on RST is detected, the DAC output may settle to the mid-scale or min-scale code depending on the state of the RSTSEL input. A logic high value on RSTSEL causes the DAC output to reset to mid-scale and a logic low value resets the DAC to min-scale. Application of a valid reset signal to the DAC does not overwrite existing data in the input register.

power-on reset

The DAC8541 contains a power-on reset circuit that controls the output voltage during power up. On power up, the DAC register (and DAC output) is set to min-scale (plus a small offset error produced by the output buffer). It remains at min-scale until a valid write sequence is made to the DAC changing the DAC register data. This is useful in applications where it is important to know the state of the output of the DAC while the system is in the process of powering up. DGND must be applied to all digital inputs until the digital and analog supplies are applied to the DAC8541. Logic voltages applied to the input pins when power is not applied to DV_{DD} and AV_{DD}, may power the device through the ESD input structures causing undesired operation.

THEORY OF OPERATION

power-down modes

The DAC8541 utilizes four modes of operation. These modes are programmable via two inputs (PD1 and PD0) to the device. Table 3 shows how the state of these pins correspond to the mode of operation of the DAC8541.

Table 3. Modes of Operation for the DAC8541

PD1	PD0	OPERATING MODE
0	0	Normal operation
POWER-DOWN MODES		
0	1	1 kΩ to AGND
1	0	100 kΩ to AGND
1	1	High impedance

When both pins are set to 0, the device works normally with its typical power consumption of 250 μA at AV_{DD} = 5 V. However, for the three power-down modes, the supply current falls to 200 nA at AV_{DD} = 5 V (50 nA at AV_{DD} = 3 V). Not only does the supply current fall, but the V_{OUT} terminal is internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the device is known while in power-down mode. There are three different options: The output is connected internally to AGND through a 1-kΩ resistor, it is connected to AGND through a 100-kΩ resistor, or it is left open-circuited (high impedance). The output stage is illustrated in Figure 31.

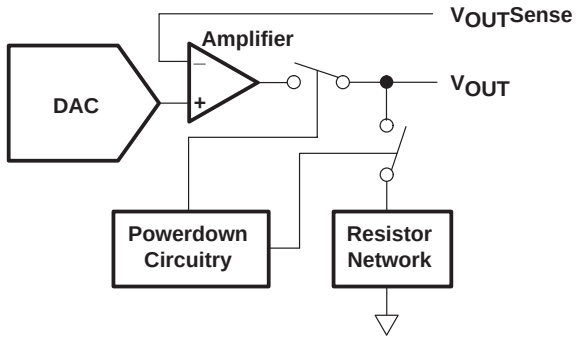


Figure 31. Output Stage During Power Down (High-Impedance)

All analog circuitry is shut down when a power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. This allows the DAC's output voltage to return to the previous level when power-up resumes. The delay time required to exit power-down is typically 2.5 μs for AV_{DD} = 5 V and 5 μs for AV_{DD} = 3 V. (See the *typical curves* section for additional information.)

voltage reference inputs

Two voltage inputs provide the reference set points for the DAC architecture. These are $V_{REF}H$ and $V_{REF}L$. For typical rail-to-rail operation, $V_{REF}H$ should be equivalent to AV_{DD} and $V_{REF}L$ tied to AGND. The output voltage is given by:

$$V_{OUT} = V_{REF}H - 2 \times V_{REF}L$$

The use of the $V_{REF}L$ input allows minor adjustments to be made to the offset of the DAC output by applying a small voltage to the $V_{REF}L$ input. The acceptable range is between −100 mV and 100 mV with respect to AGND. A low output impedance source is needed, so that the accuracy of the DAC over its operating range is not affected.

THEORY OF OPERATION

analog and digital supplies

The DAC8541 utilizes two separate supplies for operation. The analog supply (AV_{DD}) powers the output buffer and DAC while the digital supply (DV_{DD}) sets the I/O voltage thresholds. Refer to the device specification table for additional information. AV_{DD} can operate from 2.7 V to 5.5 V while DV_{DD} can independently function from 1.8 V to 5.5 V. The control and data I/O thresholds are determined by DV_{DD} and are given in the *electrical characteristics section.*

APPLICATION INFORMATION

host processor interfacing

DAC8541 to MSP430 microcontroller

Figure 32 shows a typical parallel interface connection between the DAC8541 and a MSP430 microcontroller. The setup for the interface shown uses ports 4 and 5 of the MSP430 to send or receive the 16-bit data while bits 0−7 of port 2 provides the control signals for the DAC. When data is to be transmitted to the DAC8541, the data is made available to the DAC via P4 and P5 and P2.1 is taken low. The MSP430 then toggles P2.0 from high-to-low and back to high, transferring the 16-bit data to the DAC. This data is loaded into the DAC register by applying a rising edge to P2.4. The remaining five I/O signals of P2 shown in the figure control the reset, power-down, and data format functions of the DAC. Depending on the specific requirements of a given application, these pins may be tied to DGND or DV_{DD}, enabling the desired mode of operation.

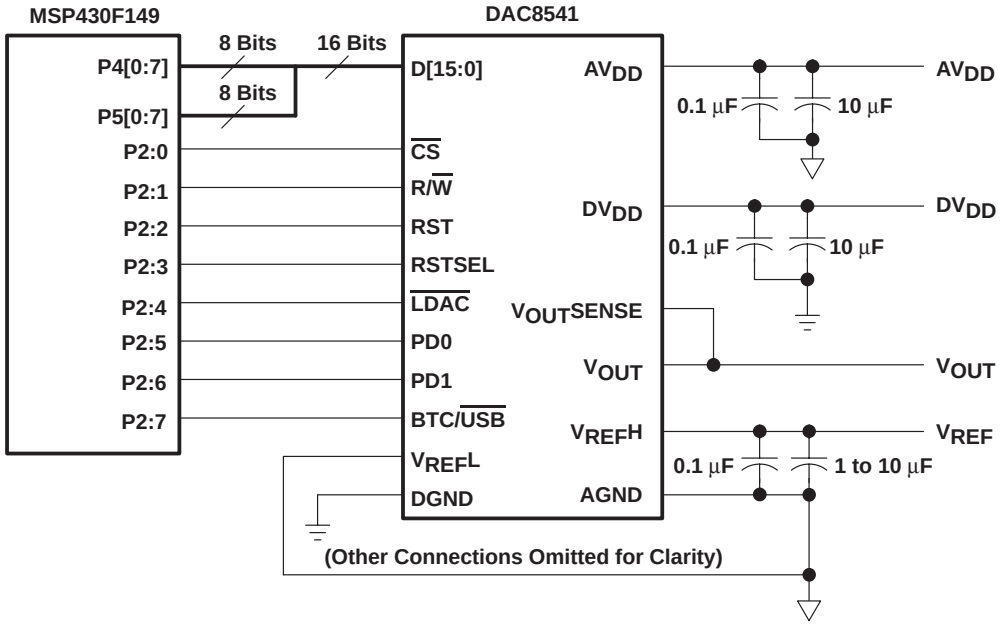


Figure 32. DAC8541 to MSP430 Microcontroller

DAC8541 to TMS320C5402 DSP

Figure 33 shows the connections between the DAC8541 and the TMS320C5402 digital signal processor. Data is provided via the parallel data bus of the DSP while the DAC's $\overline{CS}$ control input is derived from the decoded I/O strobe signal. The $\overline{IOSTRB}$ in addition to the R/$\overline{W}$ and XF(I/O) signals control the data transmission to and from the DAC as well as the $\overline{LDAC}$ control. With additional decoding, multiple DAC8541's can be connected to the same parallel data bus of the DSP.

APPLICATION INFORMATION

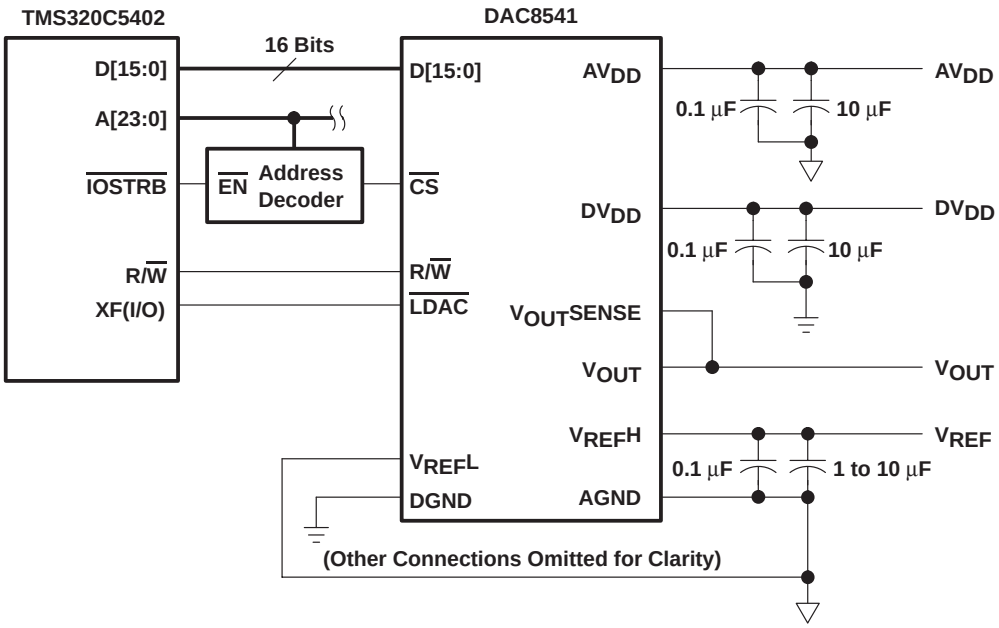


Figure 33. DAC8541 to TMS320 DSP

bipolar operation using the DAC8541

The DAC8541 has been designed for single-supply operation but a bipolar output range is also possible using the circuit shown in Figure 34. The circuit allows the DAC8541 to achieve an analog output range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an OPA703 as the output amplifier.

Setting BTC/$\overline{USB}$ = 1, sets the DAC into binary 2s complement I/O format for the bipolar V_{OUT} configuration. When operated with BTC/$\overline{USB}$ set high, the output voltage for any input code can be calculated as follows:

$$V_{OUT} = \left[V_{REF}H \times \left(\frac{D}{65536} \right) \times \left(\frac{R1 + R2}{R1} \right) - V_{REF}H \times \left(\frac{R2}{R1} \right) \right]$$

where D represents the input code in decimal, unipolar straight binary (0–65535) and $V_{REF}L$ = AGND.

With $V_{REF}H$ = 5 V, $R_1 = R_2$ = 10 kΩ:

$$V_{OUT} = \left(\frac{10 \times D}{65536} \right) - 5\ V$$

This is an output voltage range of ±5 V with 8000h corresponding to a –5 V output and 7FFFh corresponding to a 5 V output. Bipolar zero is given by 0000h applied to the DAC.

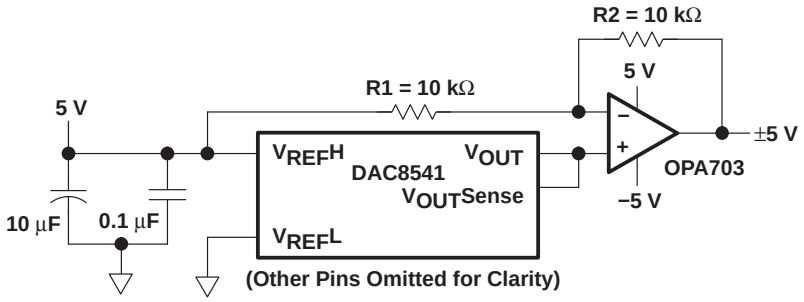


Figure 34. Bipolar Operation With the DAC8541

APPLICATION INFORMATION

layout

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies. The following measures should be taken to assure optimum performance of the DAC8541.

The DAC8541 offers dual-supply operation, as it can often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more important it becomes to separate the analog and digital ground and supply planes at the DAC.

Because the DAC8541 has both analog and digital ground pins, return currents can be better controlled and have less effect on the DAC's output error. Ideally, AGND would be connected directly to an analog ground plane and DGND to the digital ground plane. The analog ground plane would be separate from the ground connection for the digital components until they were connected at the power entry point of the system.

The power applied to AV_{DD} and $V_{REF}H$ (this also applies to $V_{REF}L$ if not tied to AGND) should be well-regulated and low-noise. Switching power supplies and dc/dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the AGND connection, AV_{DD} should be connected to a 5-V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. In addition, the 1-µF to 10-µF and 0.1-µF bypass capacitors are strongly recommended. In some situations, additional bypassing may be required, such as a 100-µF electrolytic capacitor or even a *Pi* filter made up of inductors and capacitors—all designed to essentially lowpass filter the AV_{DD} supply, removing the high frequency noise.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC8541Y/250	ACTIVE	TQFP	PBS	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	8541Y	Samples
DAC8541Y/250G4	ACTIVE	TQFP	PBS	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	8541Y	Samples
DAC8541Y/2K	ACTIVE	TQFP	PBS	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	8541Y	Samples

(1) The marketing status values are defined as follows:
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OBSOLETE: TI has discontinued the production of the device.

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(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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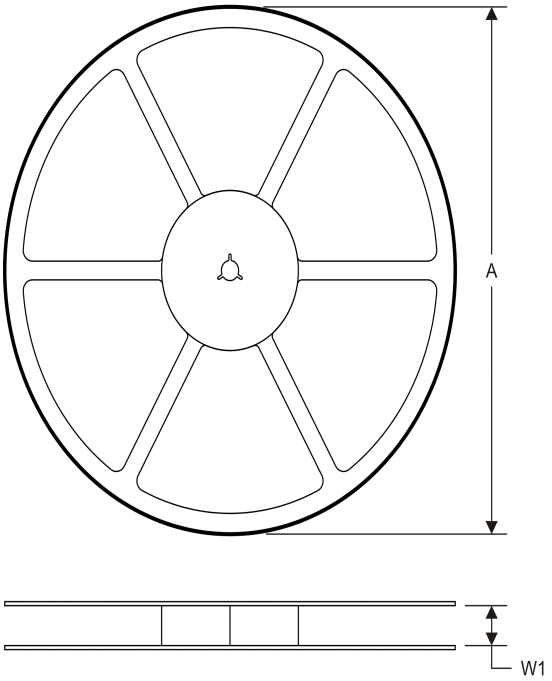
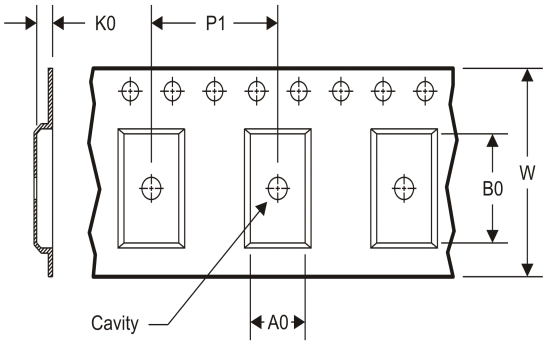
REEL DIMENSIONS



TAPE DIMENSIONS



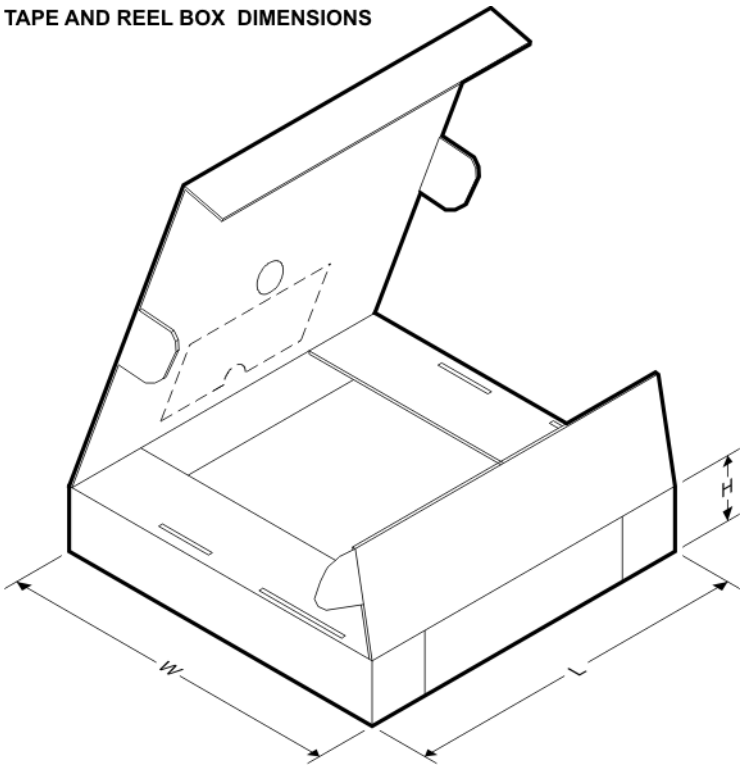
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8541Y/250	TQFP	PBS	32	250	330.0	16.4	7.2	7.2	1.5	12.0	16.0	Q2
DAC8541Y/2K	TQFP	PBS	32	2000	330.0	16.4	7.2	7.2	1.5	12.0	16.0	Q2

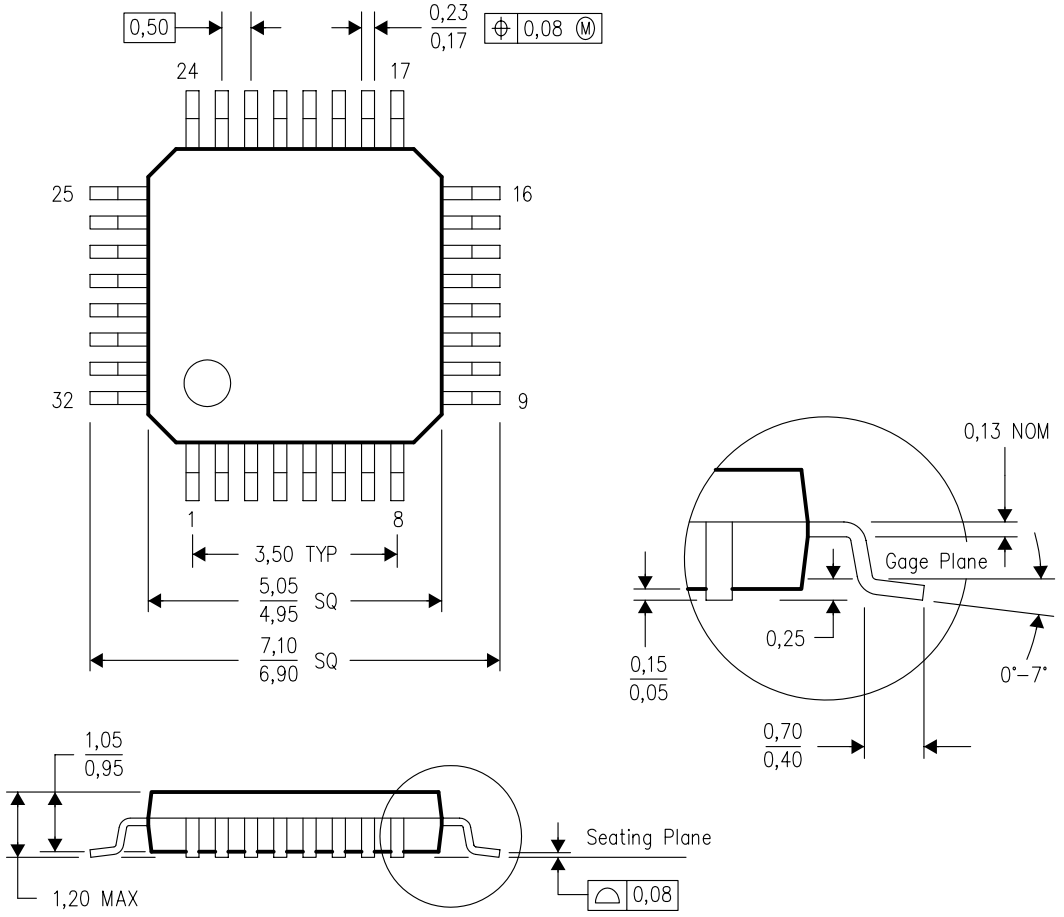
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8541Y/250	TQFP	PBS	32	250	367.0	367.0	38.0
DAC8541Y/2K	TQFP	PBS	32	2000	367.0	367.0	38.0

PBS (S–PQFP–G32) PLASTIC QUAD FLATPACK



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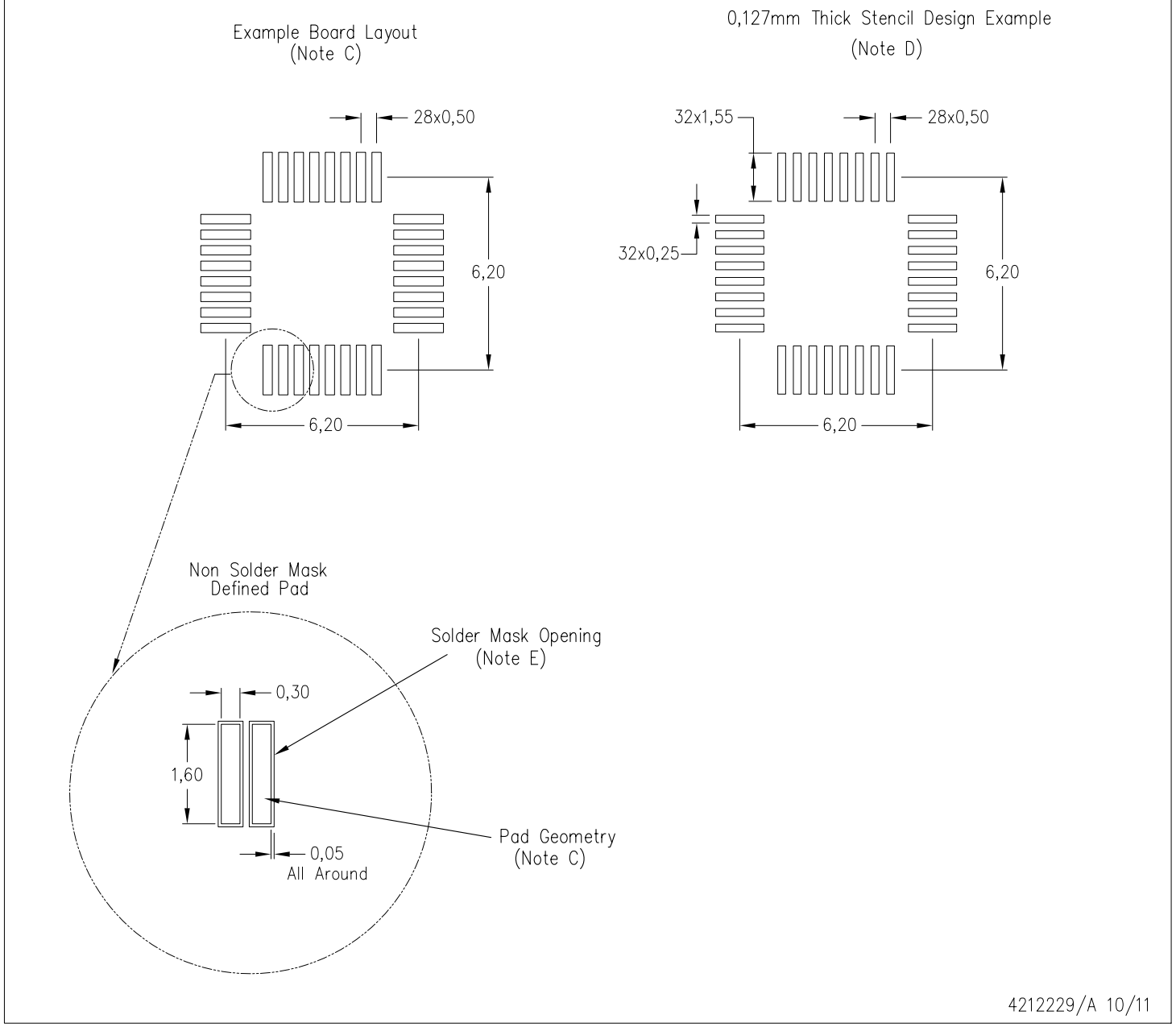
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

PBS (S–PQFP–G32) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
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C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances between and around signal pads.

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