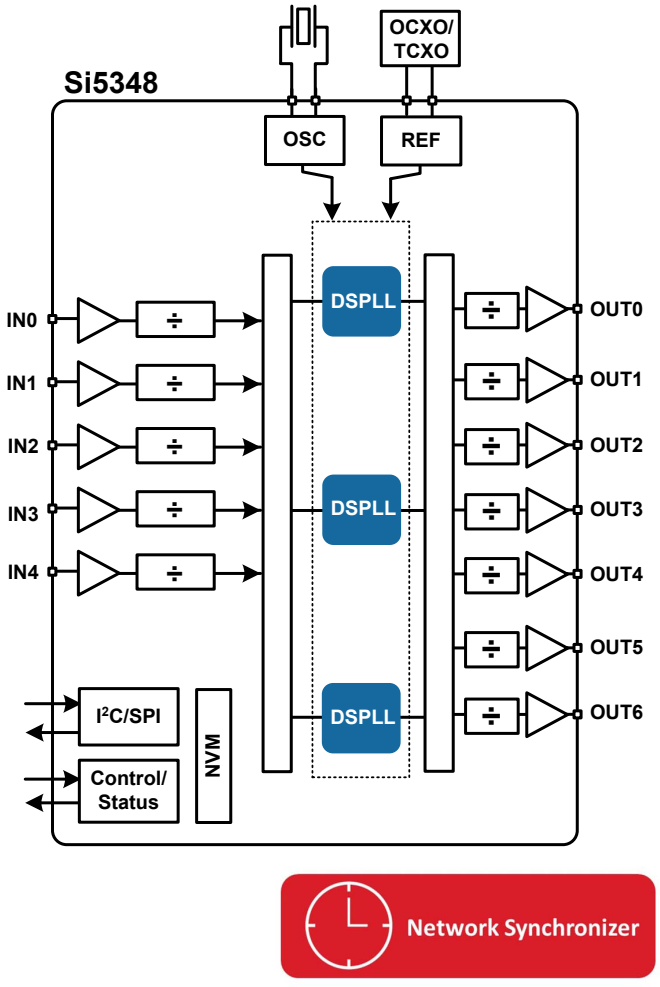
Si5348 Network Synchronizer Clock Data Short

SyncE/1588 and Stratum 3/3E Compliant Network Synchronizer Clock

The Si5348 combines the industry's smallest footprint and lowest power network synchronizer clock with unmatched frequency synthesis flexibility and ultra-low jitter. The Si5348 is ideally suited for wireless backhaul, IP radio, small and macro cell wireless communications systems, and data center switches requiring both traditional and/or packet based network synchronization. The three independent DSPLLs are individually configurable as a SyncE PLL, IEEE 1588 DCO or a general-purpose PLL for processor or FPGA clocking. The Si5348 can also be used in legacy SETS systems needing Stratum 3/3E compliance. The optional digitally controlled oscillator (DCO) mode provides precise timing adjustments to 1 ppt for 1588 (PTP) clock steering applications. The Si5348's unique design allows the TCXO/OCXO to be any value up to 250 MHz, simplifying vendor selection and qualification. The Si5348 is programmable via a serial interface with in-circuit programmable non-volatile memory so it always powers up into a known configuration. Programming the Si5348 is easy with ClockBuilder Pro software. Factory pre-programmed devices are also available.

Key Features

- Three independent DSPLLs in a single monolithic IC supporting flexible SyncE/IEEE 1588 and SETS architectures
- Meets the requirements of:
  - ITU-T G.8273.2 T-BC
  - ITU-T G.8262 (SyncE) EEC Options 1 & 2
  - ITU-T G.812 Type III, IV
  - ITU-T G.813 Option 1
  - Telcordia GR-1244, GR-253 (Stratum-3/3E)
- Each DSPLL generates any output frequency from any input frequency
- Input frequency range:
  - External crystal: 48-54 MHz
  - REF clock: 5-250 MHz
  - Diff clock: 8 kHz-750 MHz
  - LVCMOS clock: 8 kHz-250 MHz
- Output frequency range:
  - Differential: up to 712.5 MHz
  - LVCMOS: up to 250 MHz
- Pin or software controllable DCO on each DSPLL w/ typical resolution down to 1 ppt/step
- Excellent jitter performance: <130 fs typ (12 kHz-20 MHz)
- Programmable loop bandwidth per DSPLL: 1 mHz to 4 kHz
- Highly configurable output drivers: LVDS, LVPECL, LVCMOS, HCSL, CML
- Status monitoring: LOS, OOF, LOL
- Serial interface: I2C or SPI (3-wire or 4-wire)
- 5 input, 7 output, 64 pin QFN
- Temperature range: –40 to +85 °C
- Pb-free, RoHS-6 compliant



Si5348 Network Synchronizer Evaluation Tools

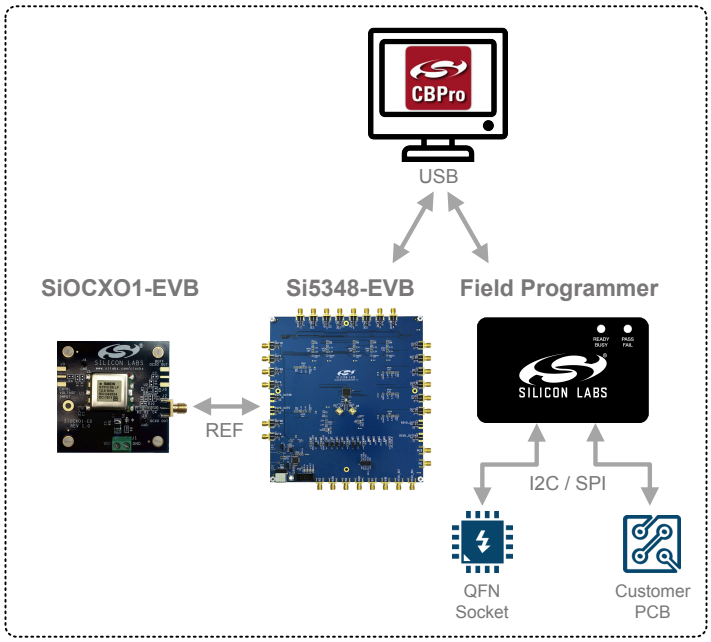
The Si5348-EVB enables customers to quickly move from device configuration to detailed performance evaluation.

Features

- Seamless configuration file download from CBPro to EVB
- SMA connectors for high quality clock evaluation
- All registers, LED indicators, and I/O are accessible
- No external clocks required: EVBs by default will free-run
- Reports power consumption, junction temperature, and over 100 design rule checks results in real time.

ClockBuilder Pro

Generating high performance clocks has never been simpler with the ClockBuilder Pro development ecosystem from Silicon Labs. ClockBuilder Pro simplifies the process of generating high performance clocks by providing resources from initial concept to the final product in a single software package. This allows developers to spend less time looking for product information and development resources and more time designing their products.



Si5348 Selector Guide

Ordering Part Number	# of DSPLLs	Output Clock Frequency Range	Package	RoHS-6, Pb-Free	Temperature Range
Si5348A-B-GM	3	1 pps to 712.5 MHz	64-Lead 9x9 QFN	Yes	–40 to 85 °C
Si5348B-B-GM		1 pps to 350 MHz			
Si5348-EVB	—	—	Evaluation Board	—	—
SiOCXO1-EVB	—	—	OCXO Reference Clock Evaluation Board for Si5348-EVB (optional).	—	—

Documentation for these products is available under NDA from Silicon Labs.

Contact your local Silicon Labs Sales Representative or Distributor for more information or to request an evaluation board.