

HTSICH56; HTSICH48

HITAG S transponder IC

Rev. 3.1 — 11 December 2014
210331

Product short data sheet
COMPANY PUBLIC

1. General description

The HITAG product line is well known and established in the contactless identification market.

Due to the open marketing strategy of NXP Semiconductors there are various manufacturers well established for both the transponders / cards as well as the Read/Write Devices. All of them supporting HITAG 1 and HITAG 2 transponder IC's. With the new HITAG S family, this existing infrastructure is extended with the next generation of IC's being substantially smaller in mechanical size, lower in cost, offering more operation distance and speed, but still being operated with the same reader infrastructure and transponder manufacturing equipment.

One Protocol - two memory options.

The protocol and command structure for HITAG S is based on HITAG 1, including anticollision algorithm.

Two different memory sizes are offered and can be operated using exactly the same protocol.

- HITAG S256 with 256 bit Total Memory Read/Write
- HITAG S2048 with 2048 bit Total Memory Read/Write

2. Features and benefits

2.1 Features

- Integrated Circuit for Contactless Identification Transponders and Cards
- Integrated resonance capacitor of 210 pF with ± 5 % tolerance over full production
- Frequency range 100 kHz to 150 kHz.

2.2 Protocol

- Modulation Read/Write Device → Transponder: 100 % ASK and Binary Pulse Length Coding
- Modulation Transponder → Read/Write Device: Strong ASK modulation with Anticollision, Manchester and Bi-phase Coding
- Fast Anticollision Protocol for inventory tracking: 100 Tags in 3.2 seconds
- Cyclic Redundancy Check (CRC)
- Optional Transponder Talks First Modes with user defined data length
- Temporary switch from Transponder Talks First into Reader Talks First Mode



- Data Rate Read/Write Device to Transponder: 5.2 kBit/s
- Data Rates Transponder to Read/Write Device: 2 kBit/s, 4 kBit/s, 8 kBit/s

2.3 Memory

- Two memory options (256 bit, 2048 bit)
- Up to 100000 erase/write cycles
- 10 years non-volatile data retention
- Secure Memory Lock functionality

2.4 Supported standards

- Full compliant to ISO 11784/85 Animal ID
- Targeted to operated on hardware infrastructure of new upcoming standards
ISO 14223 (Animal ID with anticollision and read/write functionality)
ISO 18000-2 (AIDC Techniques-RFID or Item Management)
- Supports German Waste Management Standard and Pigeon Race Standard

2.5 Security features

- 32 bit Unique Identification Number (UID)
- 48 bit secret key based encrypted authentication

2.6 Delivery types

- Sawn, gold - bumped 8" Wafer
- Sawn, gold - megabumped 8" Wafer
- Contactless Chip Card Module MOA4
- HVSON2

3. Applications

- Animal Identification
- Laundry Automation
- Beer keg and gas cylinder logistic
- Pigeon Race Sports
- Brand Protection Applications

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
Wafer EEPROM characteristics						
t_{ret}	retention time	$T_{\text{amb}} \leq 55\text{ °C}$	10	-	-	year
$N_{\text{endu(W)}}$	write endurance		100000			cycle
Interface characteristics						
C_i	input capacitance	between IN1 and IN2 HTSICxxxxxEW/x7	199	210	221	pF

[1] Typical ratings are not guaranteed. Values are at 25 °C.

[2] Measured with $Q_{\text{coil}} = 20$, $L_{\text{coil}} = 7.5\text{ mH}$, optimal tuned to resonance circuit; $V_{\text{IN1-IN2}} = 2\text{ V (RMS)}$

5. Ordering information

Table 2. Ordering information

Type number	Package	Memory size	Description	Version
	Name	Memory size	Description	Version
HTSICH5601EW/V7	Wafer	256 bit	Au-bumped die on sawn wafer, inkless	-
HTSICH4801EW/V7	Wafer	2048 bit	Au-bumped die on sawn wafer, inkless	-
HTSICC5601EW/C7	Wafer	256 bit	Au-megabumped die on sawn wafer, inkless	-
HTSICC4801EW/C7	Wafer	2048 bit	Au-megabumped die on sawn wafer, inkless	-
HTSMOH5602EV	PLLMC ^[1]	256 bit	plastic leadless module carrier package; 35 mm wide tape	SOT500-2
HTSMOH4802EV	PLLMC ^[1]	2048 bit	plastic leadless module carrier package; 35 mm wide tape	SOT500-2
HTSH5601ETK	HVSON2	256 bit	plastic thermal enhanced very thin small outline package; no leads; 2 terminals; body $3 \times 2 \times 0.85\text{ mm}$	SOT899-1
HTSH4801ETK	HVSON2	2048 bit	plastic thermal enhanced very thin small outline package; no leads; 2 terminals; body $3 \times 2 \times 0.85\text{ mm}$	SOT899-1

[1] This package is also known as MOA4

6. Block diagram

The HITAG S Transponder requires no external power supply. The contactless interface generates the power supply and the system clock via the resonant circuitry by inductive coupling to the Read/Write Device (RWD). The interface also demodulates data transmitted from the RWD to the HITAG S Transponder, and modulates the magnetic field for data transmission from the HITAG S Transponder to the RWD.

Data are stored in a non-volatile memory (EEPROM). The EEPROM has a capacity up to 2048 bit and is organized in 64 Pages consisting of 4 Bytes each (1 Page = 32 Bits).

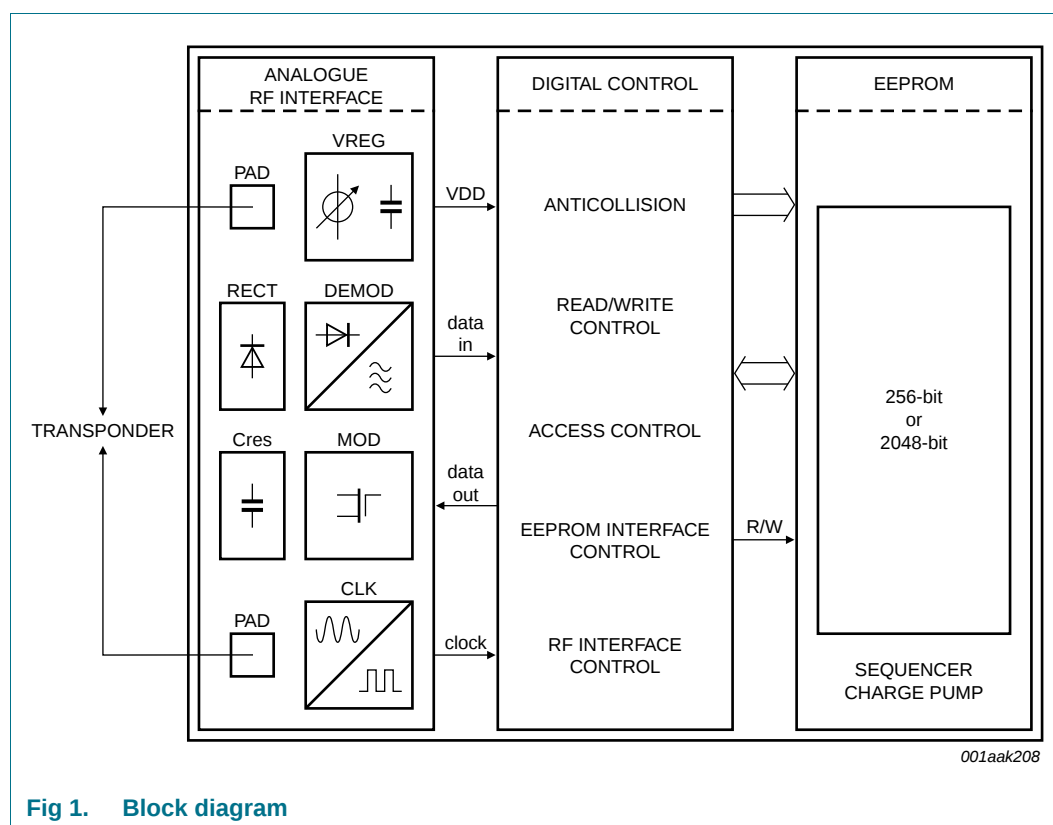


Fig 1. Block diagram

7. Functional description

7.1 Memory organization

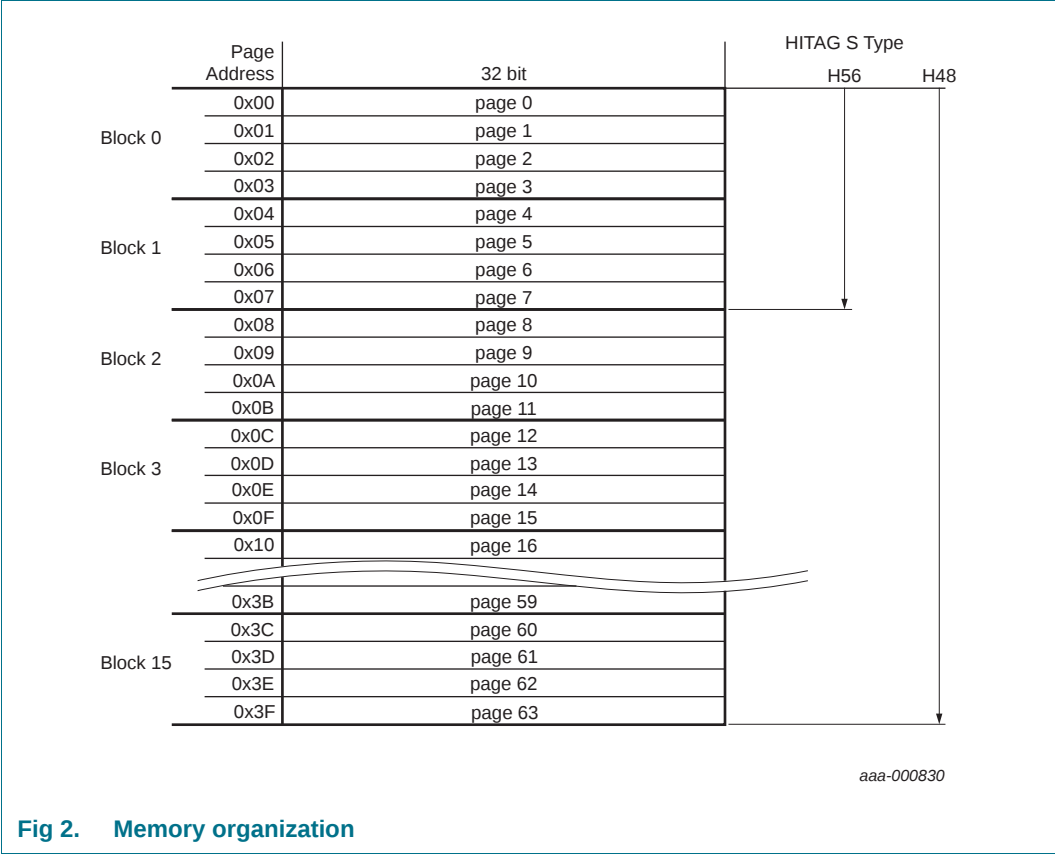


Fig 2. Memory organization

The EEPROM has a capacity up to 2048 bit and is organized in 16 Blocks, consisting of 4 Pages each, for commands with Block access. A Page consists of 4 Bytes each (1 Page = 32 Bits) and is the smallest access unit.

Addressing is done Page by Page (Page 0 to 63) and access is gained either Page by Page or Block by Block entering the respective Page start address. In case of Block Read/Write access, the transponder is processed from the start Page address within one block to the end of the corresponding block.

Two different types of HITAG S IC's with different memory sizes as shown in the figure above are available.

7.2 HITAG S plain mode

Table 3. Memory map for HITAG S in plain mode

page address	MSByte						LSByte	
	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB
0x00	UID3		UID2		UID1		UID0	
0x01	Reserved		CON2		CON1		CON0	
0x02	Data 3		Data 2		Data 1		Data 0	
0x03	Data 3		Data 2		Data 1		Data 0	

7.3 HITAG S authentication mode

Table 4. Memory map for HITAG S in authentication mode

page address	MSByte						LSByte	
	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB
0x00	UID3		UID2		UID1		UID0	
0x01	PWDH0		CON2		CON1		CON0	
0x02	KEYH1		KEYH0		PWDL1		PWDL0	
0x03	KEYL3		KEYL2		KEYL1		KEYL0	
0x04	Data 3		Data 2		Data 1		Data 0	
0x05	Data 3		Data 2		Data 1		Data 0	

7.4 State Diagram

7.4.1 General Description of States

Power Off

The powering magnetic field is switched off or the HITAG S Transponder is out of field.

Ready

After start up phase, the HITAG S Transponder is ready to receive the first command.

Init

The HITAG S Transponder enters this State after the first UID REQUEST xx command. In this State the Response Protocol Mode (see [Section 7.5](#)) may be changed by further UID REQUEST xx commands. If there are several HITAG S Transponders in the field of the RWD antenna at the same time, the AC SEQUENCE can be started to determine the UID of every HITAG S Transponder.

Authenticate

The HITAG S Transponder enters this State after a valid SELECT (UID) command when configured in Authentication Mode. After an encrypted CHALLENGE Authentication the HITAG S Transponder changes into the Selected State.

Selected

The HITAG S Transponder enters this State after a valid SELECT (UID) command when configured in Plain Mode or a SELECT (UID) and CHALLENGE sequence when configured in Authentication Mode. Only one HITAG S Transponder in the field of the RWD antenna can be Selected at the same time. In this State, Read and Write operations are possible. Data Transmission is not encrypted even if configured in Authentication Mode.

Quiet

The HITAG S Transponder enters this State after a SELECT_QUIET (UID) command in Init State or a QUIET command in Selected State. In this State, the HITAG S Transponder will not answer to any command. Switching off the powering magnetic field or moving the HITAG S Transponder out of field enters it into the Power Off State.

Transponder Talks First (TTF)

The HITAG S Transponder enters this State when configured in TTF Mode if no UID REQUEST xx command is received within the Mode switch window. Once entered this State, the HITAG S Transponder continuously transmits data with configurable data coding, data rate and data length.

7.4.2 HITAG S256 and HITAG S2048

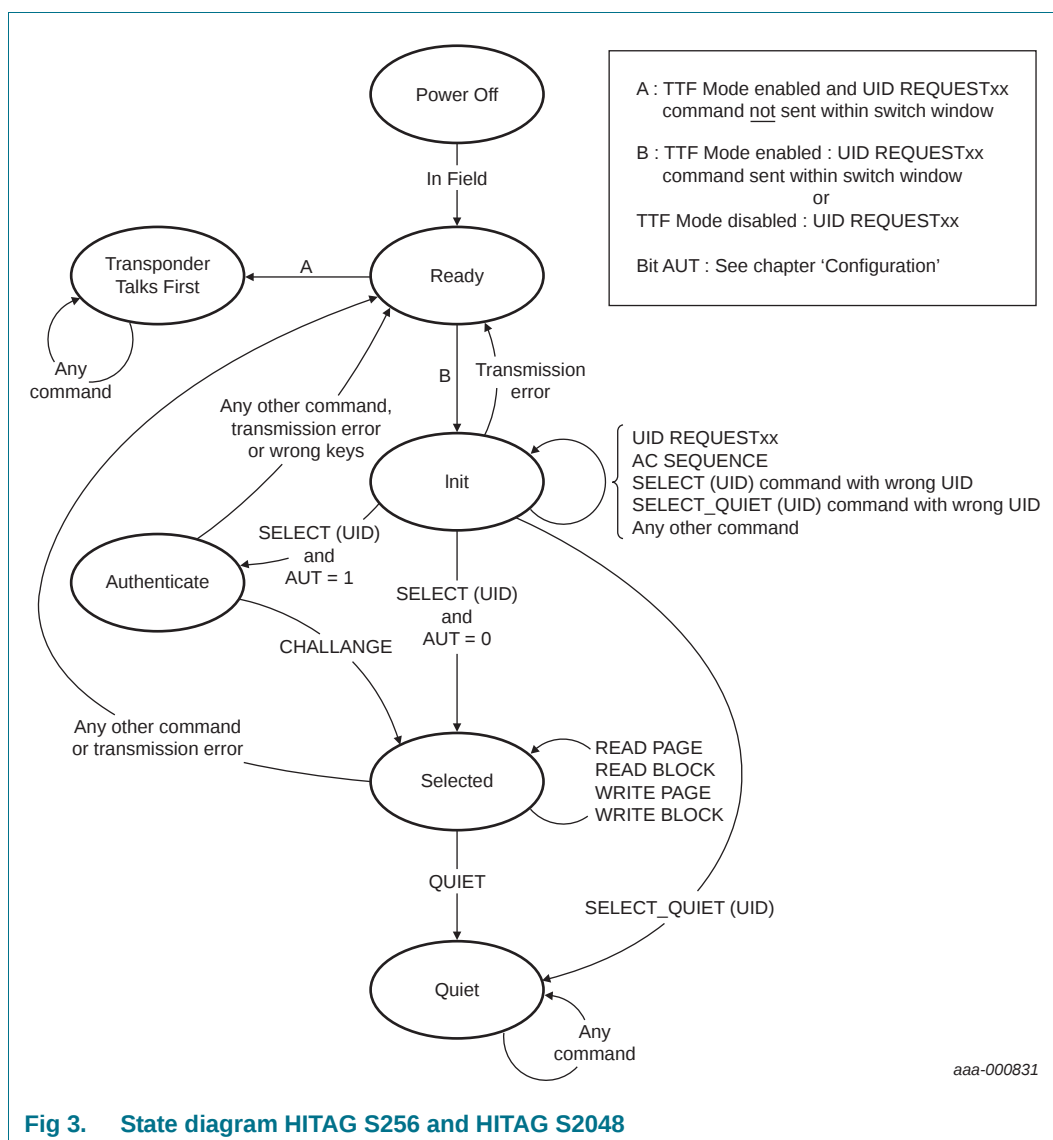


Fig 3. State diagram HITAG S256 and HITAG S2048

Remark: Switching off the powering magnetic field or moving the HITAG S Transponder out of the RWD antenna field enters the HITAG S Transponder into the Power off state independently of its actual state.

7.5 Command set

7.5.1 UID REQUEST xx

Table 5. UID request xx

				LSByte						MSByte	
	MSB	LSB		MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB
RWD:	UID REQUEST xx		EOF								
Transponder:			t _{wresp}	SOF	UID 0	UID 1	UID 2	UID 3			
				N=	1.....8	9.....k.....16	17.....24	25.....32			

7.5.2 AC SEQUENCE

If more than one HITAG S Transponder is in the field of the antenna a special designed RWD detects the first collision at the Bit position $N = k$ of the UID response. As a result the RWD starts an Anticollision Sequence (AC SEQUENCE).

Table 6. AC sequence

	MSB					LSB	1.....k	MSB	LSB		
RWD:	k4	k3	k3	k1	k0		k Bits of UID	CRC 8	EOF		
Transponder:										t_{wresp}	
										SOF	(32-k) bits to UID
										N=	k+1.....32

After transmitting this command, all HITAG S Transponders which first k Bits of the own UID match with the k received UID Bits, answer with the SOF and the rest of their own UID.

If a collision occurs again the described cycle has to be repeated until one valid UID of the transponders in the field is determined.

The complete response of the HITAG S Transponder is transmitted in Anticollision Coding (AC).

7.5.3 SELECT (UID)

Table 7. Select (UID)

LSByte								MSByte							
MSB		LSB	MSB		LSB	MSB		LSB	MSB		LSB	MSB		LSB	
RWD:	00000	UID 0	UID 1	UID 2	UID 3	CRC 8	EOF								
LSByte								MSByte							
MSB		LSB	MSB		LSB	MSB		LSB	MSB		LSB	MSB		LSB	
Transponder:								t _{wresp}	SOF	CON 0	CON 1	CON 2	Reserved	CRC 8	

The complete response of the HITAG S Transponder is transmitted in Manchester Coding (MC).

In Plain Mode the MSByte of Page 1 is a Reserved Byte, in Authentication Mode this Byte contains the password high Byte PWDH 0. At the response on a SELECT (UID) command of a HITAG S Transponder configured in Authentication Mode (Bit AUT = 1, keys and password locked), this PWDH 0 Byte is dissolved by '1' Bits.

7.5.4 CHALLENGE

By means of the response of the SELECT (UID) command the RWD detects that the HITAG S Transponder is configured in Authentication Mode (Bit AUT = 1) and starts the encrypted Challenge sequence.

Table 8. Challenge

	MSB	LSB	MSB	LSB											
RWD:	32 Bit RND		32 Bit Secret Data		EOF										
						MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB
Transponder:					t _{wresp}	SOF	CON 2	PWDH 0	PWDL 0	PWDL 1	CRC 8				
						32 Bit secret response									

The Read/Write Device sends a 32 bit Random Number (RND) and a 32 bit secret data stream to the transponder. In order to perform the secret data stream, a security co-processor is required on the read/write Device.

If the received secret data stream corresponds with the secret data stream calculated by the HITAG S Transponder, a 32 bit Secret Response (secret data stream encrypting the configuration byte CON 2, password high byte PWDH 0 and password low Bytes PWDL 0 and PWDL 1) is transmitted after the SOF.

The response of the HITAG S Transponder is transmitted in Manchester Coding (MC).

7.5.5 SELECT_QUITE (UID)

With this command a HITAG S Transponder in Init State can be directly entered into the quiet state.

Table 9. Select_quiet(UID)

		LSByte				MSByte			
		MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB
RWD:	00000	UID 0	UID 1	UID 2	UID 3	0	CRC 8	EOF	
									ACK
Transponder:								t _{wresp}	SOF 0 1

The Start Of Frame (SOF) pattern and the acknowledge (ACK) is transmitted in Manchester Coding.

7.5.6 READ PAGE

After a HITAG S Transponder was selected by the corresponding SELECT (UID) command (or SELECT (UID) and CHALLENGE for Authentication Mode) a read operation of data stored on the EEPROM can be performed. After transmitting the READ PAGE command, the Page address PADR (8 Bits) and the 8 bit Cyclic Redundancy Check (CRC 8), the HITAG S Transponder responds with the SOF and 32 Bits data of the corresponding Page.

Table 10. Read page

		MSB	LSB	MSB	LSB							
RWD:	1 1 0 0	PADR		CRC 8		EOF						
						LSByte				MSByte		
						MSB	LSB	MSB	LSB	MSB	LSB	
Transponder:					t _{wresp}	SOF	DATA 0	DATA 1	DATA 2	DATA 3	CRC 8	

The highest Page address (PADR) is 0x3F, therefore the two highest Bits must be '0'.

7.5.7 READ BLOCK

After transmitting the READ BLOCK command, the Page address PADR (8 Bits) within a block and the 8 bit Cyclic Redundancy Check (CRC 8), the HITAG S Transponder responds with the SOF and 32 up to 128 Bits of data beginning with the addressed Page within a Block to the last Page of the corresponding Block.

Table 11. Read block

		MSB	LSB	MSB	LSB														
RWD:	1 1 0 1	PADR		CRC 8		EOF													
						LSByte										MSByte			
						MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB		MSB	LSB	MSB	LSB	
Transponder:				t _{wresp}	SOF	DATA 0	DATA 1	DATA 2	DATA 3	DATA 0		DATA 3	CRC 8						

7.5.8 WRITE PAGE

After a HITAG S Transponder was selected by the corresponding SELECT (UID) command (or SELECT (UID) and CHALLENGE for Authentication Mode) a write operation of data onto the memory can be carried out. Least significant Byte is always transmitted first. E.g. in order to change the configuration page the byte CON0 would have to be transmitted first.

After transmitting the WRITE PAGE command, the Page address PADR (8 Bits) and the 8 bit Cyclic Redundancy Check (CRC 8), the HITAG S Transponder responds with the SOF and an acknowledge (ACK) to confirm the reception of a correct WRITE PAGE command. After the waiting time t_{wsc} the RWD transmits the write data with CRC 8. After the programming time t_{prog} the HITAG S Transponder responds with a SOF and an acknowledge to confirm correct programming.

Table 12. Write page

		MSB	LSB	MSB	LSB				
RWD:	1 0 0 0	PADR		CRC 8		EOF			t _{wsc}
ACK									
Transponder:					t _{wresp}	SOF	01		

Table 13. Write page

	LSByte				MSByte							
	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB				
RWD:	DATA 0		DATA 1		DATA 2		DATA 3		CRC 8		EOF	
												ACK
Transponder:										t _{prog}	SOF	01

7.5.9 WRITE BLOCK

After transmitting the WRITE BLOCK command, the Page address PADR (8 Bits) within a Block and the 8 bit Cyclic Redundancy Check (CRC 8), the HITAG S Transponder responds with the SOF and an acknowledge (ACK) to confirm the reception of a correct WRITE BLOCK command. After the waiting time t_{wsc} the RWD transmits the write data with CRC 8 Page by Page (1 to 4 Pages depending on the Page address PADR within the corresponding block). After the programming time t_{prog} the HITAG S Transponder responds with a SOF and an acknowledge to confirm correct programming of each Page.

Table 14. Write block

	MSB	LSB	MSB	LSB			
RWD:	1 0 0 1	PADR	CRC 8	EOF			t_{wsc}
						ACK	
Transponder:				t_{wresp}	SOF	01	

Table 15. Write data for page with page address: PADR

	LSByte		MSByte					
	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB
RWD:	DATA 0	DATA 1	DATA 2	DATA 3	CRC 8	EOF		t_{wsc}
							ACK	
Transponder:					t_{prog}	SOF	01	

Table 16. Write data for page with page address: PADR + 1

	LSByte		MSByte					
	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB
RWD:	DATA 0	DATA 1	DATA 2	DATA 3	CRC 8	EOF		t_{wsc}
							ACK	
Transponder:					t_{prog}	SOF	01	

Table 17. Write data for page with page address: PADR + 2

	LSByte		MSByte					
	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB
RWD:	DATA 0	DATA 1	DATA 2	DATA 3	CRC 8	EOF		t_{wsc}
							ACK	
Transponder:					t_{prog}	SOF	01	

Table 18. Write data for page with page address: PADR + 3

	LSByte		MSByte					
	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB
RWD:	DATA 0	DATA 1	DATA 2	DATA 3	CRC 8	EOF		t_{wsc}
							ACK	
Transponder:					t_{prog}	SOF	01	

7.5.10 QUIT

With this command a Selected HITAG S Transponder can be entered into the Quiet State.

A valid Page address PADR (8 Bits) and Cyclic Redundancy Check (CRC 8) must be sent for command structure reasons only.

Table 19. Quiet

		MSB	LSB	MSB	LSB		
RWD:	0 1 1 1	PADR		CRC 8		EOF	
							ACK
Transponder:					t _{wresp}	SOF	01

8. Limiting values

Table 20. Limiting values^{[1][2]}

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{ESD}	electrostatic discharge voltage	JEDEC JESD 22-A114-AB Human Body Model	±2	-	kV
I _{i(max)}	maximum input current	IN1-IN2	-	±20	mA
T _j	junction temperature		-25	+85	°C

- [1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the Operating Conditions and Electrical Characteristics section of this specification is not implied.
- [2] This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions should be taken to avoid applying values greater than the rated maxima

9. Characteristics

Table 21. Characteristics

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
f _i	input frequency		100	125	150	kHz
V _i	input voltage	IN1-IN2				
		read	-	±3.5	±4.5	V
		write	-	±6.3	±7.2	V
I _i	input current	IN1-IN2	-	-	±10	mA
Interface characteristics						
C _i	input capacitance	between IN1-IN2 ^[2] HTSICxxxxxEW/x7	199	210	221	pF
Wafer EEPROM characteristics						
t _{ret}	retention time	T _{amb} ≤ 55 °C	10	-	-	year
N _{endu(W)}	write endurance		100000			cycle

- [1] Typical ratings are not guaranteed. Values are at 25 °C.
- [2] Measured with Q_{coil} = 20, L_{coil} = 7.5 mH, optimal tuned to resonance circuit; V_{IN1-IN2} = 2 V (RMS)

10. Abbreviations

Table 22. Abbreviations

Acronym	Description
ASK	Amplitude Shift Keying
CRC	Cyclic Redundancy Check
EEPROM	Electrically Erasable Programmable Read-Only Memory
IC	Integrated Circuit
RF	Radio Frequency
RTF	Reader Talks First
RWD	Read Write Device
TTF	Transponder Talks First
UID	Unique Identification Number

11. Revision history

Table 23. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HTSICH56_48_SDS v.3.1	20141211	Product short data sheet	-	HTSICH56_48_SDS v.3.0
Modifications:	• Section 12 “Legal information”: License statement “ICs with HITAG functionality” removed • Section 2.6 “Delivery types”: updated • Section 5 “Ordering information”: updated			
HTSICH56_48_SDS v.3.0	20111012	Product short data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

12.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

12.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b)

whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

12.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

HITAG — is a trademark of NXP Semiconductors N.V.

13. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

14. Contents

1	General description	1
2	Features and benefits	1
2.1	Features	1
2.2	Protocol	1
2.3	Memory	2
2.4	Supported standards	2
2.5	Security features	2
2.6	Delivery types	2
3	Applications	2
4	Quick reference data	3
5	Ordering information	3
6	Block diagram	4
7	Functional description	5
7.1	Memory organization	5
7.2	HITAG S plain mode	6
7.3	HITAG S authentication mode	6
7.4	State Diagram	7
7.4.1	General Description of States	7
7.4.2	HITAG S256 and HITAG S2048	8
7.5	Command set	9
7.5.1	UID REQUEST xx	9
7.5.2	AC SEQUENCE	9
7.5.3	SELECT (UID)	10
7.5.4	CHALLENGE	11
7.5.5	SELECT_QUITE (UID)	12
7.5.6	READ PAGE	12
7.5.7	READ BLOCK	13
7.5.8	WRITE PAGE	14
7.5.9	WRITE BLOCK	15
7.5.10	QUITE	16
8	Limiting values	17
9	Characteristics	17
10	Abbreviations	18
11	Revision history	18
12	Legal information	19
12.1	Data sheet status	19
12.2	Definitions	19
12.3	Disclaimers	19
12.4	Trademarks	20
13	Contact information	20
14	Contents	21

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2014.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 11 December 2014
210331