Ultralow Noise XFET® Voltage References with Current Sink and Source Capability

ADR430/ADR431/ADR433/ADR434/ADR435/ADR439

FEATURES

- Low noise (0.1 Hz to 10 Hz): 3.5 µV p-p @ 2.5 V output
- No external capacitor required
- Low temperature coefficient
  - A Grade: 10 ppm/°C max
  - B Grade: 3 ppm/°C max
- Load regulation: 15 ppm/mA
- Line regulation: 20 ppm/V
- Wide operating range
  - ADR430: 4.1 V to 18 V
  - ADR431: 4.5 V to 18 V
  - ADR433: 5.0 V to 18 V
  - ADR434: 6.1 V to 18 V
  - ADR435: 7.0 V to 18 V
  - ADR439: 6.5 V to 18 V
- High output current: +30 mA/−20 mA
- Wide temperature range: −40°C to +125°C

APPLICATIONS

- Precision data acquisition systems
- High resolution data converters
- Medical instruments
- Industrial process control systems
- Optical control circuits
- Precision instruments

PIN CONFIGURATIONS

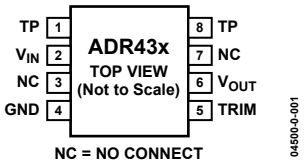

Figure 1. 8-Lead MSOP (RM Suffix)

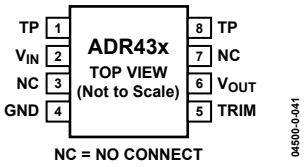

Figure 2. 8-Lead SOIC (R Suffix)

GENERAL DESCRIPTION

The ADR43x series is a family of XFET voltage references featuring low noise, high accuracy, and low temperature drift performance. Using ADI's patented temperature drift curvature correction and XFET (eXtra implanted junction FET) technology, the ADR43x's voltage change versus temperature nonlinearity is minimized.

The XFET references operate at lower current (800 µA) and supply headroom (2 V) than buried-Zener references. Buried-Zener references require more than 5 V headroom for operations. The ADR43x XFET references are the only low noise solutions for 5 V systems.

The ADR43x series has the capability to source up to 30 mA and sink up to 20 mA of output current. It also comes with a TRIM terminal to adjust the output voltage over a 0.5% range without compromising performance. The ADR43x is available in the 8-lead mini SOIC and 8-lead SOIC packages.

All versions are specified over the extended industrial temperature range (−40°C to +125°C).

Table 1. Selection Guide

Model	V_{OUT} (V)	Accuracy (mV)	Temperature Coefficient (ppm/°C)
ADR430B	2.048	±1	3
ADR430A	2.048	±3	10
ADR431B	2.500	±1	3
ADR431A	2.500	±3	10
ADR433B	3.000	±1.4	3
ADR433A	3.000	±4	10
ADR434B	4.096	±1.5	3
ADR434A	4.096	±5	10
ADR435B	5.000	±2	3
ADR435A	5.000	±6	10
ADR439B	4.500	±2	3
ADR439A	4.500	±5.4	10

Rev. B

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REVISION HISTORY

9/04—Data Sheet Changed from Rev. A to Rev. B

Added New Grade ... Universal
Changes to Specifications ... 3
Replaced Figure 3, Figure 4, Figure 5 ... 10
Updated Ordering Guide ... 21

6/04—Data Sheet Changed from Rev. 0 to Rev. A

Changes to Format ... Universal
Changes to the Ordering Guide ... 20

12/03—Revision 0: Initial Version

SPECIFICATIONS

ADR430 ELECTRICAL CHARACTERISTICS

V_{IN} = 4.1 V to 18 V, I_{LOAD} = 0 mA, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage						
B Grade	V_O		2.047	2.048	2.049	V
A Grade	V_O		2.045	2.048	2.051	V
Initial Accuracy						
B Grade	V_{OERR}				1	mV
B Grade	V_{OERR}				0.05	%
A Grade	V_{OERR}				3	mV
A Grade	V_{OERR}				0.15	%
Temperature Coefficient						
SOIC-8 (B Grade)	TCV_O	−40°C < T_A < +125°C		1	3	ppm/°C
SOIC-8 (A Grade)	TCV_O	−40°C < T_A < +125°C		2	10	
MSOP-8	TCV_O	−40°C < T_A < +125°C		2	10	ppm/°C
Line Regulation	$\Delta V_O/\Delta V_{IN}$	V_{IN} = 4.1 V to 18 V				
		−40°C < T_A < +125°C		5	20	ppm/V
Load Regulation	$\Delta V_O/\Delta I_{LOAD}$	I_{LOAD} = 0 mA to 10 mA, V_{IN} = 5.0 V				
		−40°C < T_A < +125°C			15	ppm/mA
		I_{LOAD} = −10 mA to 0 mA, V_{IN} = 5.0 V				
		−40°C < T_A < +125°C			15	ppm/mA
Quiescent Current	I_{IN}	No load, −40°C < T_A < +125°C		560	800	µA
Voltage Noise	e_N p-p	0.1 Hz to 10.0 Hz		3.5		µV p-p
Voltage Noise Density	e_N	1 kHz		60		$nV\sqrt{Hz}$
Turn-On Settling Time	t_R	C_{IN} = 0		10		µs
Long-Term Stability[1]	ΔV_O	1,000 h		40		ppm
Output Voltage Hysteresis	V_{O_HYS}			20		ppm
Ripple Rejection Ratio	RRR	f_{IN} = 10 kHz		−70		dB
Short Circuit to GND	I_{SC}			40		mA
Supply Voltage Operating Range	V_{IN}		4.1		18	V
Supply Voltage Headroom	$V_{IN} - V_O$		2			V

[1] The long-term stability specification is noncumulative. The drift in subsequent 1,000 hour periods is significantly lower than in the first 1,000 hour period.

ADR431 ELECTRICAL CHARACTERISTICS

V_{IN} = 4.5 V to 18 V, I_{LOAD} = 0 mA, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage						
B Grade	V_O		2.499	2.500	2.501	V
A Grade	V_O		2.497	2.500	2.503	V
Initial Accuracy						
B Grade	V_{OERR}				1	mV
B Grade	V_{OERR}				0.04	%
A Grade	V_{OERR}				3	mV
A Grade	V_{OERR}				0.13	%
Temperature Coefficient						
SOIC-8 (B Grade)	TCV_O	−40°C < T_A < +125°C		1	3	ppm/°C
SOIC-8 (A Grade)	TCV_O	−40°C < T_A < +125°C		2	10	ppm/°C
MSOP-8	TCV_O	−40°C < T_A < +125°C		2	10	ppm/°C
Line Regulation	$\Delta V_O/\Delta V_{IN}$	V_{IN} = 4.5 V to 18 V				
		−40°C < T_A < +125°C		5	20	ppm/V
Load Regulation	$\Delta V_O/\Delta I_{LOAD}$	I_{LOAD} = 0 mA to 10 mA, V_{IN} = 5.0 V				
		−40°C < T_A < +125°C			15	ppm/mA
		I_{LOAD} = −10 mA to 0 mA, V_{IN} = 5.0 V				
		−40°C < T_A < +125°C			15	ppm/mA
Quiescent Current	I_{IN}	No load, −40°C < T_A < +125°C		580	800	µA
Voltage Noise	e_N p-p	0.1 Hz to 10.0 Hz		3.5		µV p-p
Voltage Noise Density	e_N	1 kHz		80		$nV\sqrt{Hz}$
Turn-On Settling Time	t_R	C_{IN} = 0		10		µs
Long-Term Stability[1]	ΔV_O	1,000 h		40		ppm
Output Voltage Hysteresis	V_{O_HYS}			20		ppm
Ripple Rejection Ratio	RRR	f_{IN} = 10 kHz		−70		dB
Short Circuit to GND	I_{SC}			40		mA
Supply Voltage Operating Range	V_{IN}		4.5		18	V
Supply Voltage Headroom	$V_{IN} - V_O$		2			V

[1] The long-term stability specification is noncumulative. The drift in subsequent 1,000 hour periods is significantly lower than in the first 1,000 hour period.

ADR433 ELECTRICAL CHARACTERISTICS

V_{IN} = 5 V to 18 V, I_{LOAD} = 0 mA , T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage						
B Grade	V_O		2.9985	3.000	3.0015	V
A Grade	V_O		2.996	3.000	3.004	V
Initial Accuracy						
B Grade	V_{OERR}				1.5	mV
B Grade	V_{OERR}				0.05	%
A Grade	V_{OERR}				4	mV
A Grade	V_{OERR}				0.13	%
Temperature Coefficient	TCV_O					
SOIC-8 (B Grade)		−40°C < T_A < +125°C		1	3	ppm/°C
SOIC-8 (A Grade)		−40°C < T_A < +125°C		2	10	ppm/°C
MSOP-8		−40°C < T_A < +125°C		2	10	ppm/°C
Line Regulation	$\Delta V_O/\Delta V_{IN}$	V_{IN} = 5 V to 18 V				
		−40°C < T_A < +125°C		5	20	ppm/V
Load Regulation	$\Delta V_O/\Delta I_{LOAD}$	I_{LOAD} = 0 mA to 10 mA, V_{IN} = 6 V				
		−40°C < T_A < +125°C			15	ppm/mA
		I_{LOAD} = −10 mA to 0 mA, V_{IN} = 6 V				
		−40°C < T_A < +125°C			15	ppm/mA
Quiescent Current	I_{IN}	No load, −40°C < T_A < +125°C		590	800	µA
Voltage Noise	e_N p-p	0.1 Hz to 10.0 Hz		3.75		µV p-p
Voltage Noise Density	e_N	1 kHz		90		$nV\sqrt{Hz}$
Turn-On Settling Time	t_R	C_{IN} = 0		10		µs
Long-Term Stability[1]	ΔV_O	1,000 h		40		ppm
Output Voltage Hysteresis	V_{O_HYS}			20		ppm
Ripple Rejection Ratio	RRR	f_{IN} = 10 kHz		−70		dB
Short Circuit to GND	I_{SC}			40		mA
Supply Voltage Operating Range	V_{IN}		5		18	V
Supply Voltage Headroom	$V_{IN} - V_O$		2			V

[1]The long-term stability specification is noncumulative. The drift in subsequent 1,000 hour periods is significantly lower than in the first 1,000 hour period.

ADR434 ELECTRICAL CHARACTERISTICS

V_{IN} = 6.1 V to 18 V, I_{LOAD} = 0 mA, T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage						
B Grade	V_O		4.0945	4.096	4.0975	V
A Grade	V_O		4.091	4.096	4.101	V
Initial Accuracy						
B Grade	V_{OERR}				1.5	mV
B Grade	V_{OERR}				0.04	%
A Grade	V_{OERR}				5	mV
A Grade	V_{OERR}				0.13	%
Temperature Coefficient	TCV_O					
SOIC-8 (B Grade)		−40°C < T_A < +125°C		1	3	ppm/°C
SOIC-8 (A Grade)		−40°C < T_A < +125°C		2	10	ppm/°C
MSOP-8		−40°C < T_A < +125°C		2	10	ppm/°C
Line Regulation	$\Delta V_O/\Delta V_{IN}$	V_{IN} = 6.1 V to 18 V				
		−40°C < T_A < +125°C		5	20	ppm/V
Load Regulation	$\Delta V_O/\Delta I_{LOAD}$	I_{LOAD} = 0 mA to 10 mA, V_{IN} = 7 V				
		−40°C < T_A < +125°C			15	ppm/mA
		I_{LOAD} = −10 mA to 0 mA, V_{IN} = 7 V				
		−40°C < T_A < +125°C			15	ppm/mA
Quiescent Current	I_{IN}	No load, −40°C < T_A < +125°C		595	800	µA
Voltage Noise	e_N p-p	0.1 Hz to 10.0 Hz		6.25		µV p-p
Voltage Noise Density	e_N	1 kHz		100		$nV\sqrt{Hz}$
Turn-On Settling Time	t_R	C_{IN} = 0		10		µs
Long-Term Stability[1]	ΔV_O	1,000 h		40		ppm
Output Voltage Hysteresis	V_{O_HYS}			20		ppm
Ripple Rejection Ratio	RRR	f_{IN} = 10 kHz		−70		dB
Short Circuit to GND	I_{SC}			40		mA
Supply Voltage Operating Range	V_{IN}		6.1		18	V
Supply Voltage Headroom	$V_{IN} - V_O$		2			V

[1] The long-term stability specification is noncumulative. The drift in subsequent 1,000 hour periods is significantly lower than in the first 1,000 hour period.

ADR435 ELECTRICAL CHARACTERISTICS

V_{IN} = 7 V to 18 V, I_{LOAD} = 0 mA, T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage						
B Grade	V_O		4.998	5.000	5.002	V
A Grade	V_O		4.994	5.000	5.006	V
Initial Accuracy						
B Grade	V_{OERR}				2	mV
B Grade	V_{OERR}				0.04	%
A Grade	V_{OERR}				6	mV
A Grade	V_{OERR}				0.12	%
Temperature Coefficient	TCV_O					
SOIC-8 (B Grade)		−40°C < T_A < +125°C		1	3	ppm/°C
SOIC-8 (A Grade)		−40°C < T_A < +125°C		2	10	ppm/°C
MSOP-8		−40°C < T_A < +125°C		2	10	ppm/°C
Line Regulation	$\Delta V_O/\Delta VIN$	V_{IN} = 7 V to 18 V				
		−40°C < T_A < +125°C		5	20	ppm/V
Load Regulation	$\Delta V_O/\Delta I_{LOAD}$	I_{LOAD} = 0 mA to 10 mA, V_{IN} = 8 V				
		−40°C < T_A < +125°C			15	ppm/mA
		I_{LOAD} = −10 mA to 0 mA, V_{IN} = 8 V				
		−40°C < T_A < +125°C			15	ppm/mA
Quiescent Current	I_{IN}	No load, −40°C < T_A < +125°C		620	800	µA
Voltage Noise	e_N p-p	0.1 Hz to 10 Hz		8		µV p-p
Voltage Noise Density	e_N	1 kHz		115		nV/$\sqrt{Hz}$
Turn-On Settling Time	t_R	C_{IN} = 0		10		µs
Long-Term Stability[1]	ΔV_O	1,000 h		40		ppm
Output Voltage Hysteresis	V_{O_HYS}			20		ppm
Ripple Rejection Ratio	RRR	f_{IN} = 10 kHz		−70		dB
Short Circuit to GND	I_{SC}			40		mA
Supply Voltage Operating Range	V_{IN}		7		18	V
Supply Voltage Headroom	$V_{IN} - V_O$		2			V

[1] The long-term stability specification is noncumulative. The drift in subsequent 1,000 hour periods is significantly lower than in the first 1,000 hour period.

ADR439 ELECTRICAL CHARACTERISTICS

V_{IN} = 6.5 V to 18 V, I_{LOAD} = 0 mV, T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage						
B Grade	V_O		4.498	4.500	4.502	V
A Grade	V_O		4.4946	4.500	4.5054	V
Initial Accuracy						
B Grade	V_{OERR}				2	mV
B Grade	V_{OERR}				0.04	%
A Grade	V_{OERR}				5.4	mV
A Grade	V_{OERR}				0.12	%
Temperature Coefficient	TCV_O					
SOIC-8 (B Grade)		−40°C < T_A < +125°C		1	3	ppm/°C
SOIC-8 (A Grade)		−40°C < T_A < +125°C		2	10	ppm/°C
MSOP-8		−40°C < T_A < +125°C		2	10	ppm/°C
Line Regulation	$\Delta V_O/\Delta V_{IN}$	V_{IN} = 6.5 V to 18 V				
		−40°C < T_A < +125°C		5	20	ppm/V
Load Regulation	$\Delta V_O/\Delta I_{LOAD}$	I_{LOAD} = 0 mA to 10 mA, V_{IN} = 6.5 V				
		−40°C < T_A < +125°C			15	ppm/mA
		I_{LOAD} = −10 mA to 0 mA, V_{IN} = 6.5 V				
		−40°C < T_A < +125°C			15	ppm/mA
Quiescent Current	I_{IN}	No load, −40°C < T_A < +125°C		600	800	µA
Voltage Noise	e_N p-p	0.1 Hz to 10.0 Hz		7.5		µV p-p
Voltage Noise Density	e_N	1 kHz		110		nV/$\sqrt{Hz}$
Turn-On Settling Time	t_R	C_{IN} = 0		10		µs
Long-Term Stability[1]	ΔV_O	1,000 h		40		ppm
Output Voltage Hysteresis	V_{O_HYS}			20		ppm
Ripple Rejection Ratio	RRR	f_{IN} = 10 kHz		−70		dB
Short Circuit to GND	I_{SC}			40		mA
Supply Voltage Operating Range	V_{IN}		6.5		18	V
Supply Voltage Headroom	$V_{IN} - V_O$		2			V

[1] The long-term stability specification is noncumulative. The drift in subsequent 1,000 hour periods is significantly lower than in the first 1,000 hour period.

ABSOLUTE MAXIMUM RATINGS

@ 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
Supply Voltage	20 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range (R, RM Packages)	−65°C to +125°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 60 s)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Absolute maximum ratings apply individually only, not in combination.

PACKAGE TYPE

Table 9.

Package Type	θ_{JA}[1]	θ_{JC}	Unit
8-Lead SOIC (R)	130	43	°C/W
8-Lead MSOP (RM)	190		°C/W

[1] θ_{JA} is specified for worst-case conditions (device soldered in circuit board for surface-mount packages).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

Default conditions: ±5 V, C_L = 5 pF, G = 2, $R_g = R_f$ = 1 kΩ, R_L = 2 kΩ, V_O = 2 V p-p, Frequency = 1 MHz, T_A = 25°C.

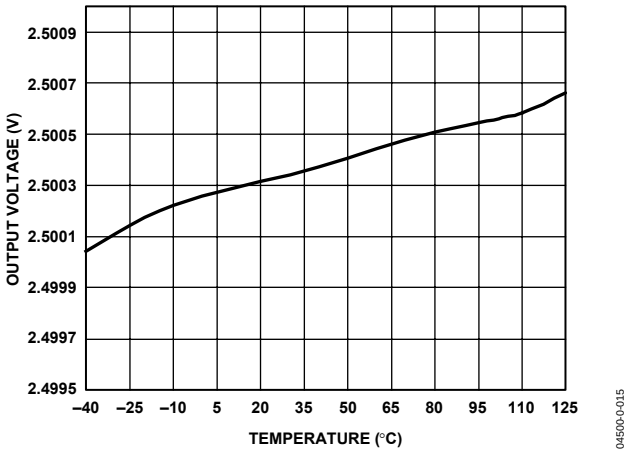

Figure 3. ADR431 V_{OUT} vs. Temperature

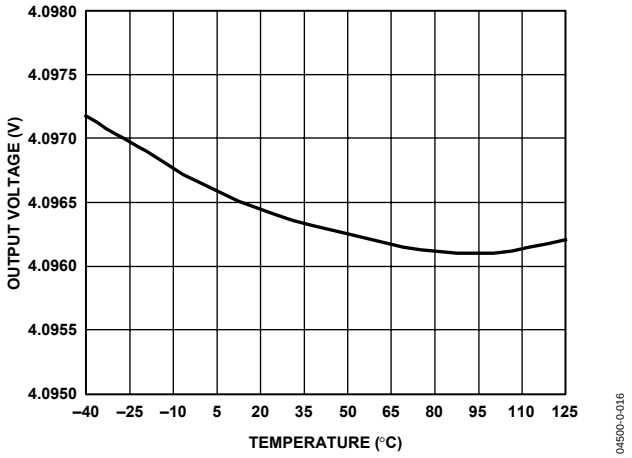

Figure 4. ADR434 V_{OUT} vs. Temperature

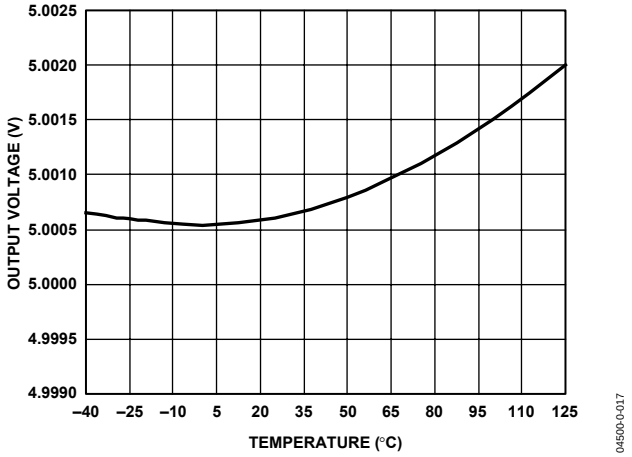

Figure 5. ADR435 V_{OUT} vs. Temperature

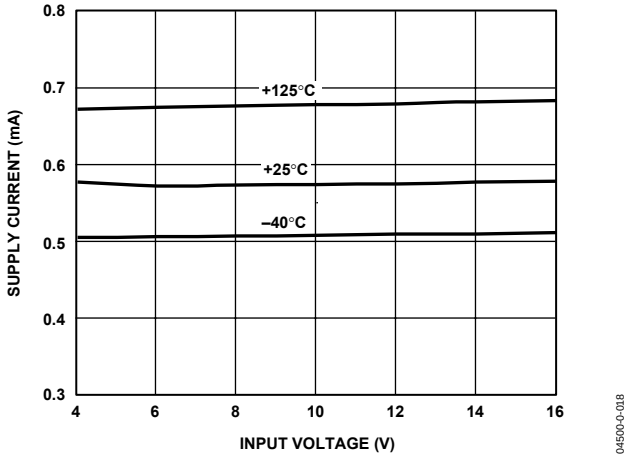

Figure 6. ADR435 Supply Current vs. Input Voltage

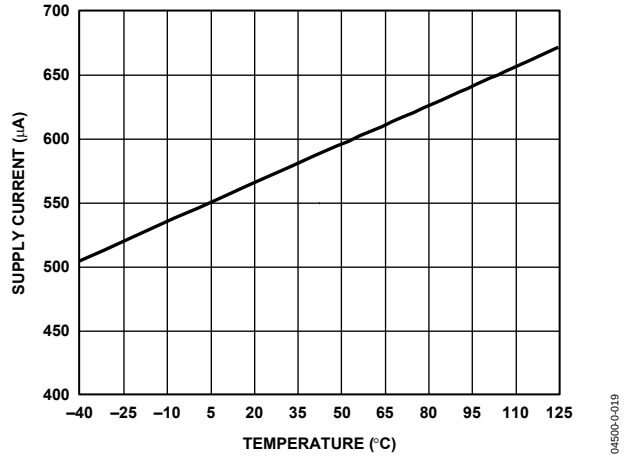

Figure 7. ADR435 Supply Current vs. Temperature

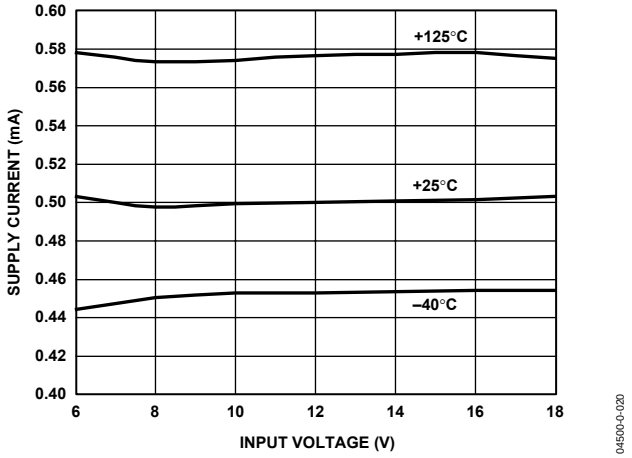

Figure 8. ADR431 Supply Current vs. Input Voltage

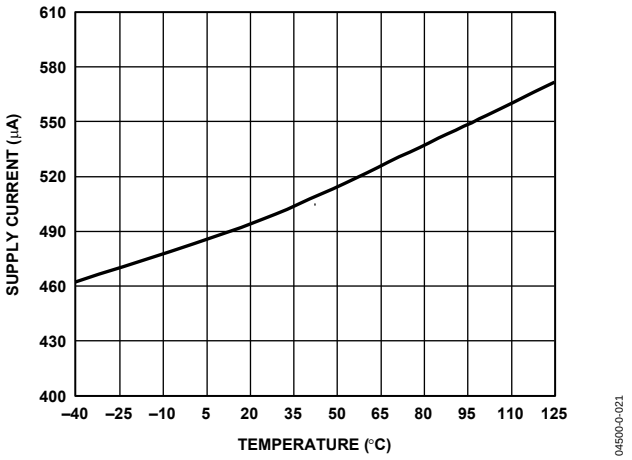

Figure 9. ADR431 Supply Current vs. Temperature

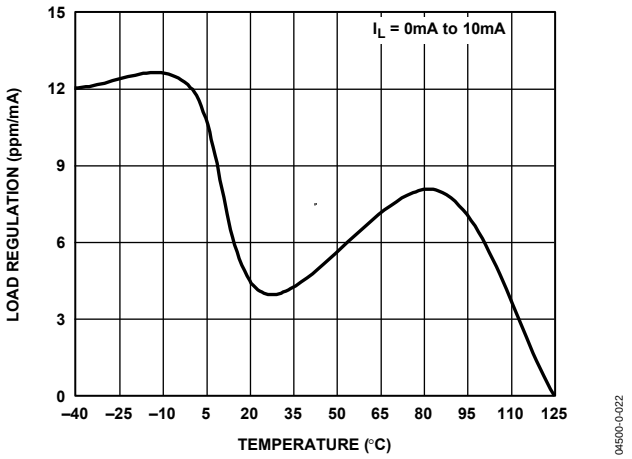

Figure 10. ADR431 Load Regulation vs. Temperature

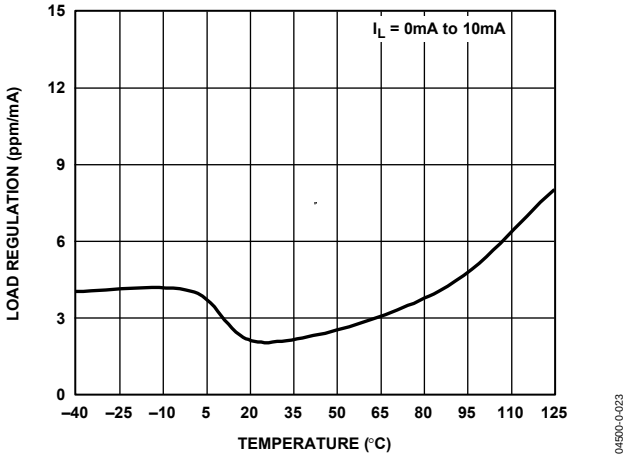

Figure 11. ADR435 Load Regulation vs. Temperature

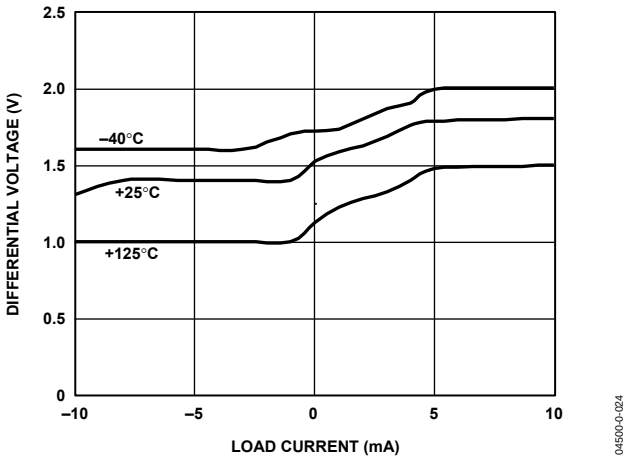

Figure 12. ADR431 Minimum Input/Output Differential Voltage vs. Load Current

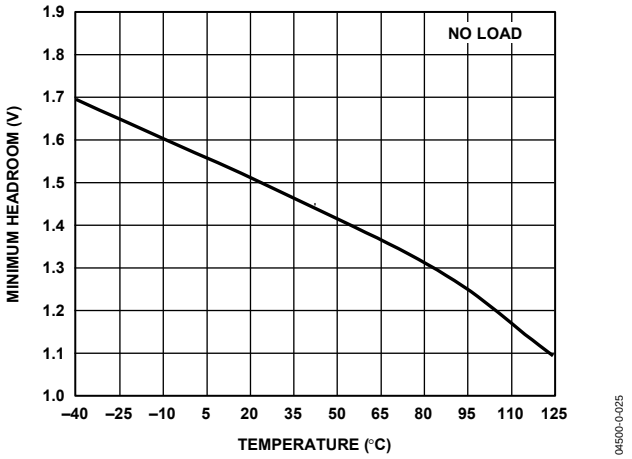

Figure 13. ADR431 Minimum Headroom vs. Temperature

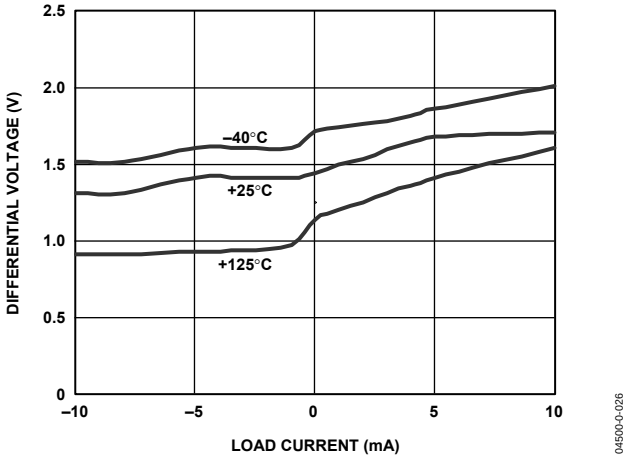

Figure 14. ADR435 Minimum Input/Output Differential Voltage vs. Load Current

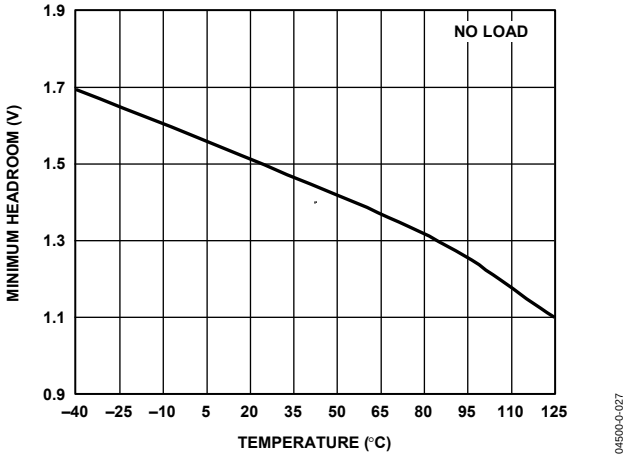

Figure 15. ADR435 Minimum Headroom vs. Temperature

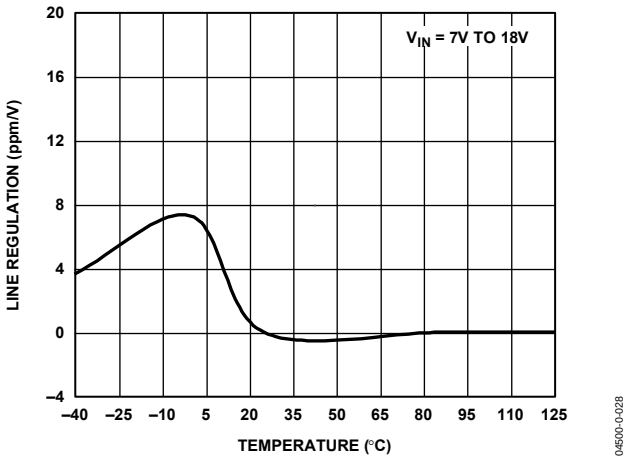

Figure 16. ADR435 Line Regulation vs. Temperature

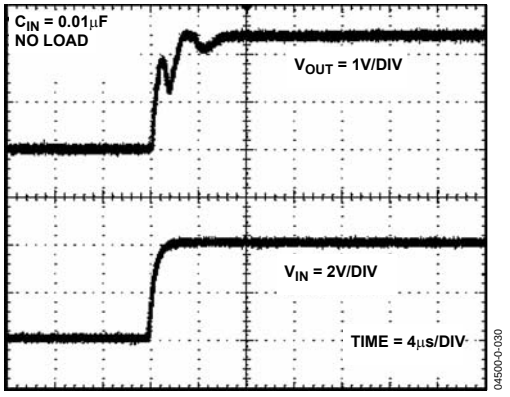

Figure 17. ADR431 Turn-On Response

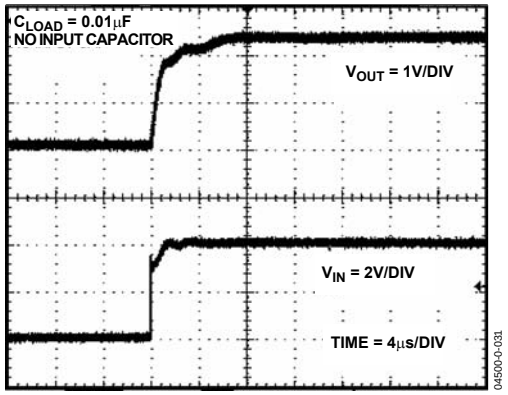

Figure 18. ADR431 Turn-On Response, 0.01 µF Load Capacitor

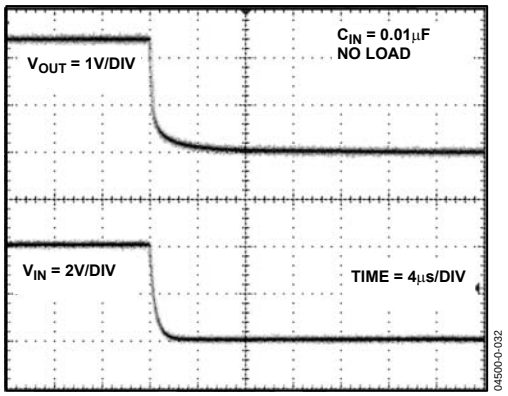

Figure 19. ADR431 Turn-Off Response

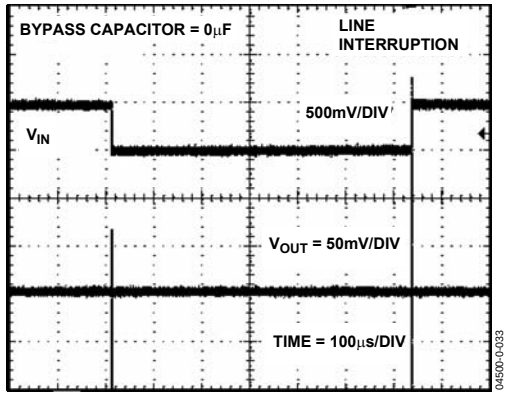

Figure 20. ADR431 Line Transient Response—No Capacitors

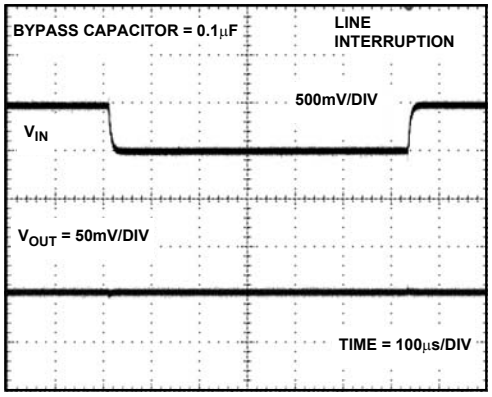

Figure 21. ADR431 Line Transient Response—0.1 µF Bypass Capacitor

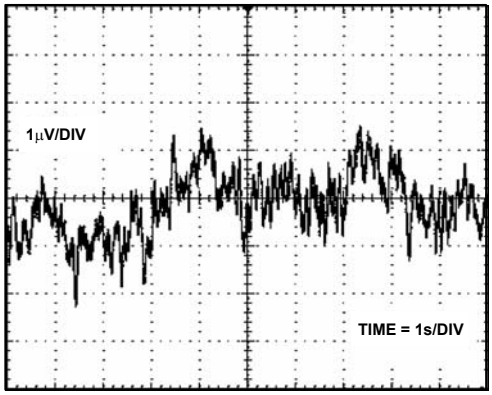

Figure 22. ADR431 0.1 Hz to 10.0 Hz Voltage Noise

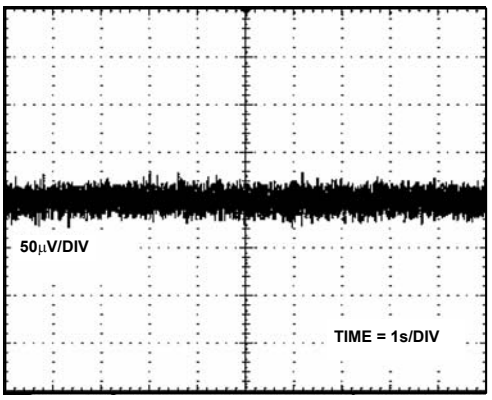

Figure 23. ADR431 10 Hz to 10 kHz Voltage Noise

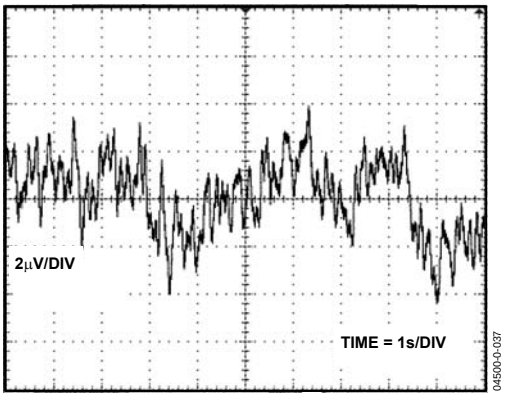

Figure 24. ADR435 0.1 Hz to 10.0 Hz Voltage Noise

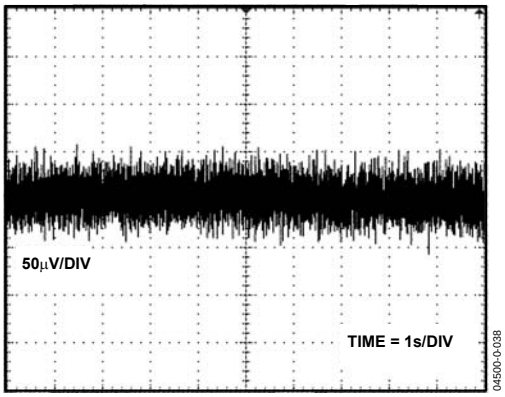

Figure 25. ADR435 10 Hz to 10 kHz Voltage Noise

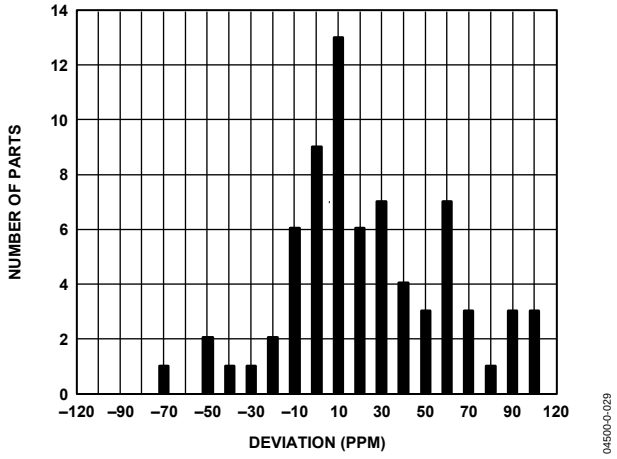

Figure 26. ADR431 Typical Hysteresis

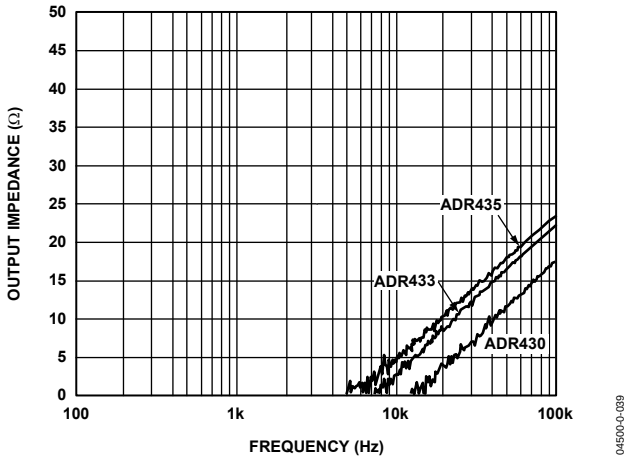

Figure 27. Output Impedance vs. Frequency

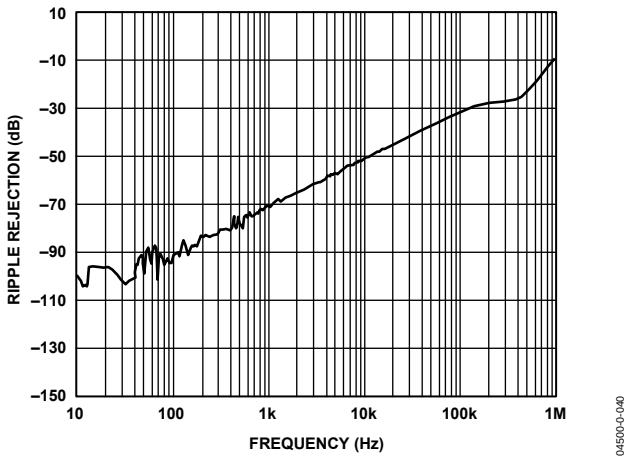

Figure 28. Ripple Rejection Ratio

THEORY OF OPERATION

The ADR43x series of references uses a new reference generation technique known as XFET (eXtra implanted junction FET). This technique yields a reference with low supply current, good thermal hysteresis, and exceptionally low noise. The core of the XFET reference consists of two junction field-effect transistors (JFETs), one of which has an extra channel implant to raise its pinch-off voltage. By running the two JFETs at the same drain current, the difference in pinch-off voltage can be amplified and used to form a highly stable voltage reference.

The intrinsic reference voltage is around 0.5 V with a negative temperature coefficient of about –120 ppm/°C. This slope is essentially constant to the dielectric constant of silicon and can be closely compensated by adding a correction term generated in the same fashion as the proportional-to-temperature (PTAT) term used to compensate band gap references. The big advantage of an XFET reference is that the correction term is some 30 times lower (therefore, requiring less correction) than for a band gap reference, resulting in much lower noise, because most of the noise of a band gap reference comes from the temperature compensation circuitry.

Figure 29 shows the basic topology of the ADR43x series. The temperature correction term is provided by a current source with a value designed to be proportional to absolute temperature. The general equation is

$$V_{OUT} = G \times \left(\Delta V_P - R1 \times I_{PTAT}\right) \quad (1)$$

where:
G is the gain of the reciprocal of the divider ratio.
ΔV_P is the difference in pinch-off voltage between the two JFETs.
I_{PTAT} is the positive temperature coefficient correction current.

ADR43x devices are created by on-chip adjustment of R2 and R3 to achieve 2.048 V or 2.500 V, respectively, at the reference output.

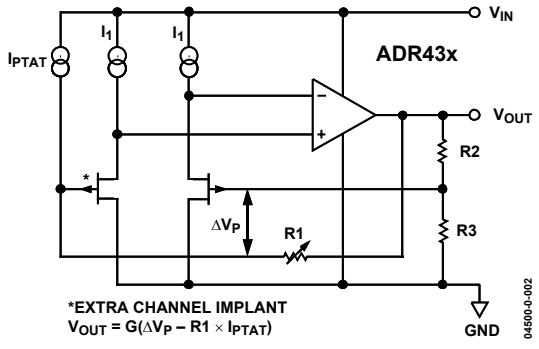

Figure 29. Simplified Schematic Device Power Dissipation Considerations

The ADR43x family of references is guaranteed to deliver load currents to 10 mA with an input voltage that ranges from 4.5 V to 18 V. When these devices are used in applications at higher currents, users should use the following equation to account for the temperature effects due to the power dissipation increases.

$$T_J = P_D \times \theta_{JA} + T_A \quad (2)$$

where:
T_J and T_A are the junction and ambient temperatures, respectively.
P_D is the device power dissipation.
θ_{JA} is the device package thermal resistance.

BASIC VOLTAGE REFERENCE CONNECTIONS

Voltage references, in general, require a bypass capacitor connected from V_{OUT} to GND. The circuit in Figure 30 illustrates the basic configuration for the ADR43x family of references. Other than a 0.1 µF capacitor at the output to help improve noise suppression, a large output capacitor at the output is not required for circuit stability.

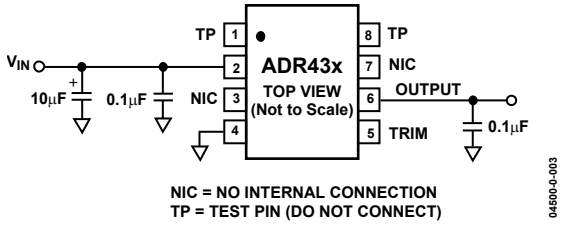

Figure 30. Basic Voltage Reference Configuration

NOISE PERFORMANCE

The noise generated by the ADR43x family of references is typically less than 3.75 µV p-p over the 0.1 Hz to 10.0 Hz band for ADR430, ADR431, and ADR433. Figure 22 shows the 0.1 Hz to 10 Hz noise of the ADR431, which is only 3.5 µV p-p. The noise measurement is made with a band-pass filter made of a 2-pole high-pass filter with a corner frequency at 0.1 Hz and a 2-pole low-pass filter with a corner frequency at 10.0 Hz.

TURN-ON TIME

Upon application of power (cold start), the time required for the output voltage to reach its final value within a specified error band is defined as the turn-on settling time. Two components normally associated with this are the time for the active circuits to settle and the time for the thermal gradients on the chip to stabilize. Figure 17 and Figure 18 show the turn-on settling time for the ADR431.

APPLICATIONS

OUTPUT ADJUSTMENT

The ADR43x trim terminal can be used to adjust the output voltage over a ±0.5% range. This feature allows the system designer to trim system errors out by setting the reference to a voltage other than the nominal. This is also helpful if the part is used in a system at temperature to trim out any error. Adjustment of the output has negligible effect on the temperature performance of the device. To avoid degrading temperature coefficients, both the trimming potentiometer and the two resistors need to be low temperature coefficient types, preferably <100 ppm/°C.

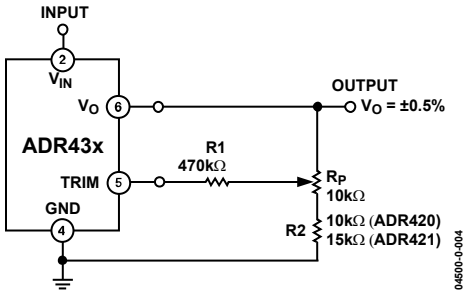

Figure 31. Output Trim Adjustment

REFERENCE FOR CONVERTERS IN OPTICAL NETWORK CONTROL CIRCUITS

In the upcoming high capacity, all-optical router network, Figure 32 employs arrays of micromirrors to direct and route optical signals from fiber to fiber without first converting them to electrical form, which reduces the communication speed. The tiny micromechanical mirrors are positioned so that each is illuminated by a single wavelength that carries unique information and can be passed to any desired input and output fiber. The mirrors are tilted by the dual-axis actuators controlled by precision ADCs and DACs within the system. Due to the microscopic movement of the mirrors, not only is the precision of the converters important, but the noise associated with these controlling converters is also extremely critical, because total noise within the system can be multiplied by the number of converters employed. As a result, to maintain the stability of the control loop for this application, the ADR43x is necessary due to its exceptionally low noise.

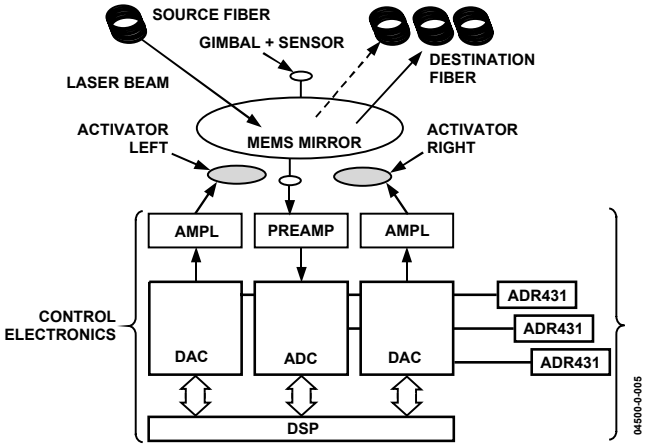

Figure 32. All-Optical Router Network

NEGATIVE PRECISION REFERENCE WITHOUT PRECISION RESISTORS

In many current-output CMOS DAC applications where the output signal voltage must be of the same polarity as the reference voltage, it is often required to reconfigure a current-switching DAC into a voltage-switching DAC through the use of a 1.25 V reference, an op amp, and a pair of resistors. Using a current-switching DAC directly requires an additional operational amplifier at the output to re-invert the signal. A negative voltage reference is then desirable from the standpoint that an additional operational amplifier is not required for either re-inversion (current-switching mode) or amplification (voltage-switching mode) of the DAC output voltage. In general, any positive voltage reference can be converted into a negative voltage reference through the use of an operational amplifier and a pair of matched resistors in an inverting configuration. The disadvantage to this approach is that the largest single source of error in the circuit is the relative matching of the resistors used.

A negative reference can easily be generated by adding a precision op amp and configuring it as shown in Figure 33. V_{OUT} is at virtual ground and, therefore, the negative reference can be taken directly from the output of the op amp. The op amp must be dual supply, have low offset and rail-to-rail capability, if negative supply voltage is close to the reference output.

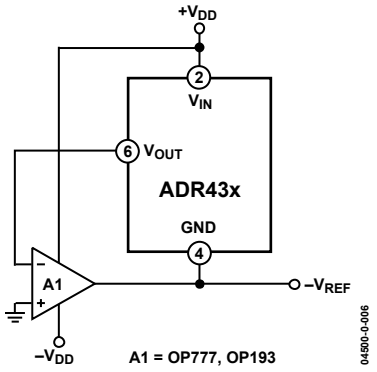

Figure 33. Negative Reference

HIGH VOLTAGE FLOATING CURRENT SOURCE

The circuit in Figure 34 can be used to generate a floating current source with minimal self-heating. This particular configuration can operate on high supply voltages determined by the breakdown voltage of the N-channel JFET.

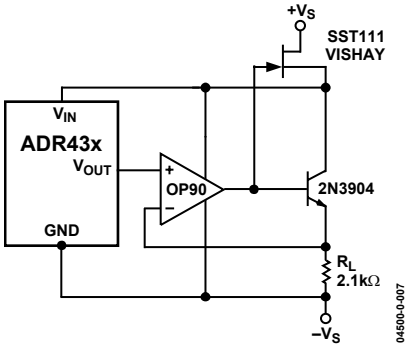

Figure 34. High Voltage Floating Current Source

KELVIN CONNECTIONS

In many portable instrumentation applications where PC board cost and area go hand-in-hand, circuit interconnects are very often of dimensionally minimum width. These narrow lines can cause large voltage drops if the voltage reference is required to provide load currents to various functions. In fact, a circuit's interconnects can exhibit a typical line resistance of 0.45 mΩ/square (1 oz. Cu, for example). Force and sense connections, also referred to as Kelvin connections, offer a convenient method of eliminating the effects of voltage drops in circuit wires. Load currents flowing through wiring resistance produce an error ($V_{ERROR} = R \times I_L$) at the load. However, the Kelvin connection of Figure 35 overcomes the problem by including the wiring resistance within the forcing loop of the op amp. Because the op amp senses the load voltage, the op amp loop control forces the output to compensate for the wiring error and to produce the correct voltage at the load.

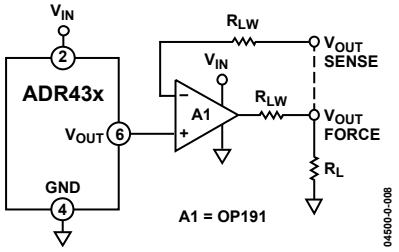

Figure 35. Advantage of Kelvin Connection

DUAL POLARITY REFERENCES

Dual polarity references can easily be made with an op amp and a pair of resistors. In order not to defeat the accuracy obtained by ADR43x, it is imperative to match the resistance tolerance as well as the temperature coefficient of all the components.

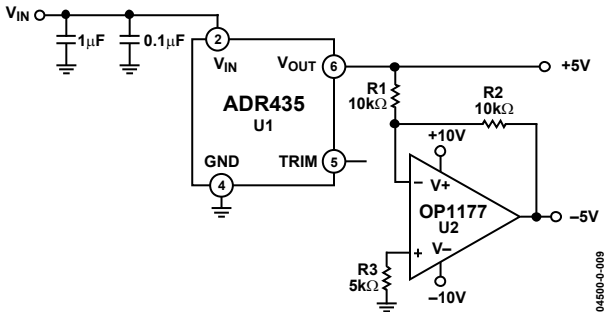

Figure 36. +5 V and –5 V References Using ADR435

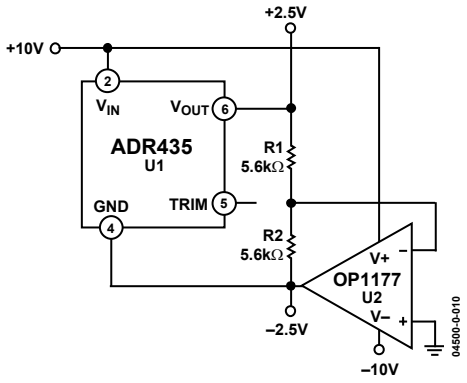

Figure 37. +2.5 V and –2.5 V References Using ADR435

PROGRAMMABLE CURRENT SOURCE

Together with a digital potentiometer and a Howland current pump, ADR435 forms the reference source for a programmable current as

$$I_L = \left(\frac{\frac{R2_A + R2_B}{R1}}{R2_B} \right) \times V_W \quad (3)$$

and

$$V_W = \frac{D}{2^N} \times V_{REF} \quad (4)$$

where:
D is the decimal equivalent of the input code.
N is the number of bits.

In addition, $R1'$ and $R2'$ must be equal to $R1$ and $R2_A + R2_B$, respectively. $R2_B$ in theory can be made as small as needed to achieve the necessary current within the A2 output current driving capability. In this example, OP2177 can deliver a maximum of 10 mA. Because the current pump employs both positive and negative feedback, capacitors C1 and C2 are needed to ensure that the negative feedback prevails and, therefore, avoids oscillation. This circuit also allows bidirectional current flow if the inputs V_A and V_B of the digital potentiometer are supplied with the dual polarity references, as shown previously.

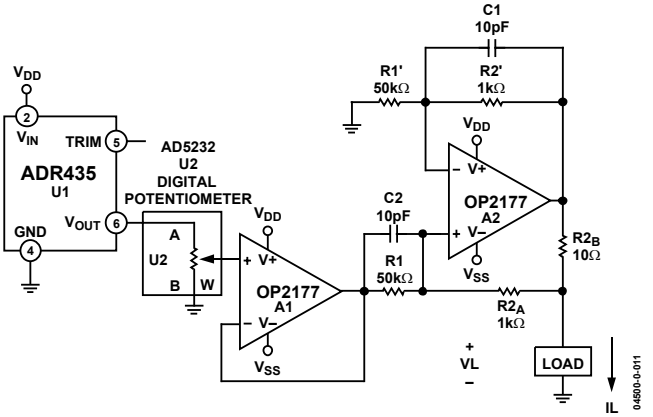

Figure 38. Programmable Current Source

PROGRAMMABLE DAC REFERENCE VOLTAGE

With a multichannel DAC such as a quad 12-bit voltage output DAC AD7398, one of its internal DACs and an ADR43x voltage reference can be used as a common programmable V_{REFX} for the rest of the DACs. The circuit configuration is shown in Figure 39.

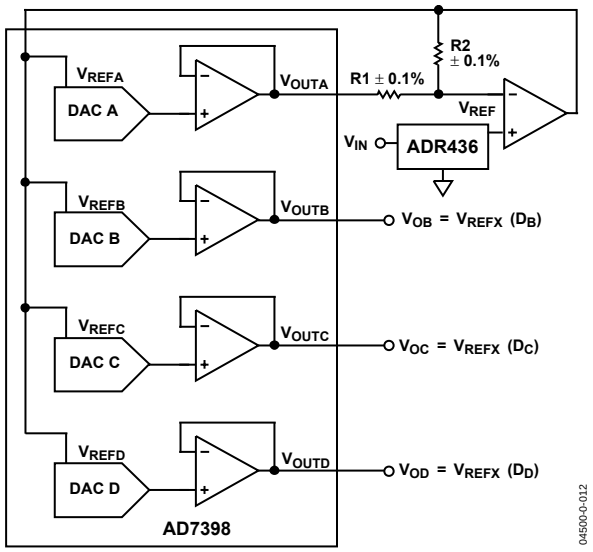

Figure 39. Programmable DAC Reference

The relationship of V_{REFX} to V_{REF} depends on the digital code and the ratio of R1 and R2, and is given by

$$V_{REFX} = \frac{V_{REF} \times \left(1 + \frac{R2}{R1}\right)}{\left(1 + \frac{D}{2^N} \times \frac{R2}{R1}\right)} \quad (5)$$

where:
D is the decimal equivalent of input code.
N is the number of bits.
V_{REF} is the applied external reference.
V_{REFX} is the reference voltage for DAC A to DAC D.

Table 10. V_{REFX} vs. R1 and R2

R1, R2	Digital Code	V_{REF}
R1 = R2	0000 0000 0000	2 V_{REF}
R1 = R2	1000 0000 0000	1.3 V_{REF}
R1 = R2	1111 1111 1111	V_{REF}
R1 = 3R2	0000 0000 0000	4 V_{REF}
R1 = 3R2	1000 0000 0000	1.6 V_{REF}
R1 = 3R2	1111 1111 1111	V_{REF}

PRECISION VOLTAGE REFERENCE FOR DATA CONVERTERS

The ADR43x family has a number of features that make it ideal for use with ADCs and DACs. The exceptional low noise, tight temperature coefficient, and high accuracy characteristics make the ADR43x ideal for low noise applications such as cellular base station applications.

Another example of ADC for which the ADR431 is well suited is the AD7701. Figure 40 shows the ADR431 used as the precision reference for this converter. The AD7701 is a 16-bit ADC with on-chip digital filtering intended for the measurement of wide dynamic range and low frequency signals such as those representing chemical, physical, or biological processes. It contains a charge-balancing (Σ-Δ) ADC, a calibration microcontroller with on-chip static RAM, a clock oscillator, and a serial communications port.

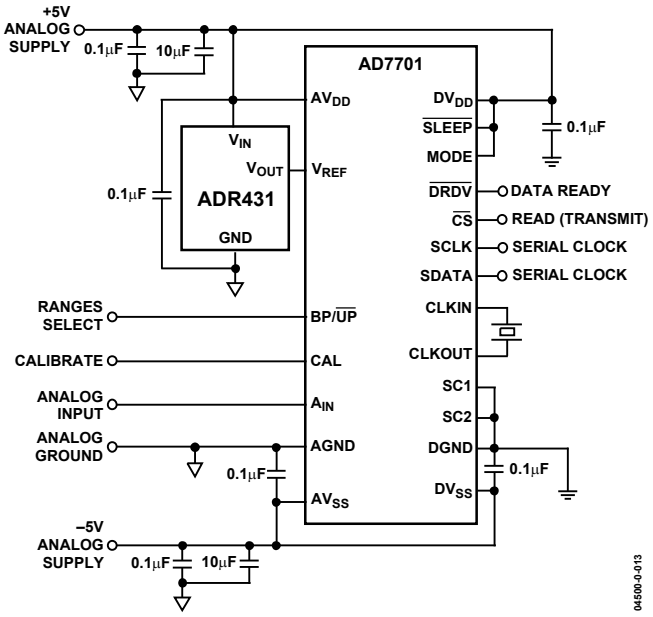

Figure 40. Voltage Reference for 16-Bit ADC AD7701

PRECISION BOOSTED OUTPUT REGULATOR

A precision voltage output with boosted current capability can be realized with the circuit shown in Figure 41. In this circuit, U2 forces V_O to be equal to V_{REF} by regulating the turn on of N1. Therefore, the load current is furnished by V_{IN}. In this configuration, a 50 mA load is achievable at V_{IN} of 5 V. Moderate heat is generated on the MOSFET, and higher current can be achieved with a replacement of the larger device. In addition, for a heavy capacitive load with step input, a buffer may be added at the output to enhance the transient response.

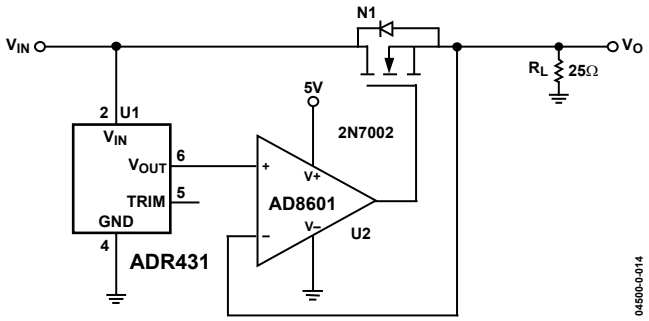

Figure 41. Precision Boosted Output Regulator

OUTLINE DIMENSIONS

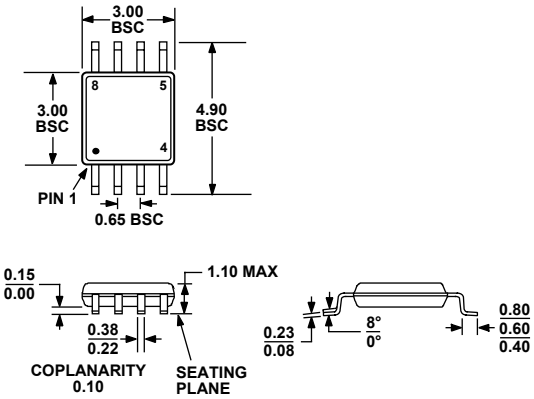

Figure 42. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

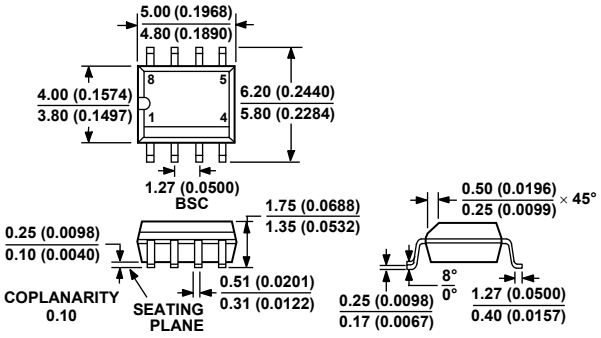

Figure 43. 8-Lead Standard Small Outline Package [SOIC]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Output Voltage (V_O)	Initial Accuracy		Temperature Coefficient Package (ppm/°C)	Package Description	Parts per Reel	Branding	Temperature Range
		mV	(%)					
ADR430AR	2.048	3	0.15	10	8-lead SOIC	N/A		–40°C to +125°C
ADR430AR-REEL7	2.048	3	0.15	10	8-Lead SOIC	3,000		–40°C to +125°C
ADR430ARM	2.048	3	0.15	10	8-Lead MSOP	N/A	RHA	–40°C to +125°C
ADR430ARM-REEL7	2.048	3	0.15	10	8-Lead MSOP	1,000	RHA	–40°C to +125°C
ADR430BR	2.048	1	0.05	3	8-lead SOIC	N/A		–40°C to +125°C
ADR430BR-REEL7	2.048	1	0.05	3	8-Lead SOIC	3,000		–40°C to +125°C
ADR431AR	2.500	3	0.12	10	8-Lead SOIC	N/A		–40°C to +125°C
ADR431AR-REEL7	2.500	3	0.12	10	8-Lead SOIC	3,000		–40°C to +125°C
ADR431ARM	2.500	3	0.12	10	8-Lead MSOP	N/A	RJA	–40°C to +125°C
ADR431ARM-REEL7	2.500	3	0.12	10	8-Lead MSOP	1,000	RJA	–40°C to +125°C
ADR431BR	2.500	1	0.04	3	8-Lead SOIC	N/A		–40°C to +125°C
ADR431BR-REEL7	2.500	1	0.04	3	8-Lead SOIC	3,000		–40°C to +125°C
ADR433AR	3.000	4	0.12	10	8-Lead SOIC	N/A		–40°C to +125°C
ADR433AR-REEL7	3.000	4	0.12	10	8-Lead SOIC	3,000		–40°C to +125°C
ADR433ARM	3.000	4	0.12	10	8-Lead MSOP	N/A	RKA	–40°C to +125°C
ADR433ARM-REEL7	3.000	4	0.12	10	8-Lead MSOP	1,000	RKA	–40°C to +125°C
ADR433BR	3.000	1.5	0.05	3	8-Lead SOIC	N/A		–40°C to +125°C
ADR433BR-REEL7	3.000	1.5	0.05	3	8-Lead SOIC	3,000		–40°C to +125°C
ADR434AR	4.096	5	0.13	10	8-Lead SOIC	N/A		–40°C to +125°C
ADR434AR-REEL7	4.096	5	0.13	10	8-Lead SOIC	3,000		–40°C to +125°C
ADR434ARM	4.096	5	0.13	10	8-Lead MSOP	N/A	RLA	–40°C to +125°C
ADR434ARM-REEL7	4.096	5	0.13	10	8-Lead MSOP	1,000	RLA	–40°C to +125°C
ADR434BR	4.096	1.5	0.04	3	8-Lead SOIC	N/A		–40°C to +125°C
ADR434BR-REEL7	4.096	1.5	0.04	3	8-Lead SOIC	3,000		–40°C to +125°C
ADR435AR	5.000	6	0.12	10	8-Lead SOIC	N/A		–40°C to +125°C
ADR435AR-REEL7	5.000	6	0.12	10	8-Lead SOIC	3,000		–40°C to +125°C
ADR435ARM	5.000	6	0.12	10	8-Lead MSOP	N/A	RMA	–40°C to +125°C
ADR435ARM-REEL7	5.000	6	0.12	10	8-Lead MSOP	1,000	RMA	–40°C to +125°C
ADR435BR	5.000	2	0.04	3	8-Lead SOIC	N/A		–40°C to +125°C
ADR435BR-REEL7	5.000	2	0.04	3	8-Lead SOIC	3,000		–40°C to +125°C
ADR439AR	4.500	5.4	0.12	10	8-Lead SOIC	N/A		–40°C to +125°C
ADR439AR-REEL7	4.500	5.4	0.12	10	8-Lead SOIC	3,000		–40°C to +125°C
ADR439ARM	4.500	5.4	0.12	10	8-Lead MSOP	N/A	RNA	–40°C to +125°C
ADR439ARM-REEL7	4.500	5.4	0.12	10	8-Lead MSOP	1,000	RNA	–40°C to +125°C
ADR439BR	4.500	2	0.04	3	8-Lead SOIC	N/A		–40°C to +125°C
ADR439BR-REEL7	4.500	2	0.04	3	8-Lead SOIC	3,000		–40°C to +125°C

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