Si3993CDV

Vishay Siliconix

Dual P-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[a]	Q_g (Typ.)
- 30	0.111 at V_{GS} = - 10 V	- 2.9	2.7 nC
	0.188 at V_{GS} = - 4.5 V	- 2.2	

FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC

Pb-free

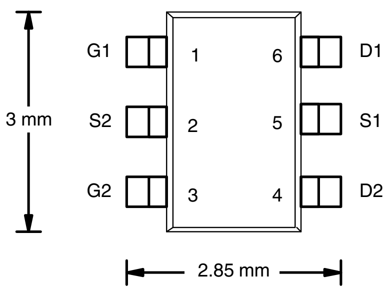
RoHS COMPLIANT

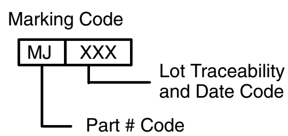
HALOGEN FREE

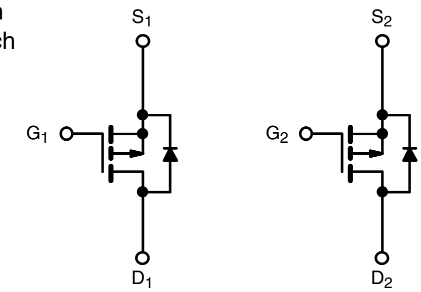
APPLICATIONS

- Load Switch for Portable Applications
- Battery Switch for Portable Devices
- Computers
  - Bus Switch
  - Load Switch

TSOP-6
Top View







P-Channel MOSFET   P-Channel MOSFET

Ordering Information: Si3993CDV-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	- 30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	- 2.9	A
	T_C = 70 °C		- 2.3	
	T_A = 25 °C		- 2.6[b, c]	
	T_A = 70 °C		- 2.1[b, c]	
Pulsed Drain Current		I_{DM}	- 8	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	- 1.17	
	T_A = 25 °C		- 0.95[b, c]	
Maximum Power Dissipation	T_C = 25 °C	P_D	1.4	W
	T_C = 70 °C		0.9	
	T_A = 25 °C		1.14[b, c]	
	T_A = 70 °C		0.73[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[b, d]	t ≤ 5 s	R_{thJA}	93	110	°C/W
Maximum Junction-to-Foot	Steady State	R_{thJF}	75	90	

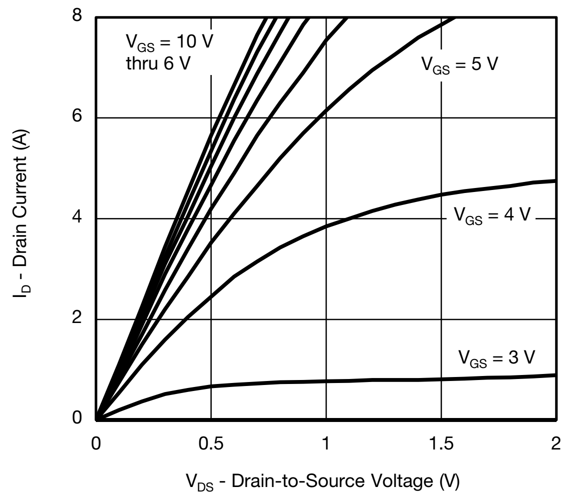
Notes:
a. T_C = 25 °C.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 5 s.
d. Maximum under steady state conditions is 150 °C/W.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = - 250 µA		- 17		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			3.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = - 250 µA	- 1.2		- 2.2	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 30 V, V_{GS} = 0 V			1	µA
		V_{DS} = - 30 V, V_{GS} = 0 V, T_J = 55 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \leq$ - 5 V, V_{GS} = - 10 V	- 8			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 10 V, I_D = - 2.5 A		0.092	0.111	Ω
		V_{GS} = - 4.5 V, I_D = - 1 A		0.156	0.188	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 15 V, I_D = - 2.6 A		5		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = - 15 V, V_{GS} = 0 V, f = 1 MHz		210		pF
Output Capacitance	C_{oss}			45		
Reverse Transfer Capacitance	C_{rss}			33		
Total Gate Charge	Q_g	V_{DS} = - 15 V, V_{GS} = - 10 V, I_D = - 2.6 A		5.2	8	nC
		V_{DS} = - 15 V, V_{GS} = - 4.5 V, I_D = - 2.6 A		2.7	4	
Gate-Source Charge	Q_{gs}			0.94		
Gate-Drain Charge	Q_{gd}			1.3		
Gate Resistance	R_g	f = 1 MHz	2	7	14	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 15 V, R_L = 7.1 Ω $I_D \cong$ - 2.1 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		39	59	ns
Rise Time	t_r			25	38	
Turn-Off Delay Time	$t_{d(off)}$			13	20	
Fall Time	t_f			9	18	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 15 V, R_L = 7.1 Ω $I_D \cong$ - 2.1 A, V_{GEN} = - 10 V, R_g = 1 Ω		5	10	
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			14	21	
Fall Time	t_f			7	14	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			1.17	A
Pulse Diode Forward Current	I_{SM}				8	
Body Diode Voltage	V_{SD}	I_S = - 2.1 A, V_{GS} = 0 V		0.85	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = - 2.1 A, dI/dt = 100 A/µs, T_J = 25 °C		13	20	ns
Body Diode Reverse Recovery Charge	Q_{rr}			6	12	nC
Reverse Recovery Fall Time	t_a			9		ns
Reverse Recovery Rise Time	t_b			4		

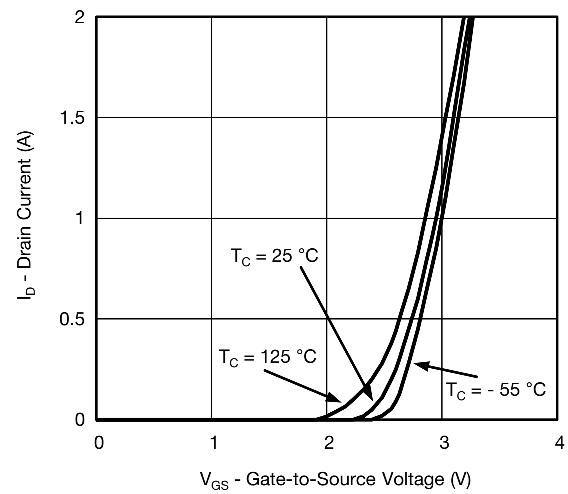
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

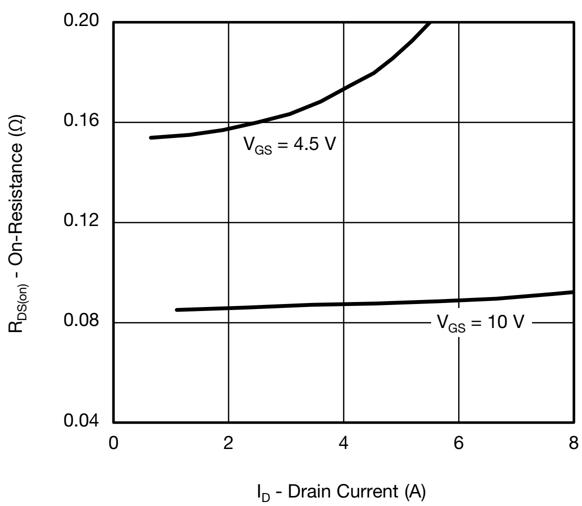
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



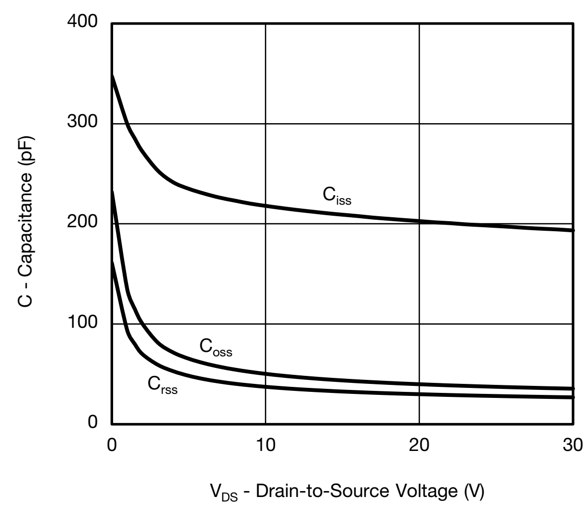
Output Characteristics



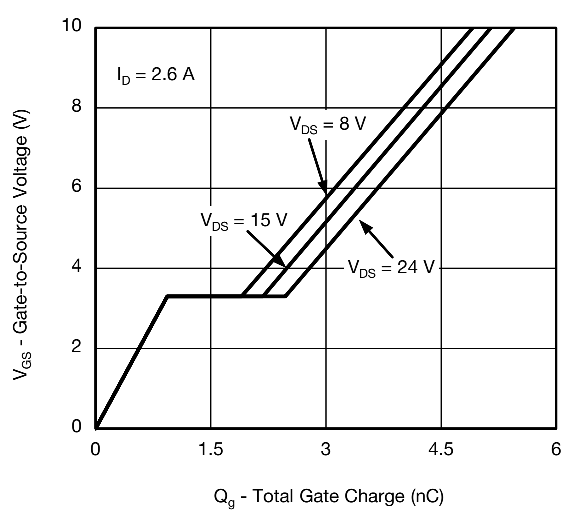
Transfer Characteristics



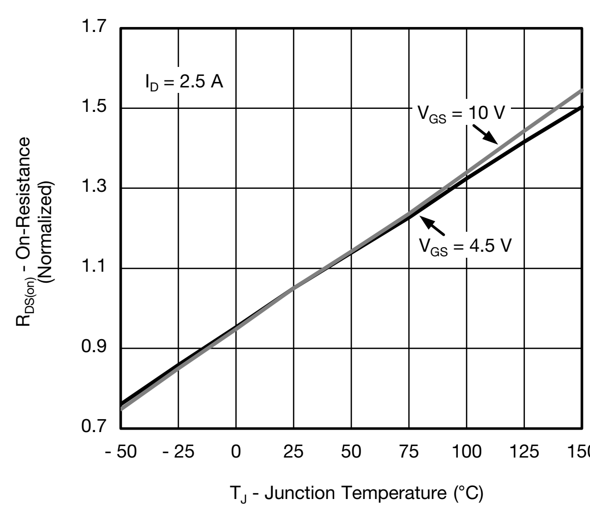
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

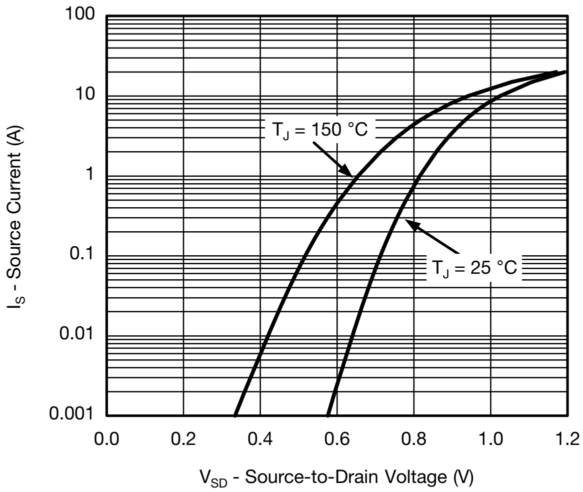


Gate Charge

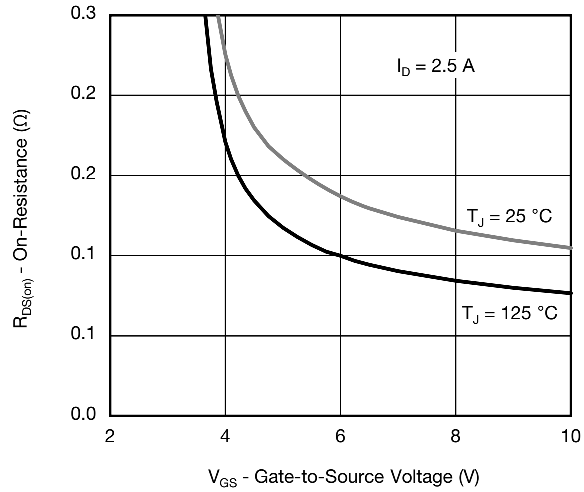


On-Resistance vs. Junction Temperature

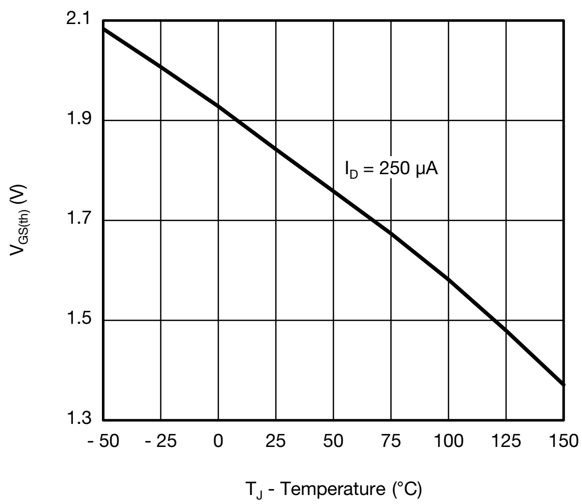
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



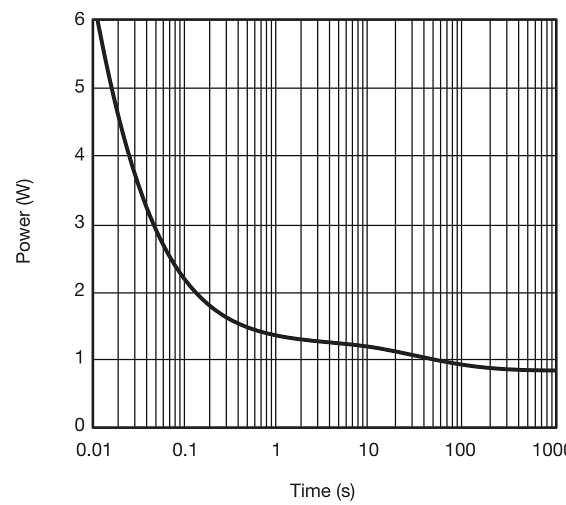
Source-Drain Diode Forward Voltage



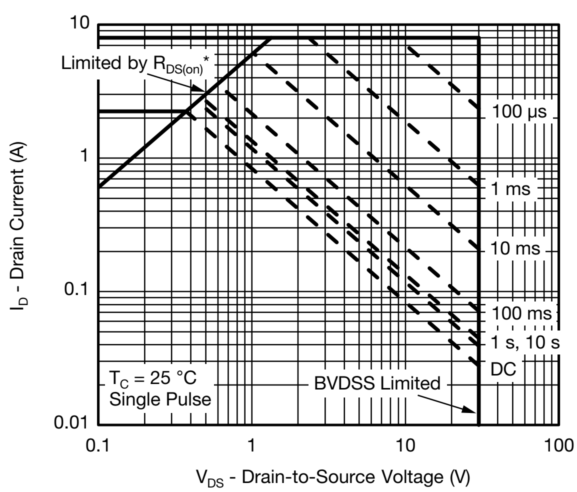
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



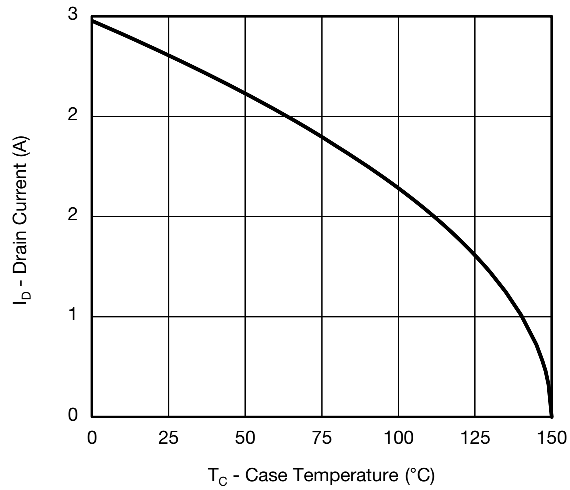
Single Pulse Power (Junction-to-Ambient)



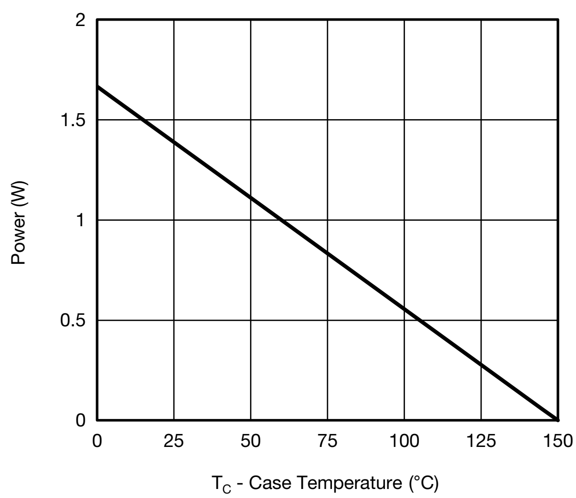
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

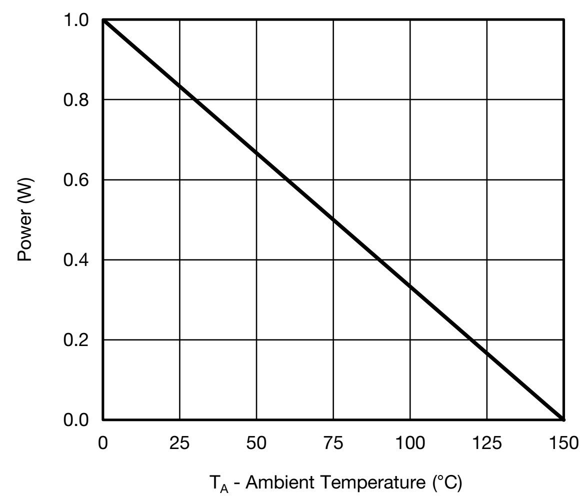
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



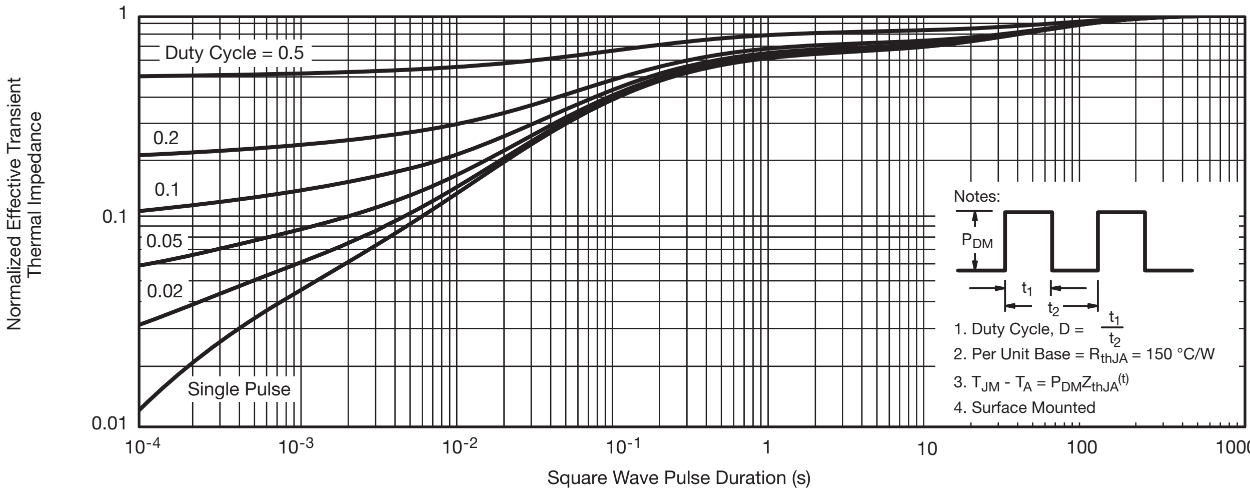
Power Derating, Junction-to-Case



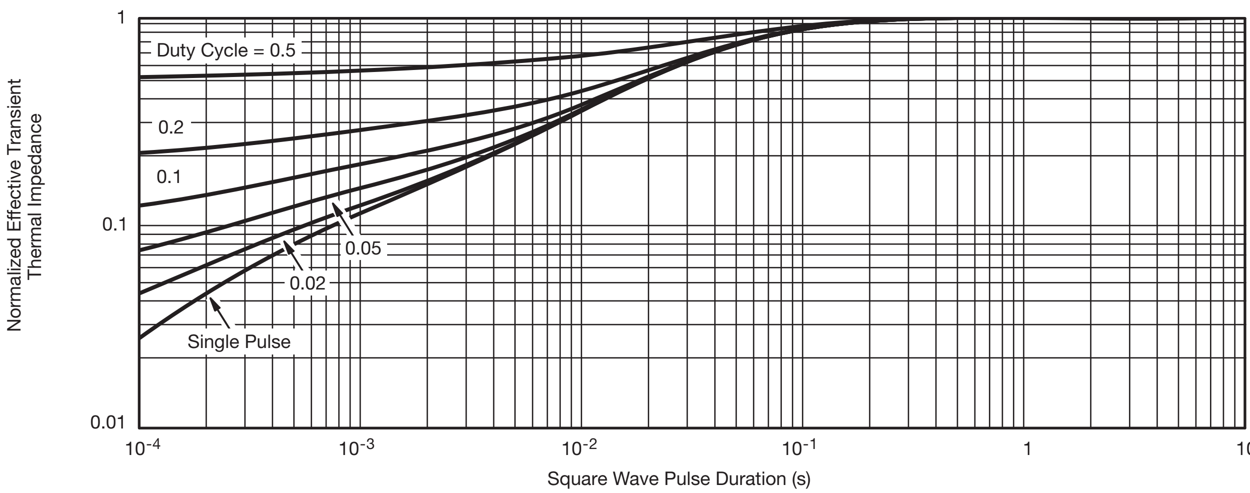
Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



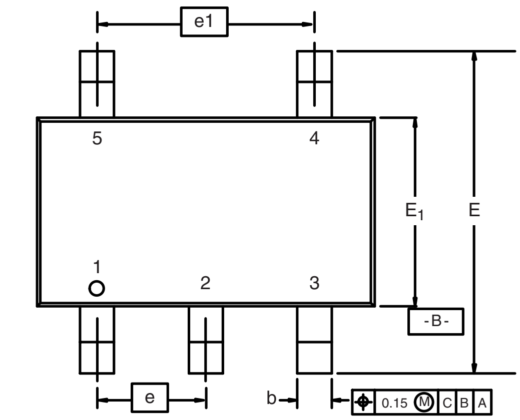
Normalized Thermal Transient Impedance, Junction-to-Ambient



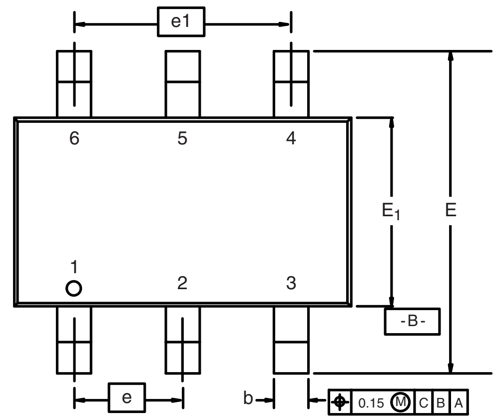
Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67331.

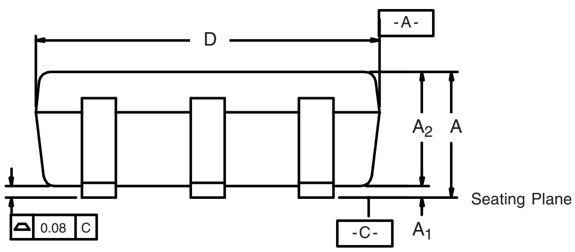
TSOP: 5/6–LEAD
JEDEC Part Number: MO-193C

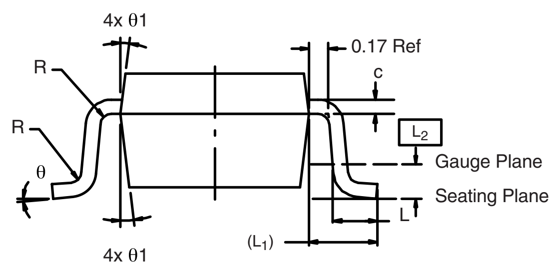


5-LEAD TSOP



6-LEAD TSOP





	MILLIMETERS			INCHES		
Dim	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	0.91	-	1.10	0.036	-	0.043
A_1	0.01	-	0.10	0.0004	-	0.004
A_2	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E_1	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e_1	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L_1	0.60 Ref			0.024 Ref		
L_2	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ_1	7° Nom			7° Nom		
ECN: C-06593-Rev. I, 18-Dec-06 DWG: 5540						

Mounting LITTLE FOOT® TSOP-6 Power MOSFETs

Surface mounted power MOSFET packaging has been based on integrated circuit and small signal packages. Those packages have been modified to provide the improvements in heat transfer required by power MOSFETs. Leadframe materials and design, molding compounds, and die attach materials have been changed. What has remained the same is the footprint of the packages.

The basis of the pad design for surface mounted power MOSFET is the basic footprint for the package. For the TSOP-6 package outline drawing see http://www.vishay.com/doc?71200 and see http://www.vishay.com/doc?72610 for the minimum pad footprint. In converting the footprint to the pad set for a power MOSFET, you must remember that not only do you want to make electrical connection to the package, but you must made thermal connection and provide a means to draw heat from the package, and move it away from the package.

In the case of the TSOP-6 package, the electrical connections are very simple. Pins 1, 2, 5, and 6 are the drain of the MOSFET and are connected together. For a small signal device or integrated circuit, typical connections would be made with traces that are 0.020 inches wide. Since the drain pins serve the additional function of providing the thermal connection to the package, this level of connection is inadequate. The total cross section of the copper may be adequate to carry the current required for the application, but it presents a large thermal impedance. Also, heat spreads in a circular fashion from the heat source. In this case the drain pins are the heat sources when looking at heat spread on the PC board.

Figure 1 shows the copper spreading recommended footprint for the TSOP-6 package. This pattern shows the starting point for utilizing the board area available for the heat spreading copper. To create this pattern, a plane of copper overlays the basic pattern on pins 1,2,5, and 6. The copper plane connects the drain pins electrically, but more importantly provides planar copper to draw heat from the drain leads and start the process of spreading the heat so it can be dissipated into the ambient air. Notice that the planar copper is shaped like a "T" to move heat away from the drain leads in all directions. This pattern uses all the available area underneath the body for this purpose.

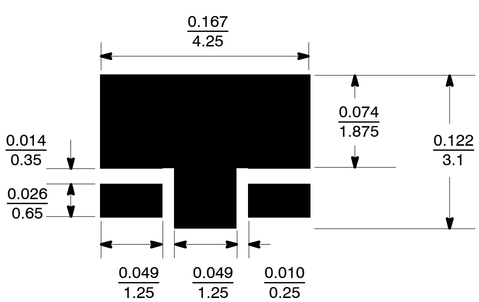


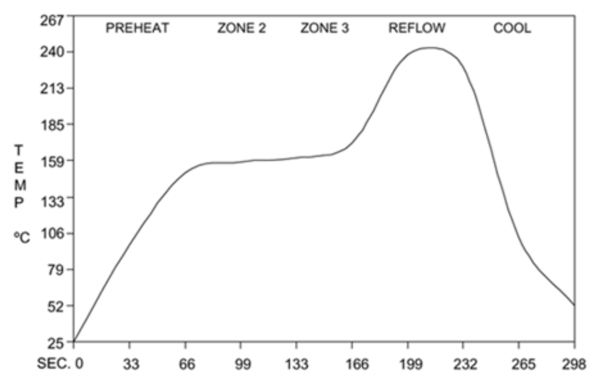
FIGURE 1. Recommended Copper Spreading Footprint

Since surface mounted packages are small, and reflow soldering is the most common form of soldering for surface mount components, "thermal" connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low impedance path for heat to move away from the device.

REFLOW SOLDERING

Vishay Siliconix surface-mount packages meet solder reflow reliability requirements. Devices are subjected to solder reflow as a test preconditioning and are then reliability-tested using temperature cycle, bias humidity, HAST, or pressure pot. The solder reflow temperature profile used, and the temperatures and time duration, are shown in Figures 2 and 3.



Ramp-Up Rate	+6°C/Second Maximum
Temperature @ 155 ± 15°C	120 Seconds Maximum
Temperature Above 180°C	70 – 180 Seconds
Maximum Temperature	240 +5/–0°C
Time at Maximum Temperature	20 – 40 Seconds
Ramp-Down Rate	+6°C/Second Maximum

FIGURE 2. Solder Reflow Temperature Profile

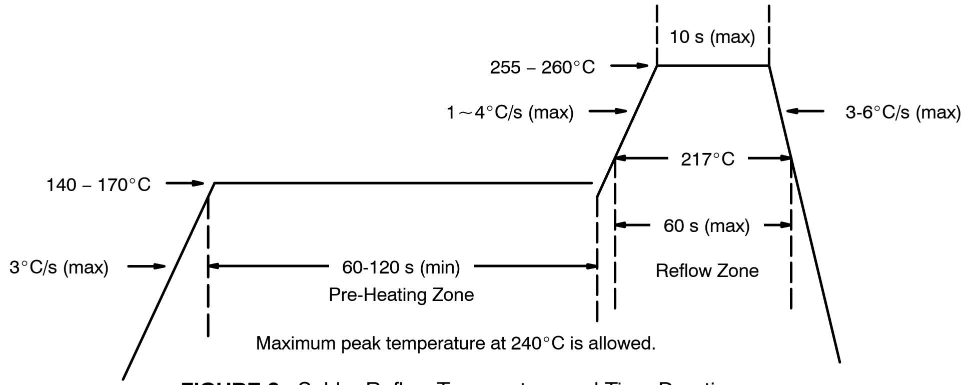


FIGURE 3. Solder Reflow Temperature and Time Durations

THERMAL PERFORMANCE

A basic measure of a device's thermal performance is the junction-to-case thermal resistance, $R\theta_{jc}$, or the junction-to-foot thermal resistance, $R\theta_{jf}$. This parameter is measured for the device mounted to an infinite heat sink and is therefore a characterization of the device only, in other words, independent of the properties of the object to which the device is mounted. Table 1 shows the thermal performance of the TSOP-6.

TABLE 1.	
Equivalent Steady State Performance—TSOP-6	
Thermal Resistance $R\theta_{jf}$	30°C/W

SYSTEM AND ELECTRICAL IMPACT OF TSOP-6

In any design, one must take into account the change in MOSFET $r_{DS(on)}$ with temperature (Figure 4).

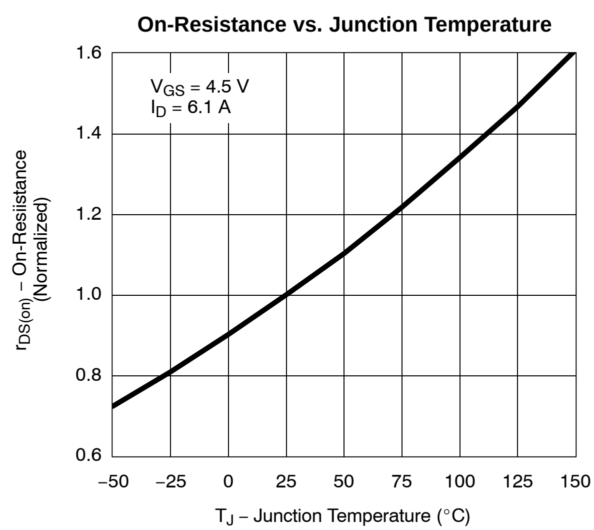
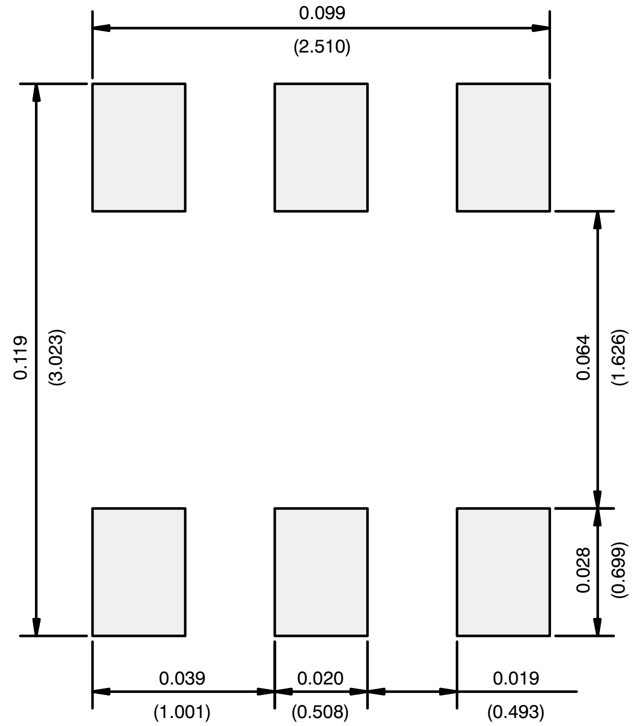


FIGURE 4. Si3434DV

RECOMMENDED MINIMUM PADS FOR TSOP-6



Recommended Minimum Pads
Dimensions in Inches/(mm)

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