

### Features and Benefits

- ☐ 128 x 1 Sensor-Element Organization (1 Not Connected, 1 dummy, 128 real,
- ☐ 1 dummy and 1 Dark Pixel)
- ☐ 385 Dots-Per-Inch (DPI) Sensor Pitch
- ☐ High Linearity and Uniformity for 256 Gray-Scale (8-Bit) Applications
- ☐ High Sensitivity:
  - ☐ 2.0V @ 10 $\mu$ W/cm<sup>2</sup> @ 0.7ms integration time for open cavity devices
  - ☐ 1.7V @ 10 $\mu$ W/cm<sup>2</sup> @ 0.7ms integration time for glass lid devices
- ☐ Special Gain Compensation for use with single LED light source
- ☐ Output Referenced to Ground
- ☐ Low Image Lag
- ☐ Single 5V Supply
- ☐ Replacement for TAOS, Inc. TSL1301 & TSL1401 and MLX90255BA
- ☐ Operation to 800kHz

### Applications

- ☐ Linear Position Encoder
- ☐ Rotary Position Encoder
- ☐ Steering Torque and Angle Sensing (EPAS, ESP)
- ☐ Spectrometer Applications
- ☐ Bio-metrical Applications
- ☐ OCR and Barcode Applications
- ☐
- ☐

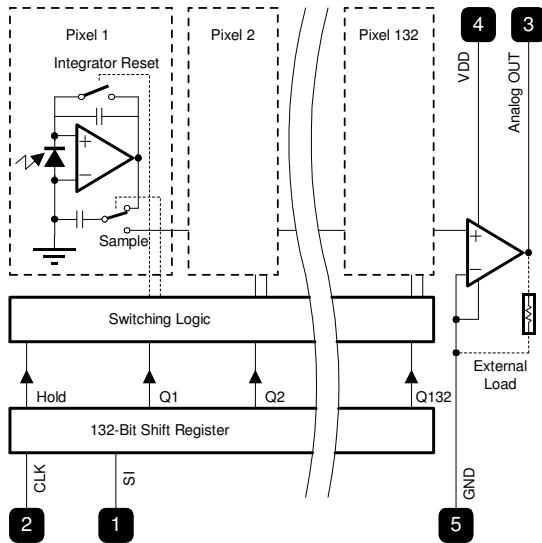
### Ordering Code

Product Code	Temperature Code	Package Code	Option Code	Packing Form Code
MLX90255	K	WB	BCM-000	TR
MLX90255	K	XA	BCR-000	RE
MLX90255	K	XA	BCR-000	TU

#### Legend:

Temperature Code: K for Temperature Range -40°C to 125°C  
 Package Code: WB for GLP5, XA for SOIC24  
 Option Code: AAA-xxx: Die version  
                   xxx-000: Standard version  
 Packing Form: RE for Reel  
                   TR for Tray  
 Ordering example: MLX90255KWB-BCM-000-TR

## 1. Functional Diagram



## 2. Description

The MLX90255BC linear sensor array consists of a 128 x 1 array of photodiodes, associated charge amplifier circuitry and a pixel data-hold function that provides simultaneous-integration start and stop times for all pixels. The pixels measure 200µm (H) by 66 µm (W). Operation is simplified by internal control logic that requires only a serial-input (SI) signal and a clock.

The sensor consists of 128 photodiodes arranged in a linear array. Light energy falling on a photodiode generates photocurrent, which is integrated by the active integration circuitry associated with that pixel. During the integration period, a sampling capacitor connects to the output of the integrator through an analog switch. The amount of charge accumulated at each pixel is directly proportional to the light intensity and the integration time. The output and reset of the integrators is controlled by a 132-bit shift register and reset logic. An output cycle is initiated by clocking in a logic 1 on SI.

*(Continued on page 6)*

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### 3. MLX90255BC Electrical Specifications

DC Operating Parameters  $T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{DD} = 4.5\text{V}$  to  $5.5\text{V}$  (unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	Vdd	4.	4.5	5	5.5	V
Input voltage	Vi	5.	0	6.	Vdd	V
High-level input voltage	Vih	7.	Vdd*0.7	8.	Vdd	V
Low-level input voltage	Vil	9.	0	10.	Vdd*0.3	V
Hysteresis on SI and CLK			0.2	0.4	0.8	V
Wavelength of light source			400	11.	1000	nm
Clock frequency	Fclock	12.	64	13.	800	kHz
Sensor integration time below $60^{\circ}\text{C}$ (1)	Tint	14.	0.125	15.	100	ms
Sensor integration time (full temperature range) (2)	Tint	16.	0.125	17.	2	ms
Pixel charge transfer time (full temp range)	Tqt	18.	8	19.	20.	$\mu\text{s}$
Setup time, serial input	Tsu(SI)	21.	350	22.	23.	ns
Hold time, serial input (3)	Th(SI)	24.	160	25.	26.	ns
Operating free-air temperature	Ta	27.	-40	28.	125	$^{\circ}\text{C}$
Clock pulse duration (high)	Tw(H)	29.	625			ns
Clock pulse duration (low)	Tw(L)	30.	625			ns

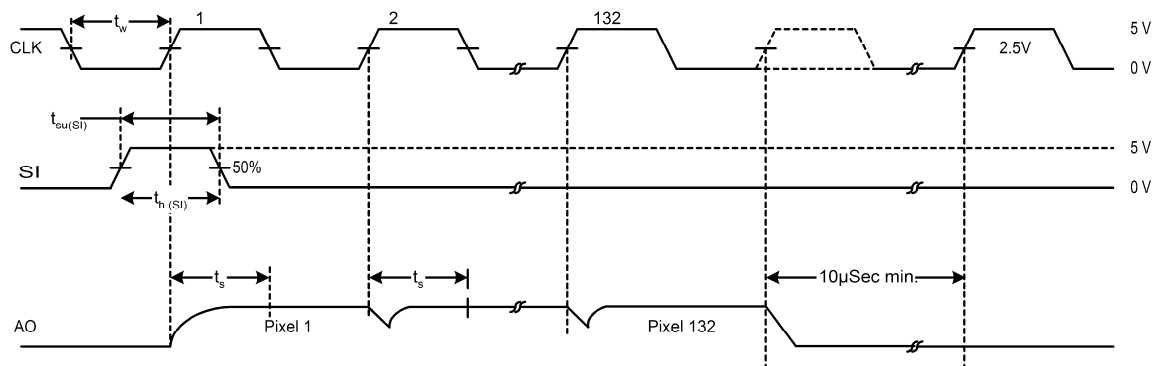
#### Notes:

(1) Reset until clock pulse 18 (on declining flank).

Minimum integration time =  $(133-18) * \text{CLK period} + 10\mu\text{s}$  (this is the time the S&H cap needs to follow).  
At 1MHz clock speed, the minimum integration time becomes 0.125ms.

(2) At  $125^{\circ}\text{C}$ , the integration time should be limited to 2ms.

(3) The SI pulse must go low before the rising edge of the next clock pulse.



### MLX90255BC Electrical specifications

All tests are made with 0.7ms integration time at 25°C at 880nm and with a clock speed of 500kHz in, 250kHz out, and 500kHz, unless otherwise specified in the Test Conditions. 100% light under Test Conditions means that the light is set in such a way that there is 2.4V at the output of the chip.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Sensitivity for devices with glas lid	Sensitivity	At 25°C	0.135	0.151	0.179	V/μW/cm <sup>2</sup>
Sensitivity for open devices			0.14	0.16	0.19	
Polyimide Wafer			0.14	0.176	0.21	
Illumination (1)	Illum100	At 25°C, 2.4V at output		14	31.	μW/cm <sup>2</sup>
Average analog output (1)	VaoLight	At 25°C, 100% light		2.4		V
Average analog output	Initial offset	At 25°C, 0% light	0	0.15	0.3	V
Average analog output	VaoDark	At 125°C, 0% light	0	0.40	1.4	V
Highest Dark Pixel	Vaodarkmax	At 125°C, 0.25ms integration time			0.8	V
Non Linearity	Nlao1	All Temp		±0.5%	±1.2%	FS
Pixel Response Non Uniformity (2)	PRNU	All Temp, 100% light		±4.0%	±8.5%	FS
Pixel Interaction Test (3)	PIT	At 25°C		5%	32.	FS
Noise Level (4)	Vn	All Temp		3	6	mV (RMS)
Hold spec, same as PRNU	PRNUH	All Temp, 100% light, 62.5kHz		±4.0%	±8.5%	FS
Output Settling Time	Ts	All Temp		450	750	ns
Array Lag (5)	Alag	At 25°C		0.5%	33.	FS
Dark Signal Non Uniformity (6)	DSNU	At 25°C		80	120	mV
		At 125°C		140	440	mV
Analog Output Saturation		All Temp	3.0			V
Change in sensitivity with Temperature at 880nm (7)				0.3	34.	%/°C
Operating Free Temp			-40	35.	125	°C
Supply Current (8)	Idd	36.	2	5	8	mA

(0) After power on, the first integration scan is not guaranteed correct. This scan is needed for initializing digital levels on chip. After a SI and 133 proper CLK signals, the system is fully initialized and all further scans are valid. The next SI will provide a valid scan.

(1) Absolute Light measurements are very test-setup dependent and should be regarded with caution. Relative measurements are possible with ±1% accuracy.

(2) PRNU is defined as the worst case deviation of any PixelValue (pixel 3 till 130) to the average light value. PixelValue = (Vout of a pixel at 100% light – Vout of same pixel at 0% light) The MLX90255BC has a cosine shaped gain: external pixels have 15% more gain than middle pixels.

(3) PIT = (Vout of pixel 132 @ 10μW – Vout of pixel 132 @ 0μW) / (Vaverage @ 10μW – Vaverage @ 0μW)

(4) Noise: We compare 5 different measurements, normalize them and then take the RMS value.

(5) Array Lag is defined as: (Vaverage 0μW1 Vaverage 0μW2) / ((Vaverage 10μW Vaverage 0μW2). Where 0μW1 is a 0% light level, 1ms after a 100% light level. (there can still be some light effects). 0μW2 is a 0% light level, 10ms after a 100% light level, which should be a true dark reference.

(6) DSNU is defined as: (max Vout of pixel i @ 0% light) - (min Vout of pixel j @ 0% light) for pixels 3 thru 130

(7) Sensitivity always increases with rising temperature.

(8) Idd is measured with Rload disconnected from the output pin.

### 4 General Description

(continued from page 2)

This causes all 132 sampling capacitors to be disconnected from their respective integrators and starts an integrator reset period. As the SI pulse is clocked through the shift register, the charge stored on the sampling capacitors is sequentially connected to a charge-coupled output amplifier that generates a voltage on the analog output AO. Two dummy pixel values are shifted out first, then the 128 actual pixel bits, followed by two additional dummy pixel bits, for a total of 132 data bits. Although there are only 132 pixels, 133 clock pulses are necessary for a complete shift out. The final pulse is used to re-initialize the shift register.

The integrator reset period ends 18 clock cycles after the SI pulse is clocked in. So the light-integration starts after the 18<sup>th</sup> CLK pulse. The light-integration ends at the next SI pulse. Between the end of the 133<sup>rd</sup> clock pulse and the next SI pulse, a minimum time of 10µs is necessary for an effective S&H function. So the minimum integration time of the MLX90255BC is  $(133 - 18) \cdot T_s + 10\mu s$  and thus dependent on clock speed. ( $T_s$  = clock period) After the 132 data bits are clocked out, the output becomes high impedance. (see figure) The AO is driven by a source follower that requires an external pulldown resistor. (typically 330Ω) The output is nominally 125mV for no light input and 2.4V for a nominal full-scale output. The pixel gain is 15% bigger at the edges than in the middle (cosine correction) in order to get a flat output when illuminating the device with a single LED light source (see also Section 6).

The MLX90255BC is intended for use in a wide variety of applications, including: image scanning, mark and code reading, optical character recognition (OCR) and contact imaging, edge detection and positioning, and optical linear and rotary encoding. The MLX90255BC is a replacement for the Texas Instruments' TSL1301 and TSL1401 parts.

### 5 Absolute Maximum Ratings

Supply Voltage, Vdd	+7V
Digital Input Current Range	-20 to 20 mA
Operating Free-Air temperature range, Ta	-40°C to 125°C (automotive compliant optical package)
Storage temperature range, Tstg	-40°C to 125°C
ESD Sensitivity (Human Body Model according to CDF-AEC-Q100-002)	2kV

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.

These are stress ratings only, and functional operation of the device at these or any other conditions

beyond those indicated under "recommended operating conditions" is not implied.  
Exposure to absolute-maximum -rated conditions for extended periods may affect device reliability.

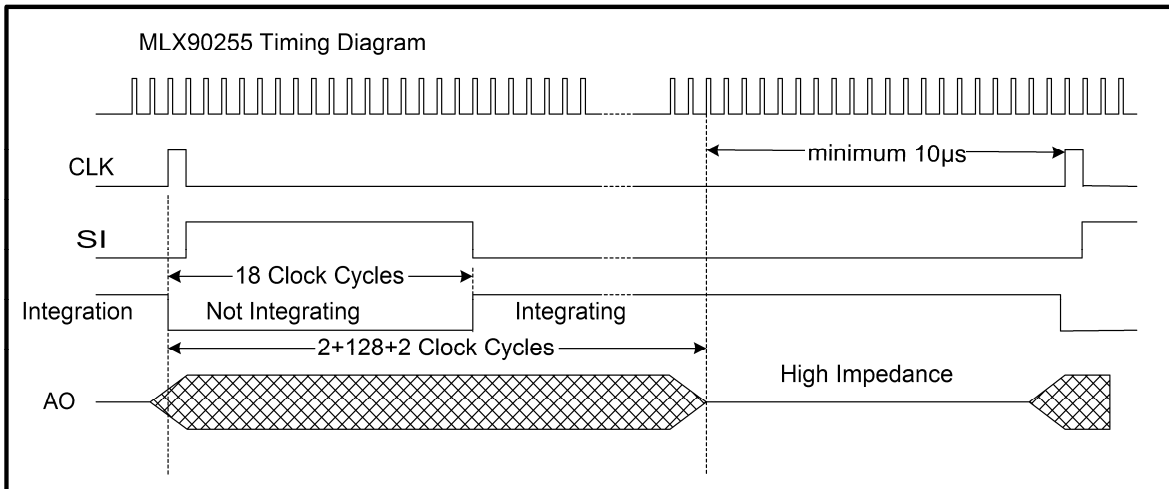
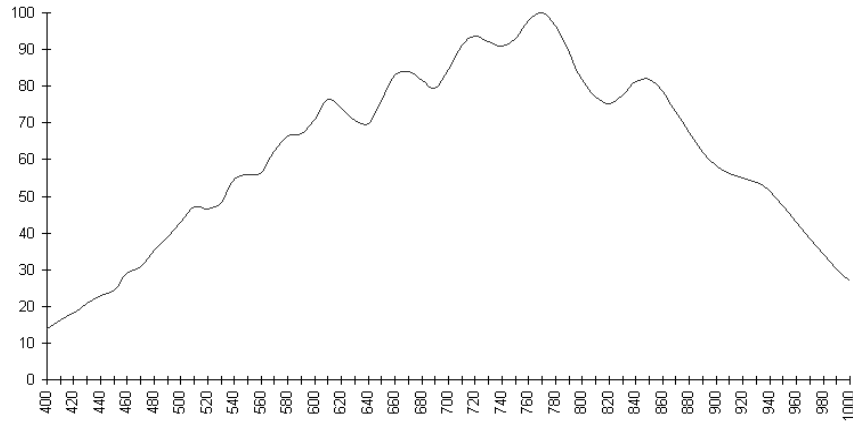
### 6 Cosine Correction

When using a single LED light source, which is placed above the middle of the die, the light intensity that falls onto the outer pixels is lower than the light intensity that falls onto the middle pixels (due to the distance die-LED, the shape of the LED light emission and the sensitivity of pixels vs. angle of incident light). To compensate for these effects, each pixel in the array has a slightly different gain correction with respect to the centre of the array. For a light source to photodiode array distance of 15mm the relative pixels sensitivities are shown in the table below.

Pixel number		Relative Pixel Sensitivity	Pixel number		Relative Pixel Sensitivity	Pixel number		Relative Pixel Sensitivity	Pixel number		Relative Pixel Sensitivity
1	132	1.1703	18	115	1.0912	35	98	1.0376	52	81	1.0076
2	131	1.1649	19	114	1.0874	36	97	1.0352	53	80	1.0066
3	130	1.1596	20	113	1.0836	37	96	1.0328	54	79	1.0056
4	129	1.1544	21	112	1.0799	38	95	1.0306	55	78	1.0047
5	128	1.1493	22	111	1.0764	39	94	1.0284	56	77	1.0039
6	127	1.1442	23	110	1.0729	40	93	1.0263	57	76	1.0031
7	126	1.1393	24	109	1.0695	41	92	1.0243	58	75	1.0025
8	125	1.1345	25	108	1.0661	42	91	1.0224	59	74	1.0019
9	124	1.1298	26	107	1.0629	43	90	1.0206	60	73	1.0014
10	123	1.1251	27	106	1.0598	44	89	1.0188	61	72	1.0010
11	122	1.1206	28	105	1.0567	45	88	1.0171	62	71	1.0006
12	121	1.1161	29	104	1.0537	46	87	1.0155	63	70	1.0003
13	120	1.1117	30	103	1.0508	47	86	1.0140	64	69	1.0002
14	119	1.1074	31	102	1.0480	48	85	1.0126	65	68	1.0000
15	118	1.1032	32	101	1.0453	49	84	1.0112	66	67	1.0000
16	117	1.0991	33	100	1.0426	50	83	1.0099			
17	116	1.0951	34	99	1.0400	51	82	1.0087			

## 7 Performance Graphs

**Typical Photodiode Spectral Response Curve (%)**





## 8 Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

### Reflow Soldering SMD's (Surface Mount Developments)

- IPC/JEDEC J-STD-020  
Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113  
Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing (reflow profiles according to table 2)

### Wave Soldering SMD's (Surface Mount Developments) and THD's (Through Hole Developments)

- EN60749-20  
Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15  
Resistance to soldering temperature for through-hole mounted devices

### Iron Soldering THD's (Through Hole Developments)

- EN60749-15  
Resistance to soldering temperature for through-hole mounted devices

### Solderability SMD's (Surface Mount Developments) and THD's (Through Hole Developments)

- EIA/JEDEC JESD22-B102 and EN60749-21  
Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis recommends reviewing on our web site the General Guidelines [soldering recommendation](http://www.melexis.com/Quality_soldering.aspx) ([http://www.melexis.com/Quality\\_soldering.aspx](http://www.melexis.com/Quality_soldering.aspx)) as well as [trim&form recommendations](http://www.melexis.com/Assets/Trim-and-form-recommendations-5565.aspx) (<http://www.melexis.com/Assets/Trim-and-form-recommendations-5565.aspx>).

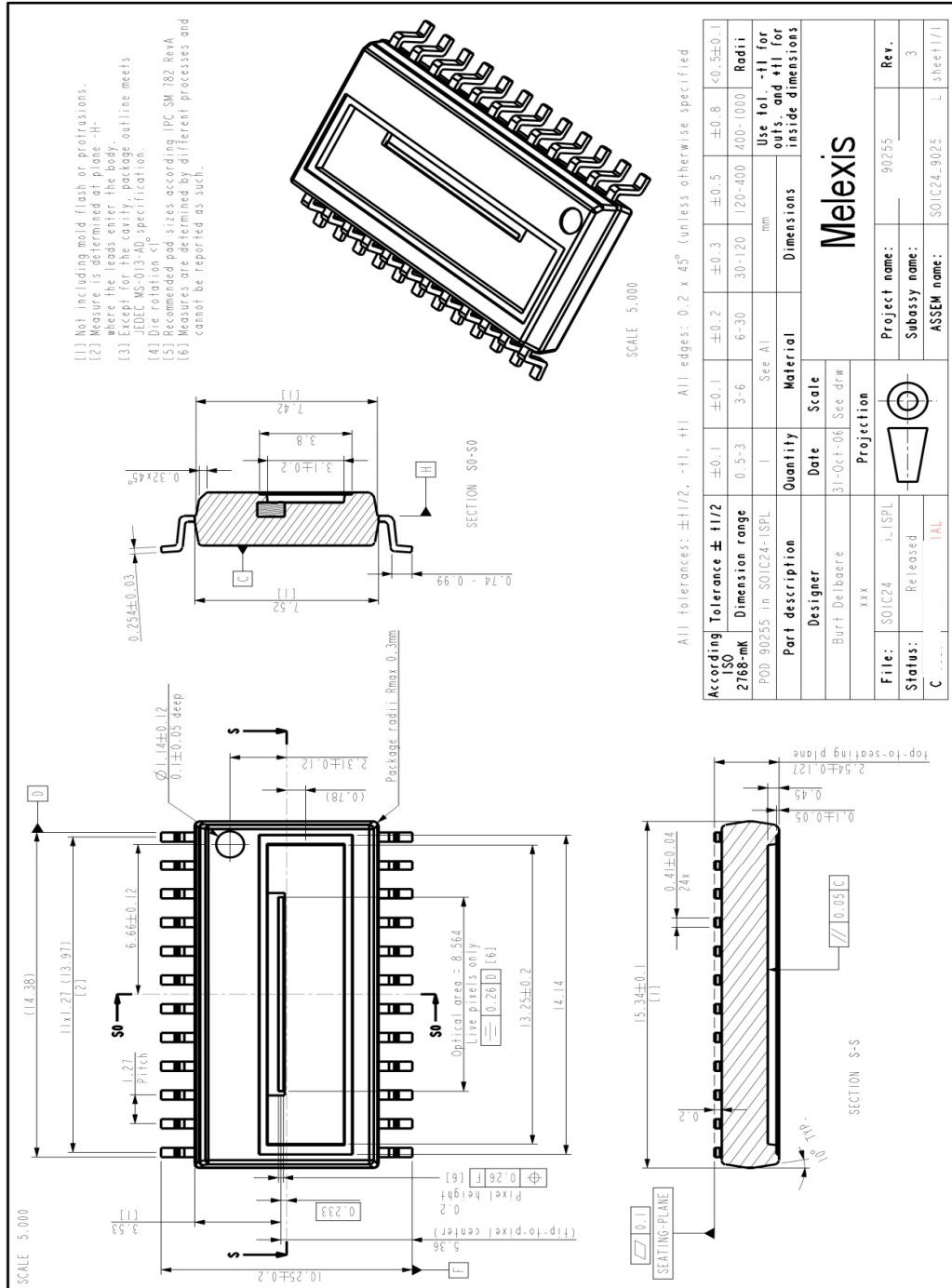
Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: <http://www.melexis.com/quality.aspx>

## 9 ESD Precautions

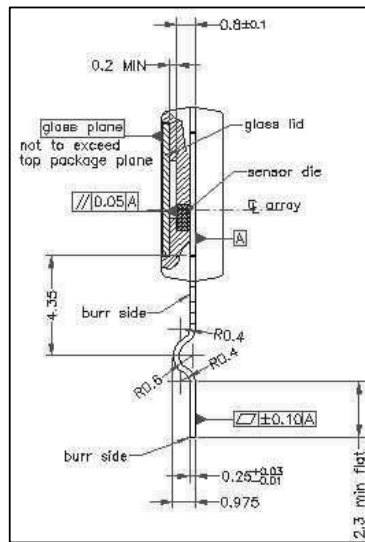
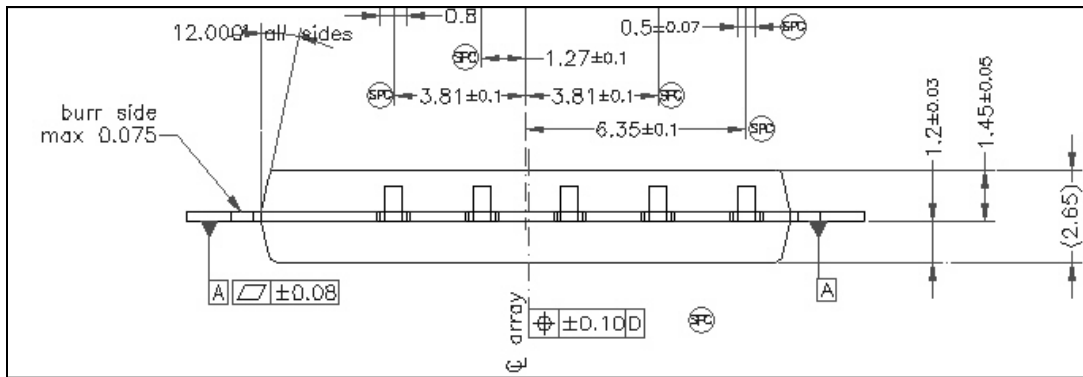
Electronic semiconductor products are sensitive to Electro Static Discharge (ESD). Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

## 10 Package Information

### a. MLX90255KXA-BCR (SOIC-24 without glass) package dimensions







## d. WB (GLP-5 with glass) Pin Description

Pin	Symbol	Description
1	SI	Serial Input. Si defines the start of the data-out sequence
2	CLK	Clock. CLK controls the charge transfer, pixel output and reset (together with SI)
3	A0	Analog Output
4	Vdd	Supply voltage, for both analog and digital circuits
5	Vss	Ground (substrate). All Vss Pins are referenced to the substrate.

## 11 Disclaimer

Devices sold by Melexis are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. Melexis makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Melexis reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with Melexis for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military,

medical life-support or life-sustaining equipment are specifically not recommended without additional processing by Melexis for each application.

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