

TCA6416 Low-Voltage 16-Bit I²C and SMBus I/O Expander With Interrupt Output, Reset, and Configuration Registers

Not Recommended for New Designs

1 Features

- Operating Power-Supply Voltage Range of 1.65 V to 5.5 V
- Allows Bidirectional Voltage-Level Translation and GPIO Expansion Between:
 - 1.8-V SCL/SDA and 1.8-V, 2.5-V, 3.3-V, or 5-V P Port
 - 2.5-V SCL/SDA and 1.8-V, 2.5-V, 3.3-V, or 5-V P Port
 - 3.3-V SCL/SDA and 1.8-V, 2.5-V, 3.3-V, or 5-V P Port
 - 5-V SCL/SDA and 1.8-V, 2.5-V, 3.3-V, or 5-V P Port
- I²C to Parallel Port Expander
- Low Standby Current Consumption of 1 μ A
- Schmitt-Trigger Action Allows Slow Input Transition and Better Switching Noise Immunity at the SCL and SDA Inputs
 - $V_{hys} = 0.18$ V Typ at 1.8 V
 - $V_{hys} = 0.25$ V Typ at 2.5 V
 - $V_{hys} = 0.33$ V Typ at 3.3 V
 - $V_{hys} = 0.5$ V Typ at 5 V
- 5-V Tolerant I/O Ports
- Active-Low Reset (RESET) Input
- Open-Drain Active-Low Interrupt (INT) Output
- 400-kHz Fast I²C Bus
- Input/Output Configuration Register

- Polarity Inversion Register
- Internal Power-On Reset
- Power Up With All Channels Configured as Inputs
- No Glitch On Power Up
- Noise Filter on SCL/SDA Inputs
- Latched Outputs With High-Current Drive Maximum Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

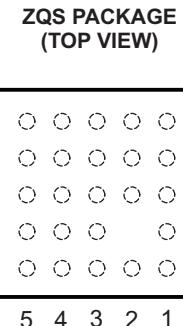
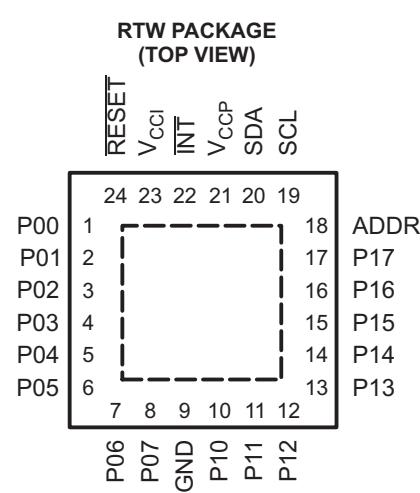
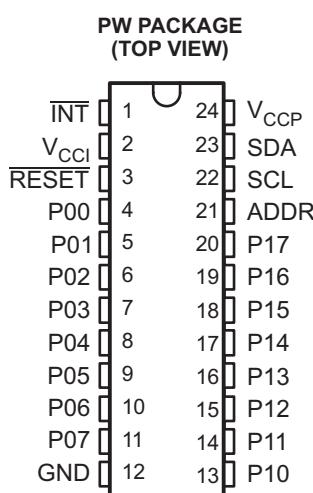
2 Description

This 16-bit I/O expander for the two-line bidirectional bus (I²C) is designed to provide general-purpose remote I/O expansion for most microcontroller families via the I²C interface [serial clock (SCL) and serial data (SDA)].

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TCA6416	TSSOP (24)	7.80 mm x 4.40 mm
	WQFN (24)	4.00 mm x 4.00 mm
	BGA (24)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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3 Revision History

Changes from Revision A (February 2009) to Revision B

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•	Added Interrupt Errata section	18

4 Description (Continued)

The major benefit of this device is its wide V_{CC} range. It can operate from 1.65 V to 5.5 V on the P-port side and on the SDA/SCL side. This allows the TCA6416 to interface with next-generation microprocessors and microcontrollers on the SDA/SCL side, where supply levels are dropping down to conserve power. In contrast to the dropping power supplies of microprocessors and microcontrollers, some PCB components, such as LEDs, remain at a 5-V power supply.

The bidirectional voltage level translation in the TCA6416 is provided through V_{CC1} . V_{CC1} should be connected to the V_{CC} of the external SCL/SDA lines. This indicates the V_{CC} level of the I²C bus to the TCA6416. The voltage level on the P-port of the TCA6416 is determined by the V_{CCP} .

The TCA6416 consists of two 8-bit Configuration (input or output selection), Input, Output, and Polarity Inversion (active high) registers. At power on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The system master can reset the TCA6416 in the event of a timeout or other improper operation by asserting a low in the $\overline{\text{RESET}}$ input. The power-on reset puts the registers in their default state and initializes the I²C/SMBus state machine. The $\overline{\text{RESET}}$ pin causes the same reset/initialization to occur without depowering the part.

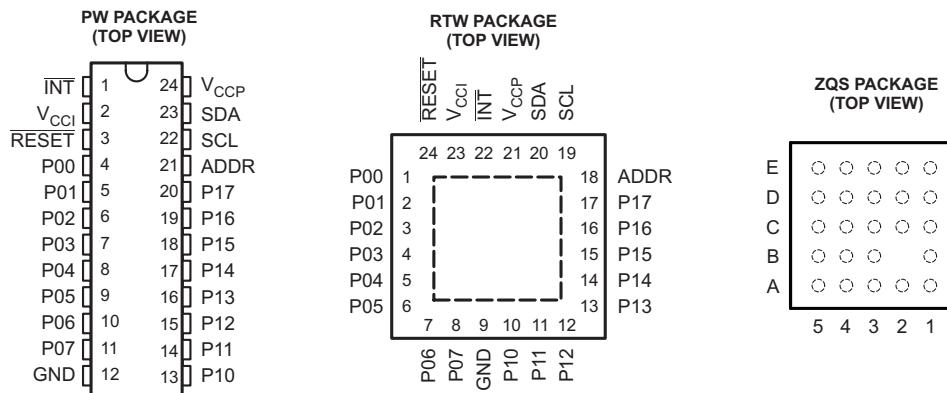
The TCA6416 open-drain interrupt ($\overline{\text{INT}}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

$\overline{\text{INT}}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C bus. Thus, the TCA6416 can remain a simple slave device.

The device P-port outputs have high-current sink capabilities for directly driving LEDs while consuming low device current.

One hardware pin (ADDR) can be used to program and vary the fixed I²C address and allow up to two devices to share the same I²C bus or SMBus.

5 Pin Configuration And Functions



Pin Functions

NAME	PIN			DESCRIPTION	
	NO.				
	TSSOP (PW)	QFN (RTW)	BGA (ZQS)		
INT	1	22	A3	Interrupt output. Connect to V _{CCI} or V _{CCP} through a pullup resistor.	
V _{CCI}	2	23	B3	Supply voltage of I ² C bus. Connect directly to the V _{CC} of the external I ² C master. Provides voltage-level translation.	
RESET	3	24	A2	Active-low reset input. Connect to V _{CCP} through a pullup resistor, if no active connection is used.	
P00	4	1	A1	P-port input/output (push-pull design structure). At power on, P00 is configured as an input.	
P01	5	2	C3	P-port input/output (push-pull design structure). At power on, P01 is configured as an input.	
P02	6	3	B1	P-port input/output (push-pull design structure). At power on, P02 is configured as an input.	
P03	7	4	C1	P-port input/output (push-pull design structure). At power on, P03 is configured as an input.	
P04	8	5	C2	P-port input/output (push-pull design structure). At power on, P04 is configured as an input.	
P05	9	6	D1	P-port input/output (push-pull design structure). At power on, P05 is configured as an input.	
P06	10	7	E1	P-port input/output (push-pull design structure). At power on, P06 is configured as an input.	
P07	11	8	D2	P-port input/output (push-pull design structure). At power on, P07 is configured as an input.	
GND	12	9	E2	Ground	
P10	13	10	E3	P-port input/output (push-pull design structure). At power on, P10 is configured as an input.	
P11	14	11	E4	P-port input/output (push-pull design structure). At power on, P11 is configured as an input.	
P12	15	12	D3	P-port input/output (push-pull design structure). At power on, P12 is configured as an input.	
P13	16	13	E5	P-port input/output (push-pull design structure). At power on, P13 is configured as an input.	
P14	17	14	D4	P-port input/output (push-pull design structure). At power on, P14 is configured as an input.	
P15	18	15	D5	P-port input/output (push-pull design structure). At power on, P15 is configured as an input.	
P16	19	16	C5	P-port input/output (push-pull design structure). At power on, P16 is configured as an input.	
P17	20	17	C4	P-port input/output (push-pull design structure). At power on, P17 is configured as an input.	
ADDR	21	18	B5	Address input. Connect directly to V _{CCP} or ground.	
SCL	22	19	A5	Serial clock bus. Connect to V _{CCI} through a pullup resistor.	
SDA	23	20	A4	Serial data bus. Connect to V _{CCI} through a pullup resistor.	
V _{CCP}	24	21	B4	Supply voltage of TCA6416 for P port	

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V_{CCI}	Supply voltage range			-0.5	6.5	V
V_{CCP}	Supply voltage range			-0.5	6.5	V
V_I	Input voltage range ⁽²⁾			-0.5	6.5	V
V_O	Output voltage range ⁽²⁾			-0.5	6.5	V
I_{IK}	Input clamp current	ADDR, $\overline{\text{RESET}}$, SCL	$V_I < 0$		± 20	mA
I_{OK}	Output clamp current	INT	$V_O < 0$		± 20	mA
I_{IOK}	Input/output clamp current	P port	$V_O < 0$ or $V_O > V_{CCP}$		± 20	mA
		SDA	$V_O < 0$ or $V_O > V_{CCI}$		± 20	
I_{OL}	Continuous output low current	P port	$V_O = 0$ to V_{CCP}		25	mA
		SDA, $\overline{\text{INT}}$	$V_O = 0$ to V_{CCI}		15	
I_{OH}	Continuous output high current	P port	$V_O = 0$ to V_{CCP}		25	mA
I_{CC}	Continuous current through GND				200	mA
	Continuous current through V_{CCP}				160	
	Continuous current through V_{CCI}				10	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		-65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CCI}	Supply voltage		1.65	5.5	V
V_{CCP}	Supply voltage		1.65	5.5	
V_{IH}	High-level input voltage	SCL, SDA	$0.7 \times V_{CCI}$	5.5	V
		ADDR, P17–P00, $\overline{\text{RESET}}$	$0.7 \times V_{CCP}$	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	-0.5	$0.3 \times V_{CCI}$	V
		ADDR, P17–P00, $\overline{\text{RESET}}$	-0.5	$0.3 \times V_{CCP}$	
I_{OH}	High-level output current	P17–P00		10	mA
I_{OL}	Low-level output current	P17–P00		25	mA
T_A	Operating free-air temperature		-40	85	°C
θ_{JA}	Package thermal impedance ⁽¹⁾	PW package		88	°C/W
		RTW package		66	
		ZQS package		171.6	

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

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6.4 Electrical Characteristics

over recommended operating free-air temperature range, $V_{CC1} = 1.65\text{ V}$ to 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCP}	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK}	Input diode clamp voltage	$I_I = -18\text{ mA}$	1.65 V to 5.5 V	-1.2			V
V_{POR}	Power-on reset voltage	$V_I = V_{CCP}$ or GND, $I_O = 0$	1.65 V to 5.5 V	1	1.4		V
V_{OH}	P-port high-level output voltage	$I_{OH} = -8\text{ mA}$	1.65 V	1.2			V
			2.3 V	1.8			
			3 V	2.6			
			4.5 V	4.1			
		$I_{OH} = -10\text{ mA}$	1.65 V	1			
			2.3 V	1.7			
			3 V	2.5			
			4.5 V	4.0			
			1.65 V	0.45			
			2.3 V	0.25			
V_{OL}	P-port low-level output voltage	$I_{OL} = 8\text{ mA}$	3 V	0.25			V
			4.5 V	0.23			
			1.65 V	0.6			
			2.3 V	0.3			
		$I_{OL} = 10\text{ mA}$	3 V	0.25			
			4.5 V	0.24			
			1.65 V to 5.5 V	3			
			1.65 V to 5.5 V	3	15		
I_I	SCL, SDA	$V_I = V_{CC1}$ or GND	1.65 V to 5.5 V		± 0.1		μA
	ADDR, $\overline{\text{RESET}}$	$V_I = V_{CCP}$ or GND	1.65 V to 5.5 V		± 0.1		
I_{IH}	P port	$V_I = V_{CCP}$	1.65 V to 5.5 V		1	μA	
I_{IL}	P port	$V_I = \text{GND}$	1.65 V to 5.5 V		1	μA	
I_{CC} ($I_{CC1} + I_{CCP}$)	SDA, P port, ADDR, $\overline{\text{RESET}}$	V_I on SDA = V_{CC1} or GND, V_I on P port, ADDR and $\overline{\text{RESET}} = V_{CCP}$, $I_O = 0$, I/O = inputs, $f_{SCL} = 400\text{ kHz}$	1.65 V to 5.5 V		7.8	30	μA
	SDA, P port, ADDR, $\overline{\text{RESET}}$	V_I on SDA = V_{CC1} or GND, V_I on P port, ADDR and $\overline{\text{RESET}} = V_{CCP}$, $I_O = 0$, I/O = inputs, $f_{SCL} = 100\text{ kHz}$	1.65 V to 5.5 V		1.7	10	
	SCL, SDA, P port, ADDR, $\overline{\text{RESET}}$	V_I on SCL and SDA = V_{CC1} or GND, V_I on P port, ADDR and $\overline{\text{RESET}} = V_{CCP}$, $I_O = 0$, I/O = inputs, $f_{SCL} = 0$	1.65 V to 5.5 V		0.1	2	
ΔI_{CC1} ΔI_{CCP}	SCL, SDA	One input at $V_{CC1} - 0.6\text{ V}$, Other inputs at V_{CC1} or GND	1.65 V to 5.5 V		25		μA
	P port, ADDR, $\overline{\text{RESET}}$	One input at $V_{CCP} - 0.6\text{ V}$, Other inputs at V_{CCP} or GND	1.65 V to 5.5 V		60		
C_I	SCL	$V_I = V_{CC1}$ or GND	1.65 V to 5.5 V		6	7	pF
C_{io}	SDA	$V_{IO} = V_{CC1}$ or GND	1.65 V to 5.5 V		7	8	pF
	P port	$V_{IO} = V_{CCP}$ or GND	1.65 V to 5.5 V		7.5	8.5	

(1) Except for I_{CC} , all typical values are at nominal supply voltage (1.8-V, 2.5-V, 3.3-V, or 5-V V_{CC}) and $T_A = 25^\circ\text{C}$. For I_{CC} , the typical values are at $V_{CCP} = V_{CC1} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$.

6.5 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 14](#))

		STANDARD MODE I ² C BUS		FAST MODE I ² C BUS		UNIT
		MIN	MAX	MIN	MAX	
t_{scl}	I ² C clock frequency	0	100	0	400	kHz
t_{sch}	I ² C clock high time	4		0.6		μs
t_{scl}	I ² C clock low time	4.7		1.3		μs
t_{sp}	I ² C spike time	0	50	0	50	ns
t_{sds}	I ² C serial data setup time	250		100		ns
t_{sdh}	I ² C serial data hold time	0		0		ns
t_{icr}	I ² C input rise time		1000	$20 + 0.1C_b$ ⁽¹⁾	300	ns
t_{icf}	I ² C input fall time		300	$20 + 0.1C_b$ ⁽¹⁾	300	ns
t_{ocf}	I ² C output fall time; 10 pF to 400 pF bus		300	$20 + 0.1C_b$ ⁽¹⁾	300	μs
t_{buf}	I ² C bus free time between Stop and Start	4.7		1.3		μs
t_{sts}	I ² C Start or repeater Start condition setup time	4.7		0.6		μs
t_{sth}	I ² C Start or repeater Start condition hold time	4		0.6		μs
t_{sps}	I ² C Stop condition setup time	4		0.6		μs
$t_{vd(data)}$	Valid data time; SCL low to SDA output valid		1		1	μs
$t_{vd(ack)}$	Valid data time of ACK condition; ACK signal from SCL low to SDA (out) low		1		1	μs

(1) C_b = total capacitance of one bus line in pF

6.6 Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 17](#))

		STANDARD MODE I ² C BUS		FAST MODE I ² C BUS		UNIT
		MIN	MAX	MIN	MAX	
t_W	Reset pulse duration	4		4		ns
t_{REC}	Reset recovery time	0		0		ns
t_{RESET}	Time to reset ⁽¹⁾	600		600		ns

(1) Minimum time for SDA to become high or minimum time to wait before doing a START

6.7 Switching Characteristics

over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted) (see [Figure 14](#))

PARAMETER	FROM	TO	STANDARD MODE I ² C BUS		FAST MODE I ² C BUS		UNIT
			MIN	MAX	MIN	MAX	
t_{IV}	Interrupt valid time	P port	\overline{INT}		4		4
t_{IR}	Interrupt reset delay time	SCL	\overline{INT}		4		4
t_{PV}	Output data valid	SCL	P7–P0		400		400
t_{PS}	Input data setup time	P port	SCL	0		0	ns
t_{PH}	Input data hold time	P port	SCL	300		300	ns

6.8 Typical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

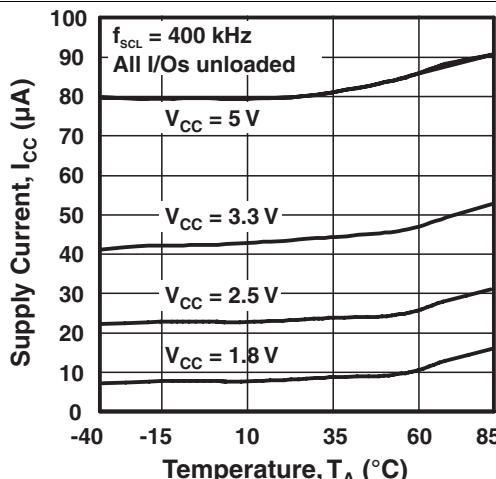


Figure 1. Supply Current vs Temperature

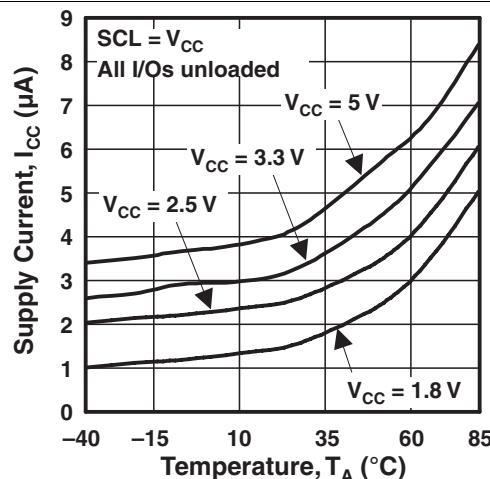


Figure 2. Standby Supply Current vs Temperature

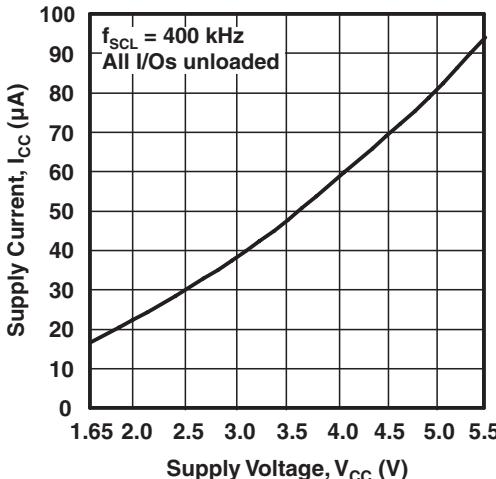


Figure 3. Supply Current vs Supply Voltage

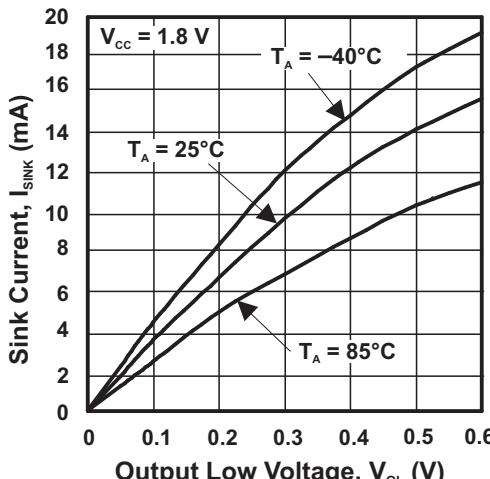


Figure 4. I/O Sink Current vs Output Low Voltage

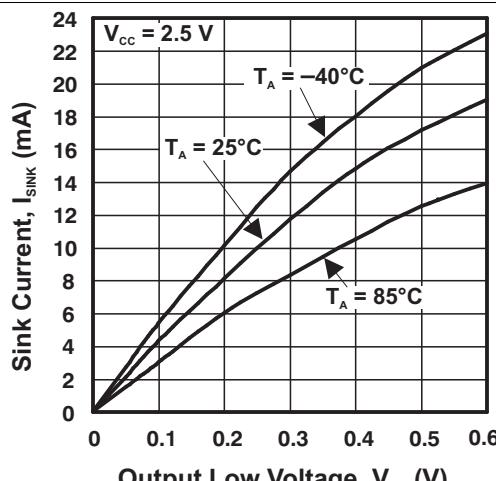


Figure 5. I/O Sink Current vs Output Low Voltage

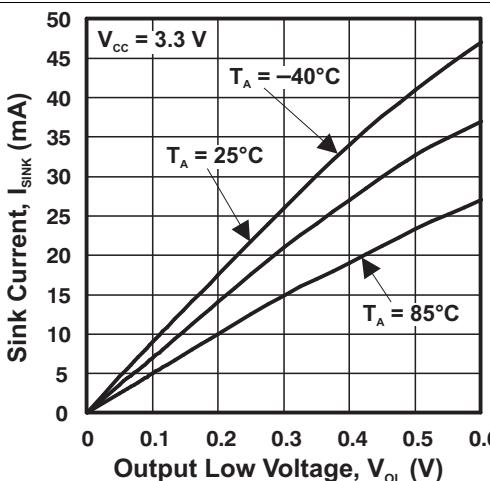


Figure 6. I/O Sink Current vs Output Low Voltage

Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

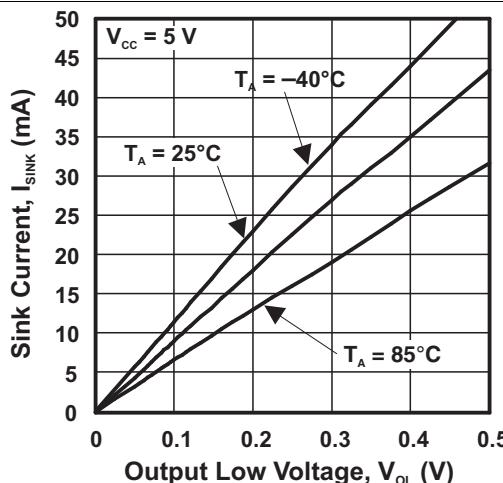


Figure 7. I/O Sink Current vs Output Low Voltage

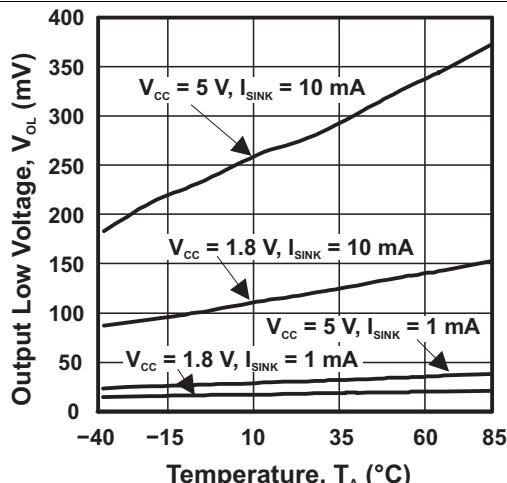


Figure 8. I/O Low Voltage vs Temperature

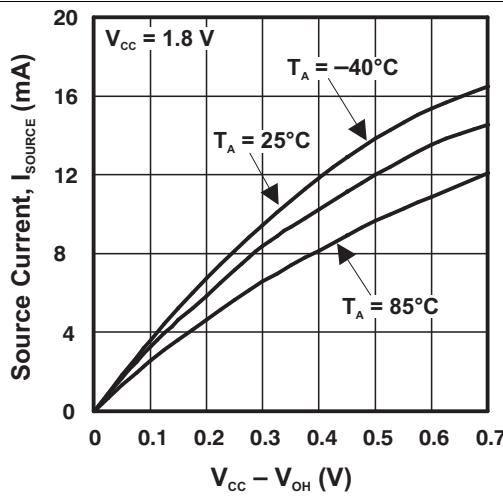


Figure 9. I/O Source Current vs Output High Voltage

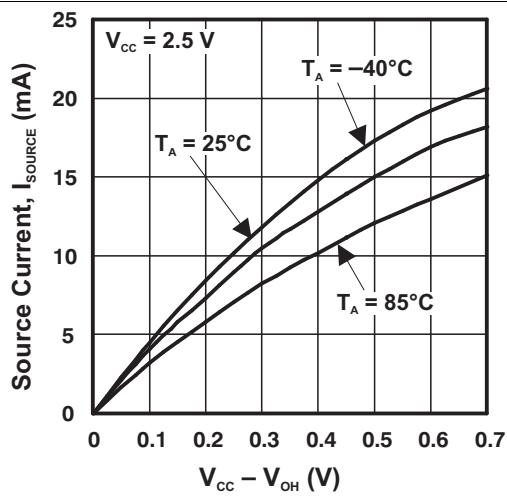


Figure 10. I/O Source Current vs Output High Voltage

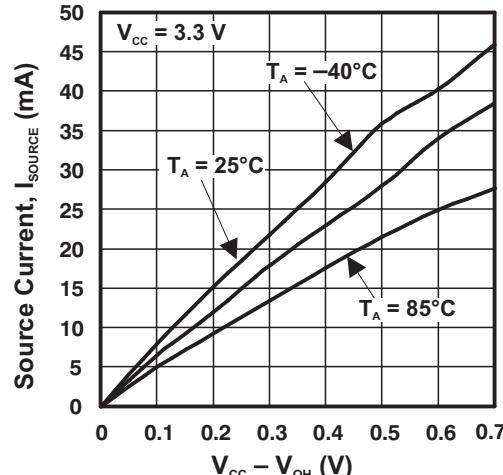


Figure 11. I/O Source Current vs Output High Voltage

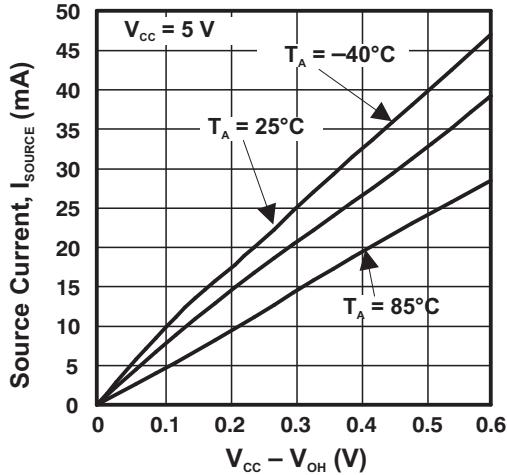


Figure 12. I/O Source Current vs Output High Voltage

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Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

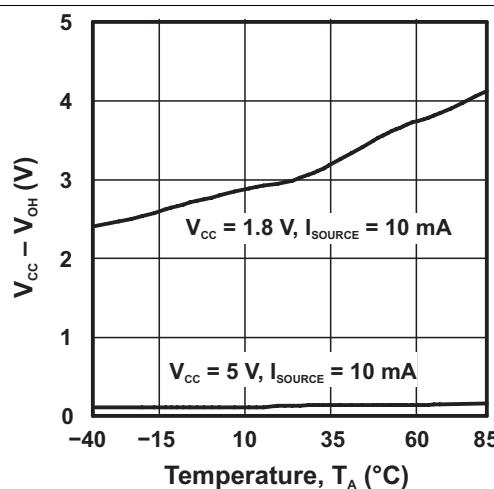
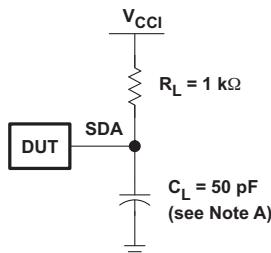
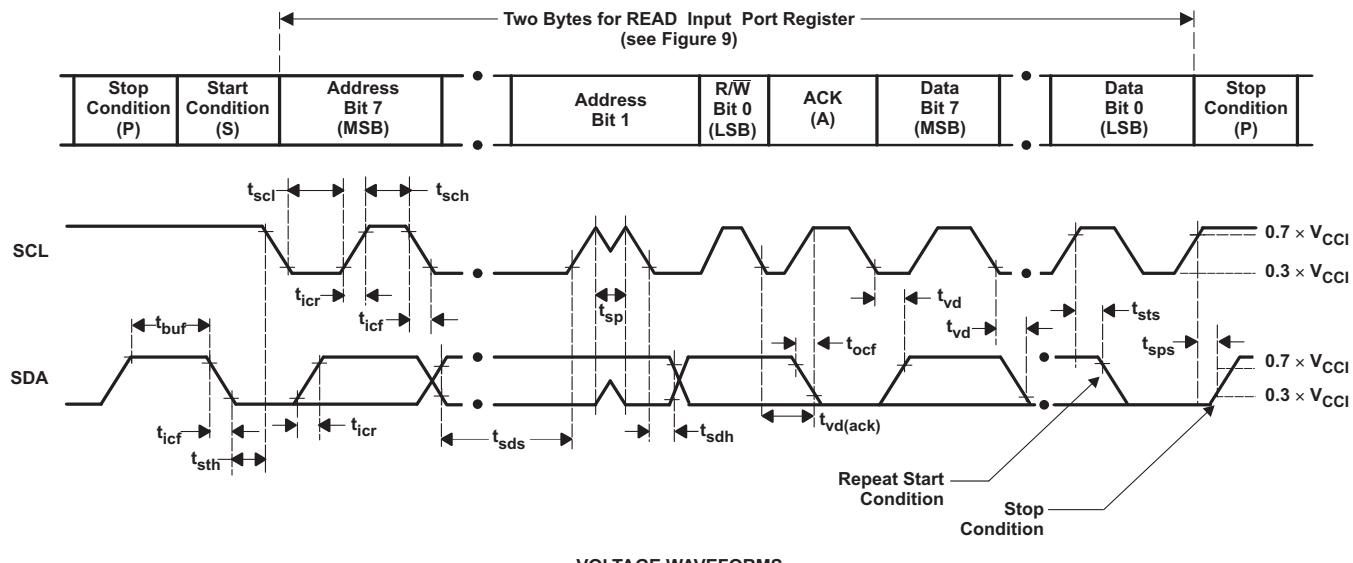


Figure 13. I/O High Voltage vs Temperature

7 Parameter Measurement Information



SDA LOAD CONFIGURATION

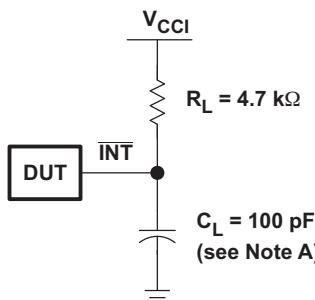


BYTE	DESCRIPTION
1	I ² C address
2	Input register port data

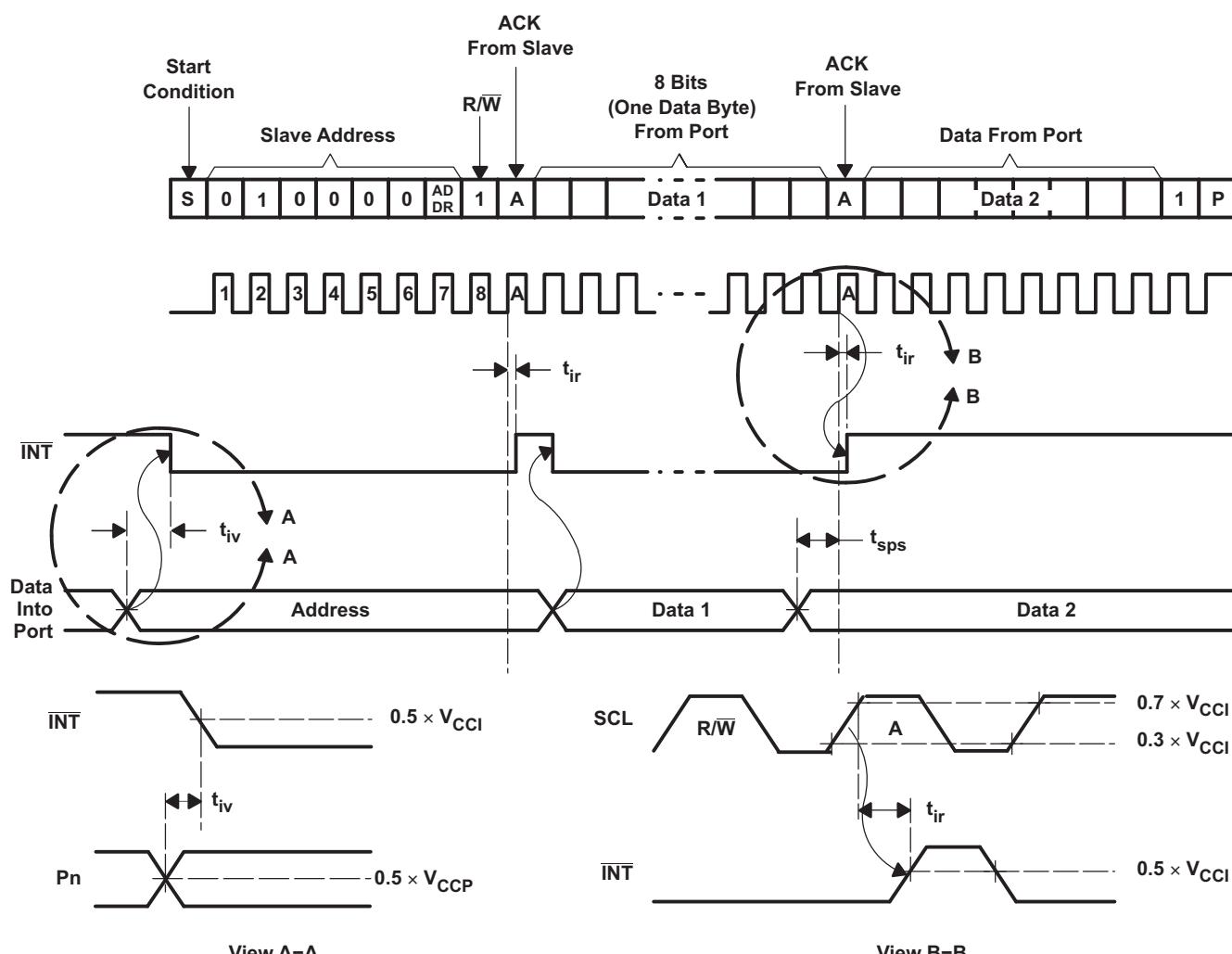
- A. C_L includes probe and jig capacitance. t_{ocf} is measured with C_L of 10 pF or 400 pF.
- B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50\Omega$, $t_f/t_r \leq 30$ ns.
- C. All parameters and waveforms are not applicable to all devices.

Figure 14. I²C Interface Load Circuit And Voltage Waveforms

Parameter Measurement Information (continued)

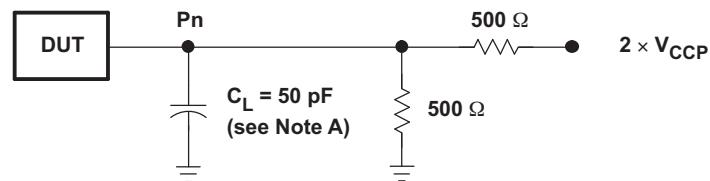
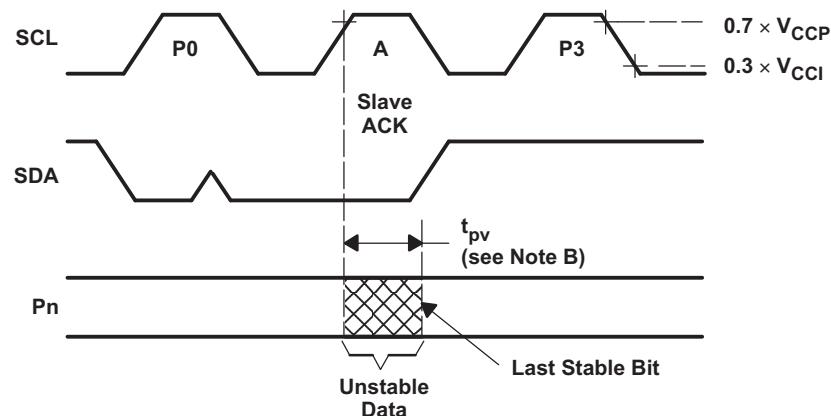
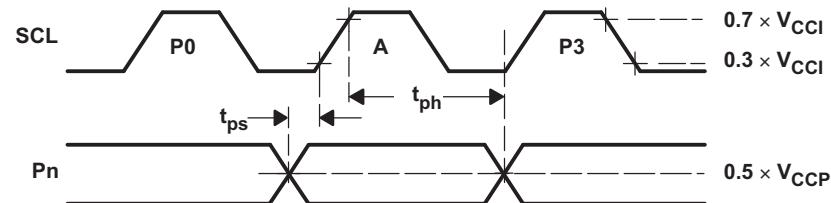


INTERRUPT LOAD CONFIGURATION



- A. C_L includes probe and jig capacitance.
 B. All inputs are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_0 = 50 \Omega$, $t_r/t_f \leq 30 \text{ ns}$.
 C. All parameters and waveforms are not applicable to all devices.

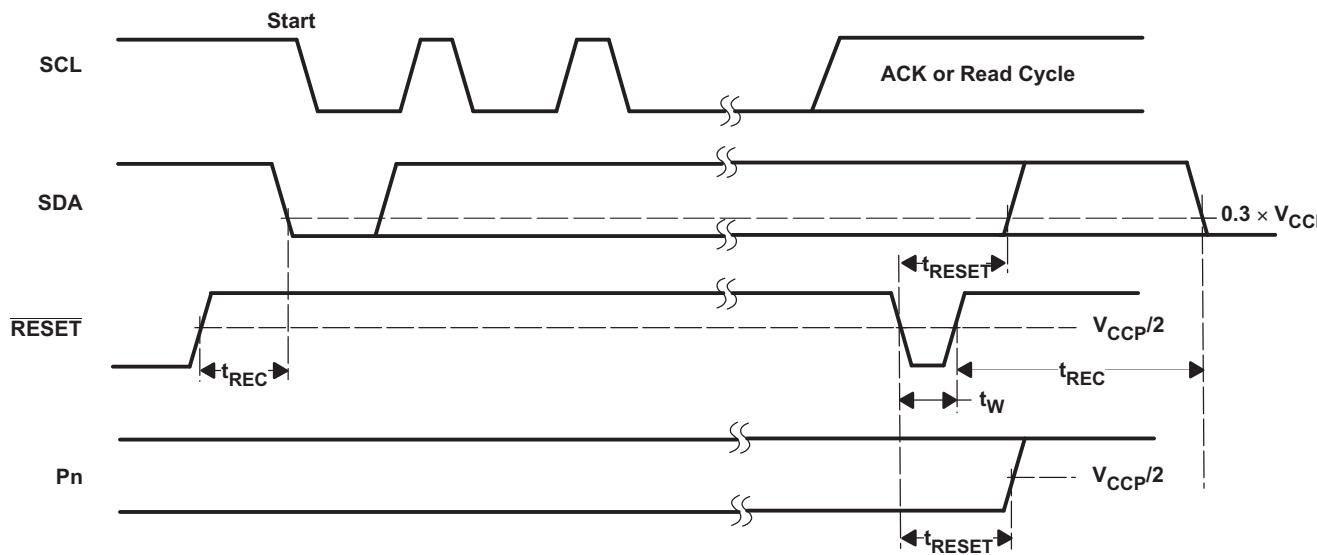
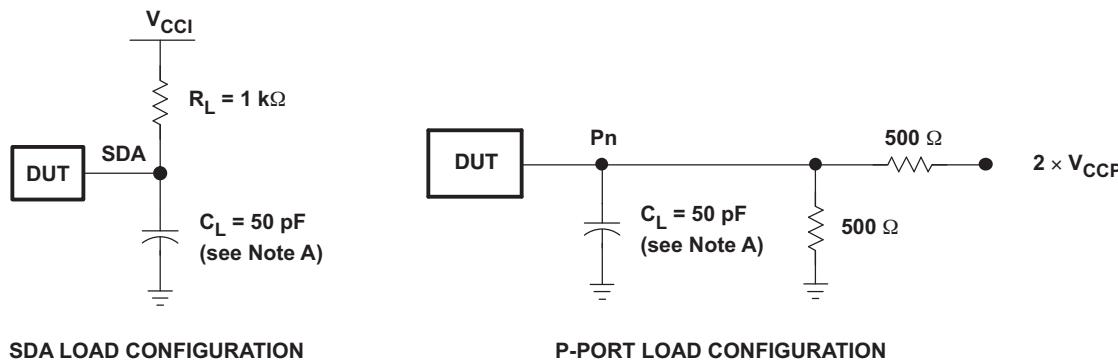
Figure 15. Interrupt Load Circuit And Voltage Waveforms

Parameter Measurement Information (continued)

P-PORT LOAD CONFIGURATION

WRITE MODE (R/W = 0)

READ MODE (R/W = 1)

- C_L includes probe and jig capacitance.
- t_{pv} is measured from $0.7 \times V_{CC}$ on SCL to 50% I/O (Pn) output.
- All inputs are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r/t_f \leq 30$ ns.
- The outputs are measured one at a time, with one transition per measurement.
- All parameters and waveforms are not applicable to all devices.

Figure 16. P Port Load Circuit And Timing Waveforms

Parameter Measurement Information (continued)

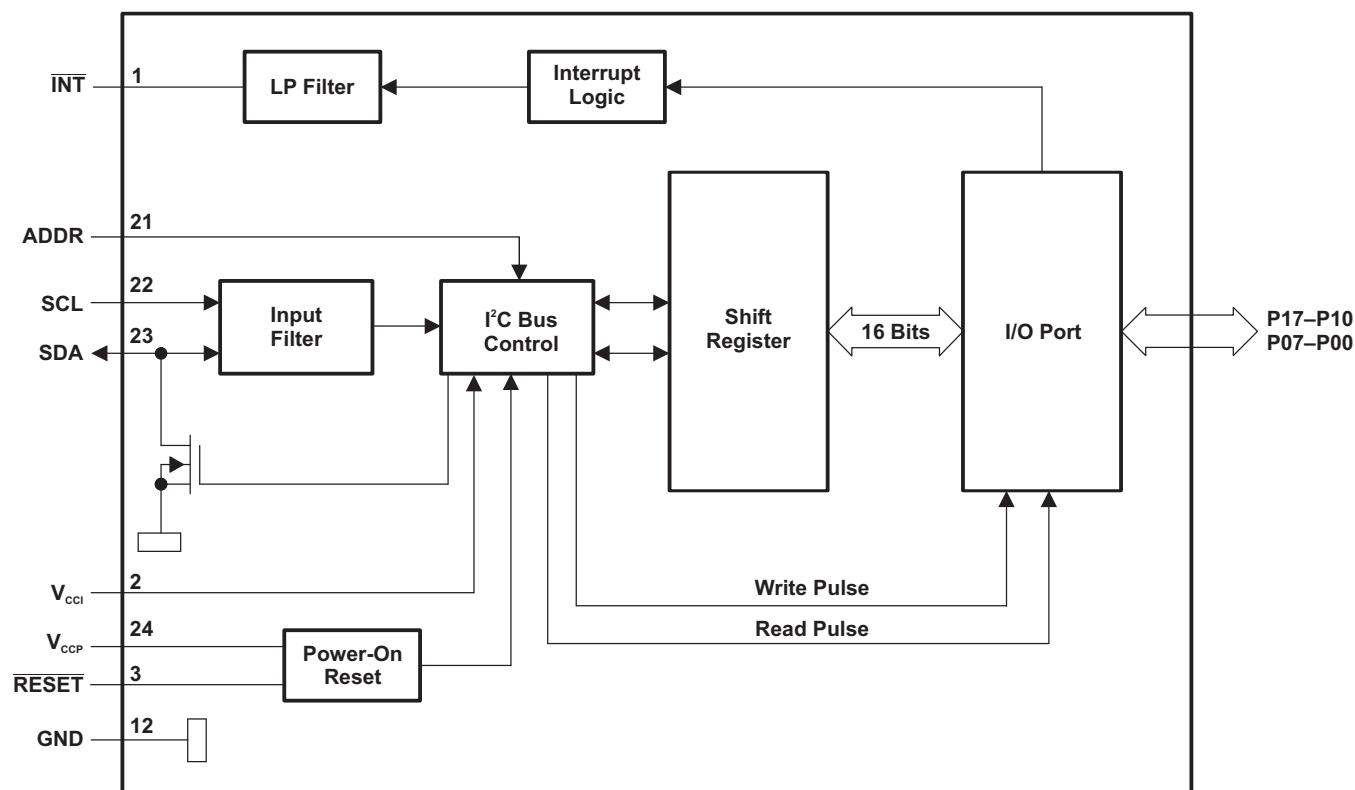


- A. C_L includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r/t_f \leq 30$ ns.
- C. The outputs are measured one at a time, with one transition per measurement.
- D. I/Os are configured as inputs.
- E. All parameters and waveforms are not applicable to all devices.

Figure 17. Reset Load Circuits And Voltage Waveforms

8 Detailed Description

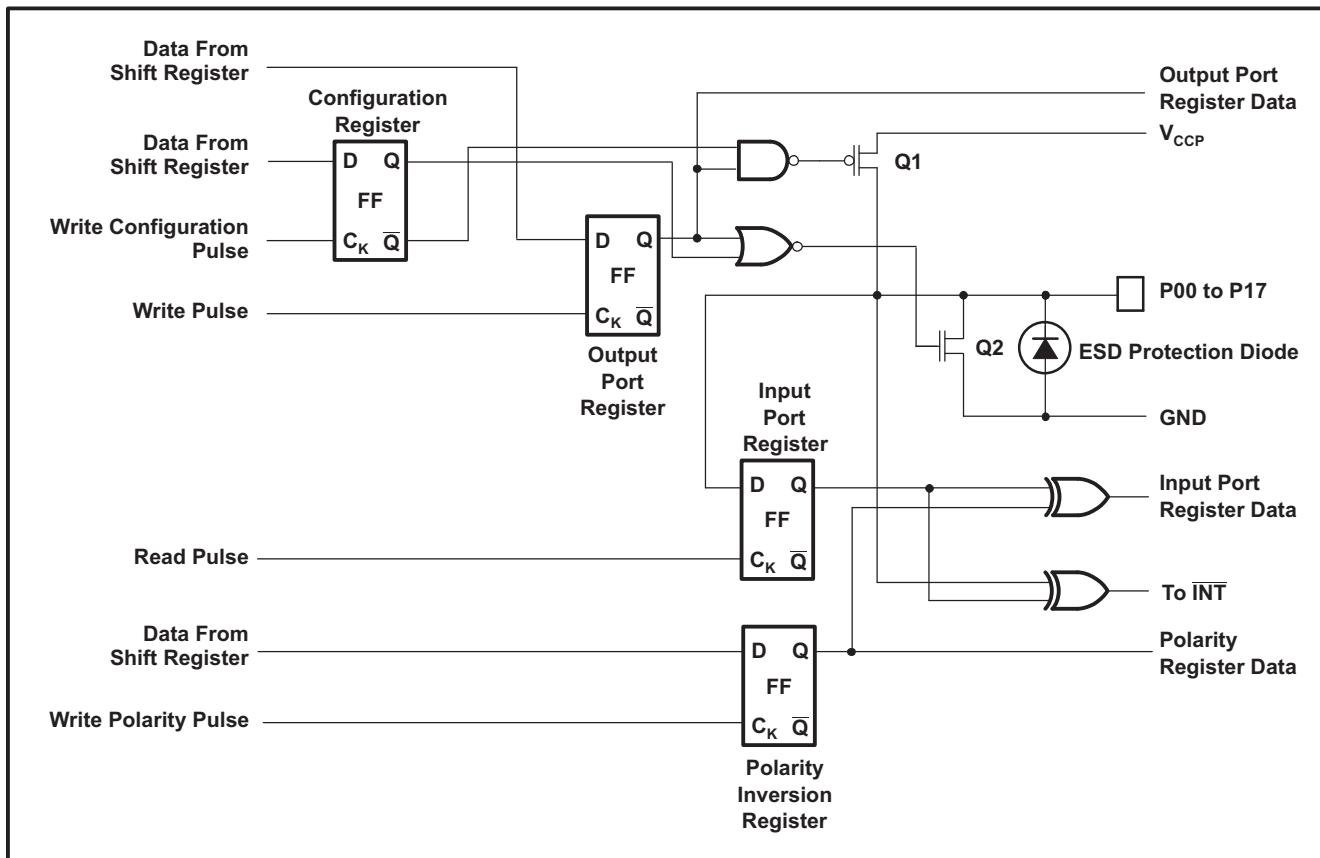
8.1 Functional Block Diagram



- A. All I/Os are set to inputs at reset.
- B. Pin numbers shown are for the PW package.

Figure 18. Logic Diagram (Positive Logic)

Functional Block Diagram (continued)



A. On power up or reset, all registers return to default values.

Figure 19. Simplified Schematic Of P0 To P17

8.2 Device Functional Modes

8.2.1 Voltage Translation

Table 1 shows how to set up V_{CC} levels for the necessary voltage translation between the I²C bus and the TCA6416.

Table 1. Voltage Translation

V_{CCI} (SDA AND SCL OF I ² C MASTER) (V)	V_{CCP} (P PORT) (V)
1.8	1.8
1.8	2.5
1.8	3.3
1.8	5
2.5	1.8
2.5	2.5
2.5	3.3
2.5	5
3.3	1.8
3.3	2.5
3.3	3.3
3.3	5
5	1.8
5	2.5
5	3.3
5	5

8.2.2 Reset Input (RESET)

The RESET input can be asserted to initialize the system while keeping the V_{CCP} at its operating level. A reset can be accomplished by holding the RESET pin low for a minimum of t_W . The TCA6416 registers and I²C/SMBus state machine are changed to their default state once RESET is low (0). When RESET is high (1), the I/O levels at the P port can be changed externally or through the master. This input requires a pullup resistor to V_{CCP} , if no active connection is used.

8.2.2.1 RESET Errata

If RESET voltage set higher than V_{CC} , current will flow from RESET pin to V_{CC} pin.

System Impact

V_{CC} will be pulled above its regular voltage level

System Workaround

Design such that RESET voltage is same or lower than V_{CC}

8.2.3 Power-On Reset

When power (from 0 V) is applied to V_{CCP} , an internal power-on reset holds the TCA6416 in a reset condition until V_{CCP} has reached V_{POR} . At that time, the reset condition is released, and the TCA6416 registers and I²C/SMBus state machine initializes to their default states. After that, V_{CCP} must be lowered to below 0.2 V and back up to the operating voltage for a power-reset cycle.

8.2.4 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 (in [Figure 19](#)) are off, which creates a high-impedance input. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the output port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

8.2.5 Interrupt (INT) Output

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{IV} , the signal \overline{INT} is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting, data is read from the port that generated the interrupt or in a stop event. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as \overline{INT} .

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register.

In the TCA6416, an interrupt is not immediately generated by any rising or falling edge of port inputs in input mode after issuing any I²C commands (read or write). In order to capture the \overline{INT} in the TCA6416, the user needs to add one more SCL clock pulse after a Stop signal.

The \overline{INT} output has an open-drain structure and requires a pullup resistor to V_{CCP} or V_{CCI} depending on the application. If the \overline{INT} signal is connected back to the processor that provides the SCL signal to the TCA6416, then the INT pin has to be connected to V_{CCI} . If not, the INT pin can be connected to V_{CCP} .

8.2.5.1 Interrupt Errata

The INT will be improperly de-asserted if the following two conditions occur:

1. The last I²C command byte (register pointer) written to the device was 00h.

NOTE

This generally means the last operation with the device was a Read of the input register. However, the command byte may have been written with 00h without ever going on to read the input register. After reading from the device, if no other command byte written, it will remain 00h.

2. Any other slave device on the I²C bus acknowledges an address byte with the R/W bit set high

System Impact

Can cause improper interrupt handling as the Master will see the interrupt as being cleared.

System Workaround

Minor software change: User must change command byte to something besides 00h after a Read operation to the TCA6416 device or before reading from another slave device.

NOTE

Software change will be compatible with other versions (competition and TI redesigns) of this device.

8.3 Programming

8.3.1 I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output, while the SCL input is high (see [Figure 20](#)). After the Start condition, the device address is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address (ADDR) input of the slave device must not be changed between the Start and the Stop conditions.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see [Figure 21](#)).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see [Figure 20](#)).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period (see [Figure 22](#)). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

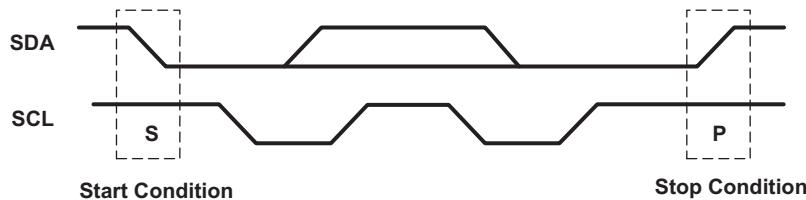


Figure 20. Definition Of Start And Stop Conditions

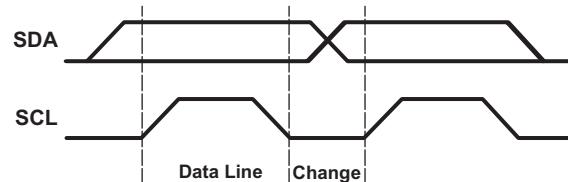


Figure 21. Bit Transfer

Programming (continued)

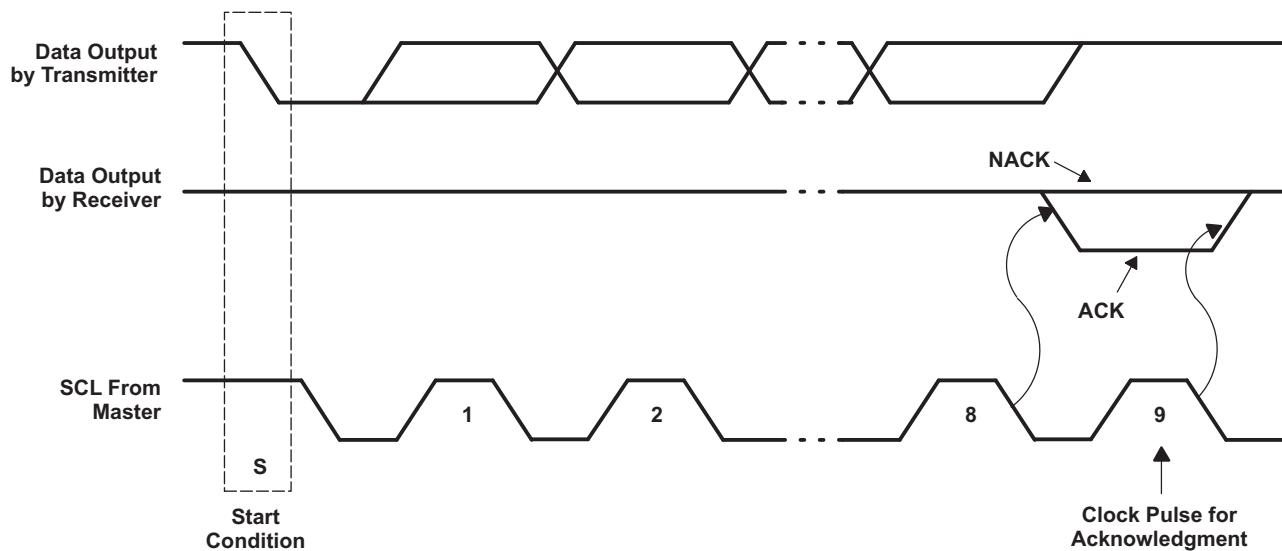


Figure 22. Acknowledgment On The I²C Bus

8.3.2 Register Map

Table 2. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I ² C slave address	L	H	L	L	L	L	ADDR	R/W
I/O data bus	P07	P06	P05	P04	P03	P02	P01	P00
	P17	P16	P15	P14	P13	P12	P11	P10

8.3.2.1 Device Address

The address of the TCA6416 is shown in Figure 23.

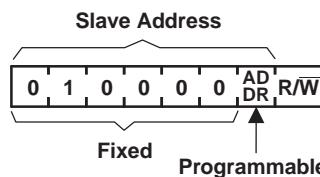


Figure 23. Tca6416 Address

Table 3. Address Reference

ADDR	I ² C BUS SLAVE ADDRESS
L	32 (decimal), 20 (hexadecimal)
H	33 (decimal), 21 (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

8.3.2.2 Control Register And Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte, which is stored in the control register in the TCA6416. Three bits of this data byte state the operation (read or write) and the internal registers (input, output, polarity inversion, or configuration) that will be affected. This register can be written or read through the I²C bus. The command byte is sent only during a write transmission.

Once a new command has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.

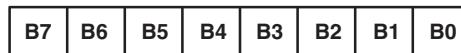


Figure 24. Control Register Bits

Table 4. Command Byte

CONTROL REGISTER BITS								COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B7	B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	0	00	Input Port 0	Read byte	xxxx xxxx ⁽¹⁾
0	0	0	0	0	0	0	1	01	Input Port 1	Read byte	xxxx xxxx
0	0	0	0	0	0	1	0	02	Output Port 0	Read/write byte	1111 1111
0	0	0	0	0	0	1	1	03	Output Port 1	Read/write byte	1111 1111
0	0	0	0	0	1	0	0	04	Polarity Inversion Port 0	Read/write byte	0000 0000
0	0	0	0	0	1	0	1	05	Polarity Inversion Port 1	Read/write byte	0000 0000
0	0	0	0	0	1	1	0	06	Configuration Port 0	Read/write byte	1111 1111
0	0	0	0	0	1	1	1	07	Configuration Port 1	Read/write byte	1111 1111

(1) Undefined

8.3.2.3 Register Descriptions

The Input Port registers (registers 0 and 1) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. They act only on read operation. Writes to these registers have no effect. The default value (X) is determined by the externally applied logic level. Before a read operation, a write transmission is sent with the command byte to indicate to the I²C device that the Input Port register will be accessed next.

Table 5. Registers 0 And 1 (Input Port Registers)

BIT	I-07	I-06	I-05	I-04	I-03	I-02	I-01	I-00
DEFAULT	X	X	X	X	X	X	X	X
BIT	I-17	I-16	I-15	I-14	I-13	I-12	I-11	I-10
DEFAULT	X	X	X	X	X	X	X	X

The Output Port registers (registers 2 and 3) shows\ the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that is in the flip-flop controlling the output selection, NOT the actual pin value.

Table 6. Registers 2 And 3 (Output Port Registers)

BIT	O-07	O-06	O-05	O-04	O-03	O-02	O-01	O-00
DEFAULT	1	1	1	1	1	1	1	1
BIT	O-17	O-16	O-15	O-14	O-13	O-12	O-11	O-10
DEFAULT	1	1	1	1	1	1	1	1

The Polarity Inversion registers (register 4 and 5) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in these registers is set (written with 1), the corresponding port pin's polarity is inverted. If a bit in these registers is cleared (written with a 0), the corresponding port pin's original polarity is retained.

Table 7. Registers 4 And 5 (Polarity Inversion Registers)

BIT	P-07	P-06	P-05	P-04	P-03	P-02	P-01	P-00
DEFAULT	0	0	0	0	0	0	0	0
BIT	P-17	P-16	P-15	P-14	P-13	P-12	P-11	P-10
DEFAULT	0	0	0	0	0	0	0	0

The Configuration registers (registers 6 and 7) configure the direction of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in these registers is cleared to 0, the corresponding port pin is enabled as an output.

Table 8. Registers 6 And 7 (Configuration Registers)

BIT	C-07	C-06	C-05	C-04	C-03	C-02	C-01	C-00
DEFAULT	1	1	1	1	1	1	1	1
BIT	C-17	C-16	C-15	C-14	C-13	C-12	C-11	C-10
DEFAULT	1	1	1	1	1	1	1	1

8.3.2.4 Bus Transactions

Data is exchanged between the master and TCA6416 through write and read commands.

8.3.2.4.1 Writes

Data is transmitted to the TCA6416 by sending the device address and setting the least-significant bit (LSB) to a logic 0 (see [Figure 23](#) for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission.

The eight registers within the TCA6416 are configured to operate as four register pairs. The four pairs are input ports, output ports, polarity inversion ports and configuration ports. After sending data to one register, the next data byte is sent to the other register in the pair (see [Figure 25](#) and [Figure 26](#)). For example, if the first byte is sent to Output Port 1 (register 3), the next byte is stored in Output Port 0 (register 2).

There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.

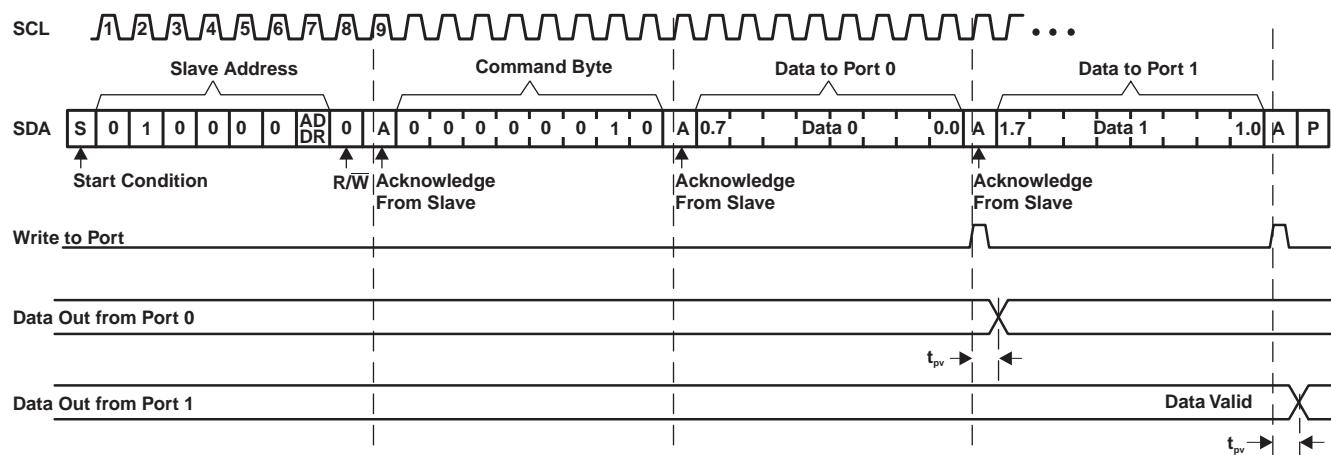


Figure 25. Write To Output Port Register

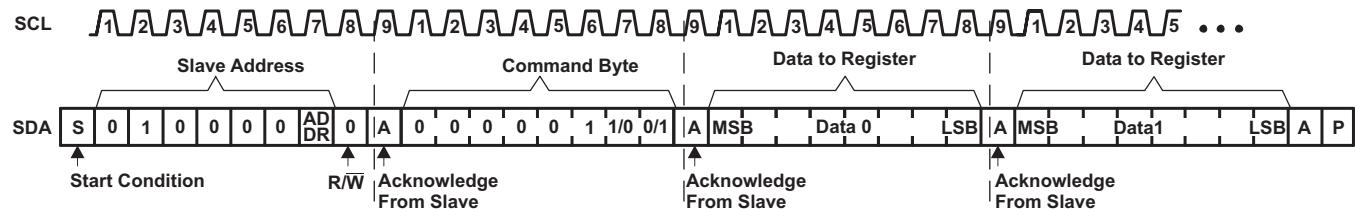


Figure 26. Write To Configuration Or Polarity Inversion Registers

8.3.2.4.2 Reads

The bus master first must send the TCA6416 address with the LSB set to a logic 0 (see [Figure 23](#) for device address). The command byte is sent after the address and determines which register is accessed.

After a restart, the device address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the TCA6416 (see [Figure 27](#) and [Figure 28](#)).

After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. For example, if the command byte references Input Port 1 before the restart, and the restart occurs when Input Port 0 is being read, the stored command byte changes to reference Input Port 0. The original command byte is forgotten. If a subsequent restart occurs, Input Port 0 is read first. Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte is read, additional bytes may be read, but the data now reflects the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0.

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

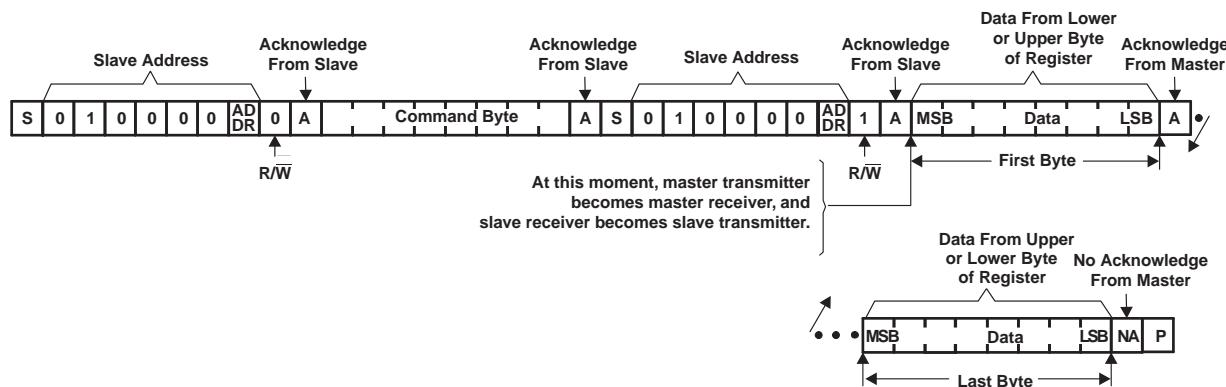
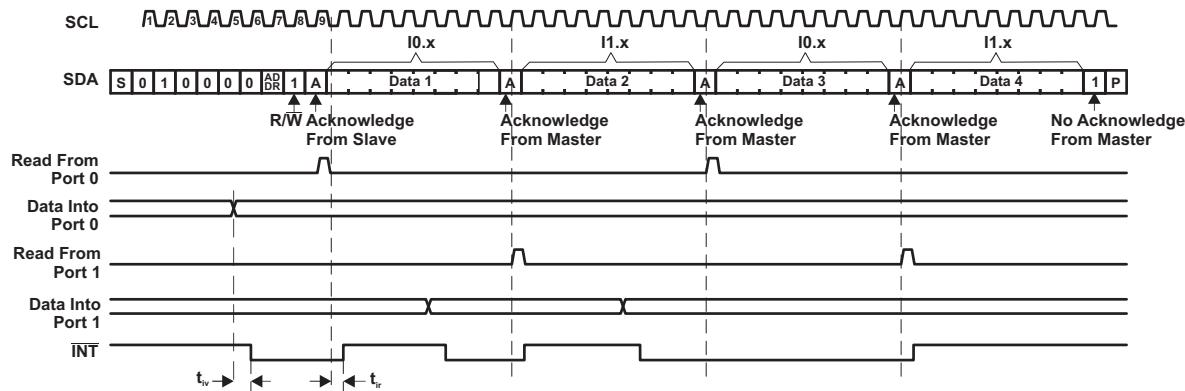


Figure 27. Read From Register



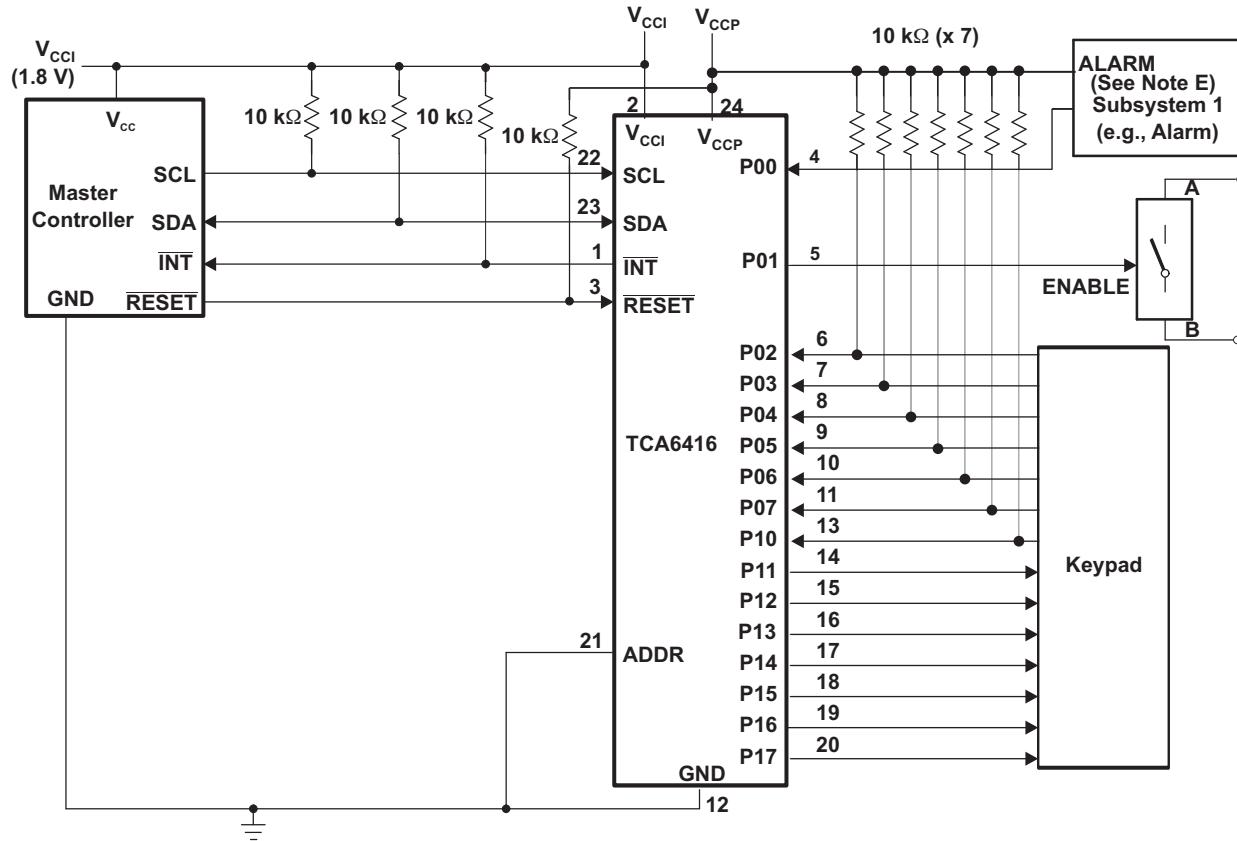
- A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).
 - B. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from P port (see [Figure 27](#)).

Figure 28. Read Input Port Register

9 Application And Implementation

9.1 Typical Application

Figure 29 shows an application in which the TCA6416 can be used.



- A. Device address configured as 0100000 for this example.
 - B. P00 and P02–P10 are configured as inputs.
 - C. P01 and P11–P17 are configured as outputs.
 - D. Pin numbers shown are for the PW package.
 - E. Resistors are required for inputs (on P port) that may float. If a driver to an input will never let the input float, a resistor is not needed. Outputs (in the P port) do not need pullup resistors.

Figure 29. Typical Application

Typical Application (continued)

9.1.1 Detailed Design Procedure

9.1.1.1 Minimizing I_{CC} When I/Os Control LEDs

When the I/Os are used to control LEDs, normally they are connected to V_{CC} through a resistor as shown in Figure 29. The LED acts as a diode so, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC} . The ΔI_{CC} parameter in Electrical Characteristics shows how I_{CC} increases as V_{IN} becomes lower than V_{CC} . Designs that must minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{CC} when the LED is off.

Figure 30 shows a high-value resistor in parallel with the LED. Figure 31 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevent additional supply current consumption when the LED is off.

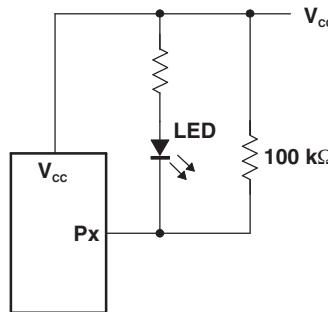


Figure 30. High-Value Resistor In Parallel With The Led

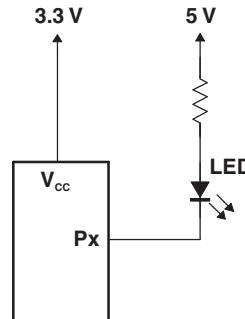


Figure 31. Device Supplied By A Low Voltage

10 Power Supply Recommendations

10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, TCA6416 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in [Figure 32](#) and [Figure 33](#).

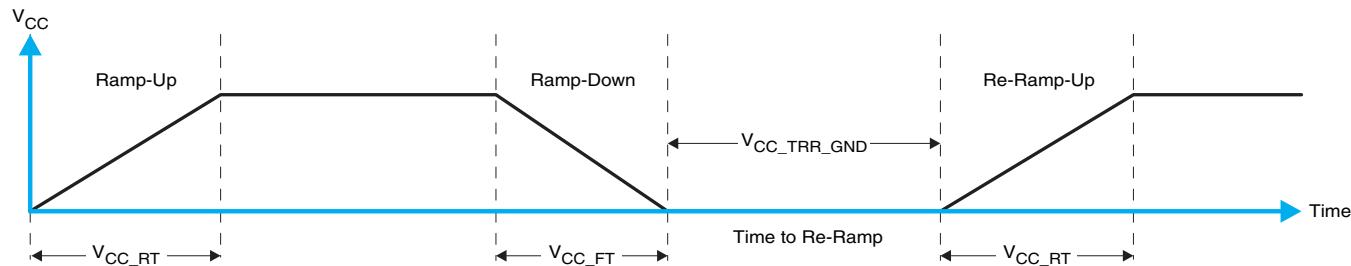


Figure 32. V_{CC} Is Lowered Below 0.2 V Or 0 V And Then Ramped Up To V_{CC}

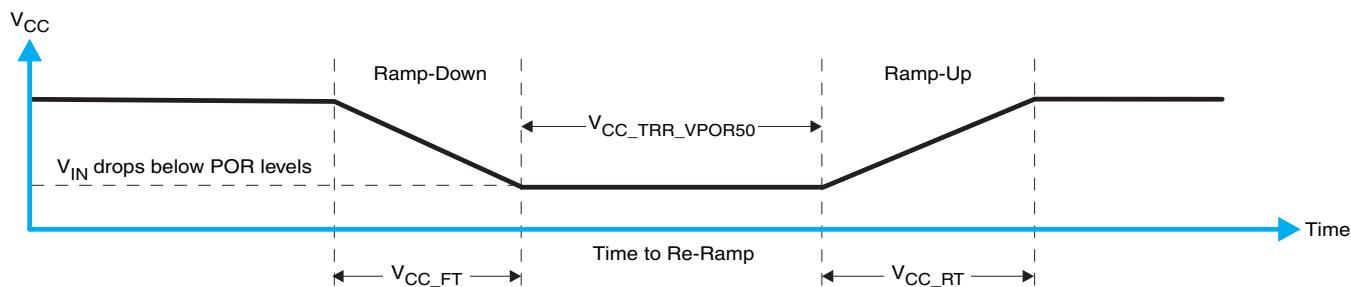


Figure 33. V_{CC} Is Lowered Below The Por Threshold, Then Ramped Back Up To V_{CC}

[Table 9](#) specifies the performance of the power-on reset feature for TCA6416 for both types of power-on reset.

Table 9. Recommended Supply Sequencing And Ramp Rates⁽¹⁾

PARAMETER		MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall rate	See Figure 32	1	100	ms
V_{CC_RT}	Rise rate	See Figure 32	0.01	100	ms
$V_{CC_TRR_GND}$	Time to re-ramp (when V_{CC} drops to GND)	See Figure 32	0.001		ms
$V_{CC_TRR_POR50}$	Time to re-ramp (when V_{CC} drops to $V_{POR_MIN} - 50$ mV)	See Figure 33	0.001		ms
V_{CC_GH}	Level that V_{CC} can glitch down to, but not cause a functional disruption when $V_{CC_GH} = 1$ μ s	See Figure 34		1.2	V
V_{CC_GW}	Glitch width that will not cause a functional disruption when $V_{CC_GH} = 0.5 \times V_{CC}$	See Figure 34			μ s
V_{PORF}	Voltage trip point of POR on falling V_{CC}		0.767	1.144	V
V_{PORR}	Voltage trip point of POR on rising V_{CC}		1.033	1.428	V

(1) $T_A = -40^\circ\text{C}$ to 85°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. [Figure 34](#) and [Table 9](#) provide more information on how to measure these specifications.



Figure 34. Glitch Width And Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I²C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. [Figure 35](#) and [Table 9](#) provide more details on this specification.

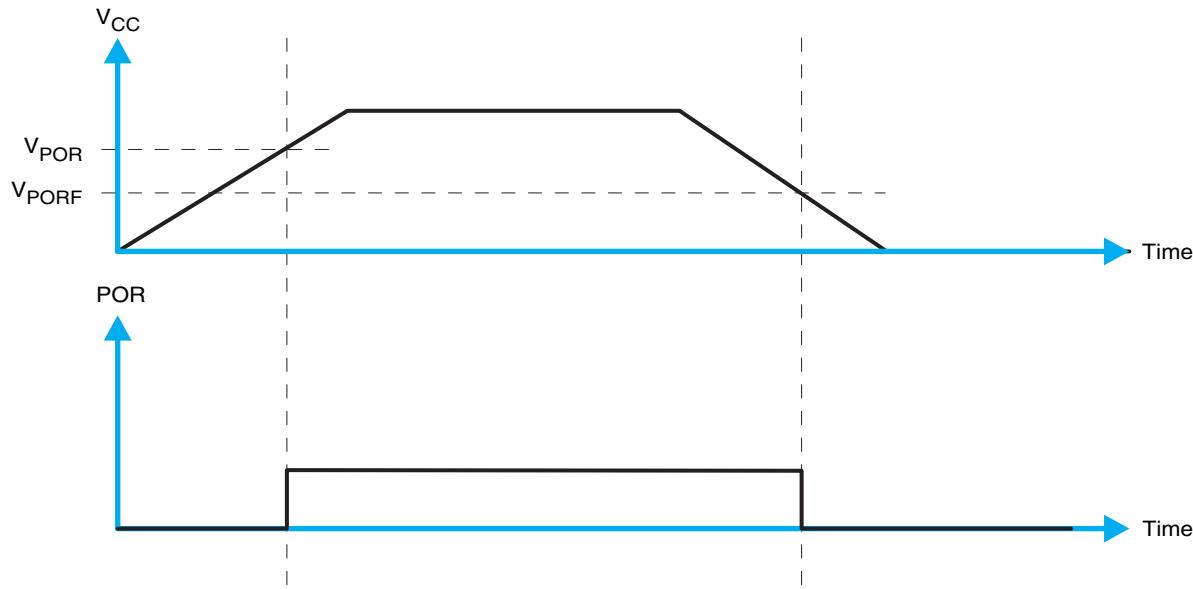


Figure 35. V_{POR}

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCA6416PWR	NRND	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PH416
TCA6416PWR.A	NRND	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PH416
TCA6416PWR.B	NRND	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PH416
TCA6416PWT	NRND	Production	TSSOP (PW) 24	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PH416
TCA6416PWT.A	NRND	Production	TSSOP (PW) 24	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PH416
TCA6416PWT.B	NRND	Production	TSSOP (PW) 24	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PH416
TCA6416RTWR	NRND	Production	WQFN (RTW) 24	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PH416
TCA6416RTWR.A	NRND	Production	WQFN (RTW) 24	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PH416
TCA6416RTWR.B	NRND	Production	WQFN (RTW) 24	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PH416

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

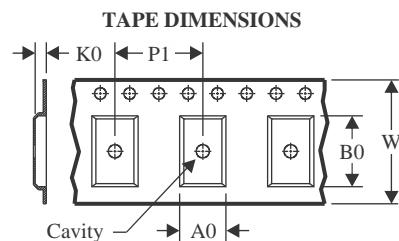
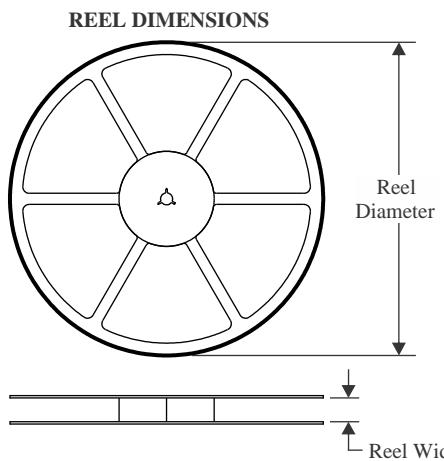
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

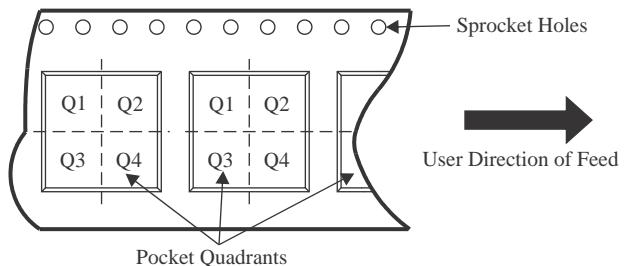
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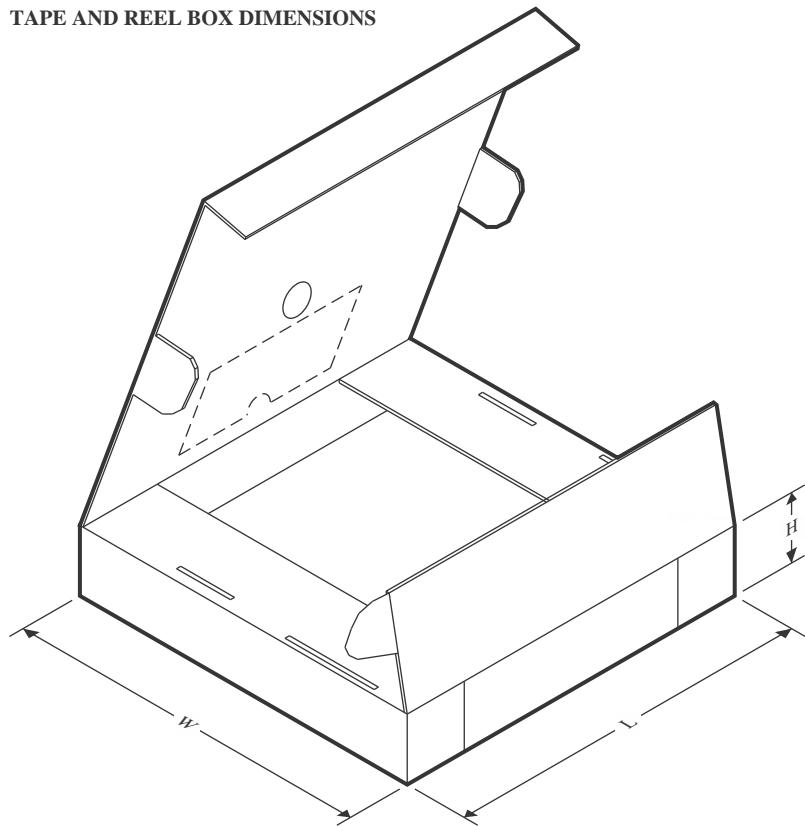
TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA6416PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TCA6416PWT	TSSOP	PW	24	250	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TCA6416RTWR	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

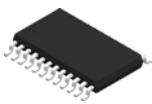
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA6416PWR	TSSOP	PW	24	2000	353.0	353.0	32.0
TCA6416PWT	TSSOP	PW	24	250	353.0	353.0	32.0
TCA6416RTWR	WQFN	RTW	24	3000	353.0	353.0	32.0

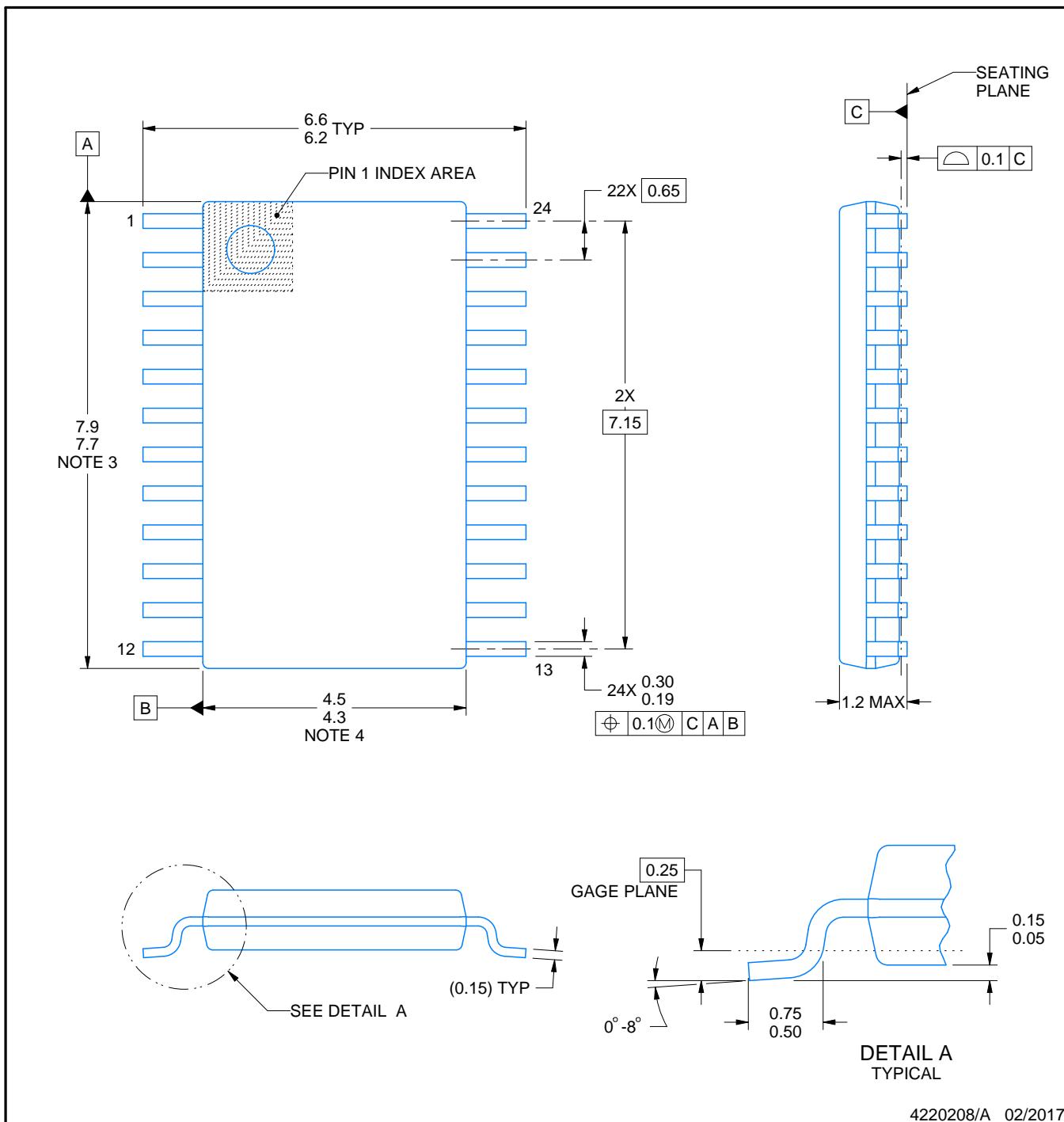
PACKAGE OUTLINE

PW0024A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

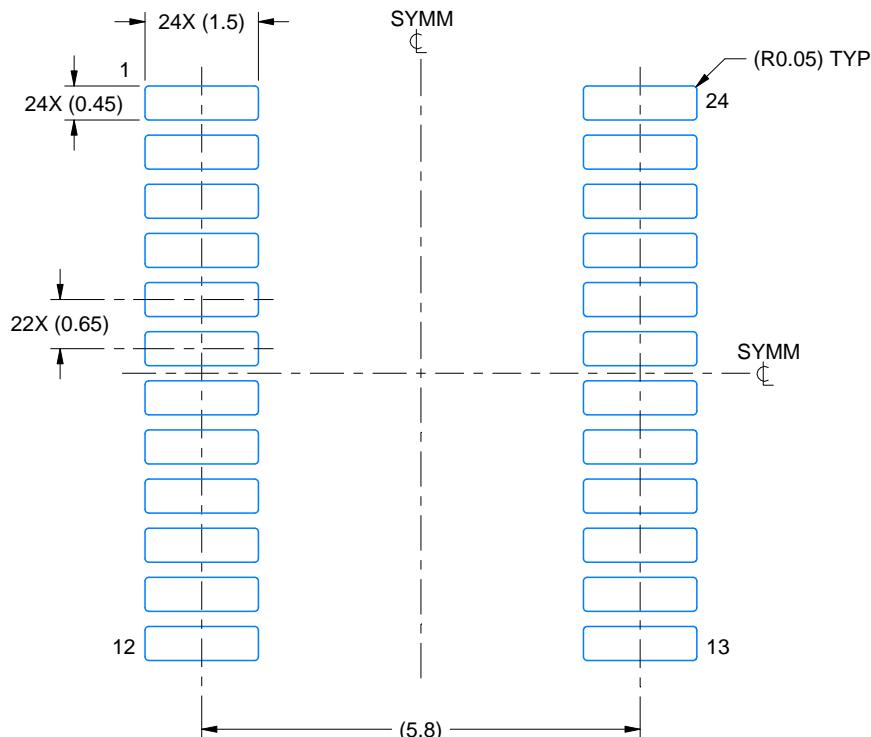
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

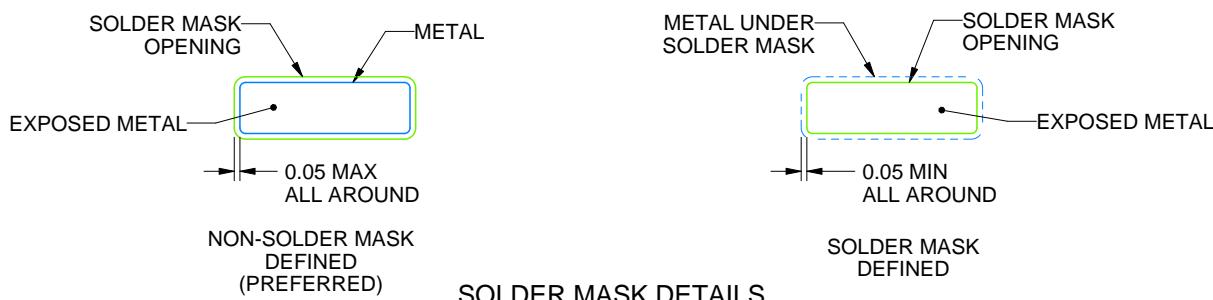
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

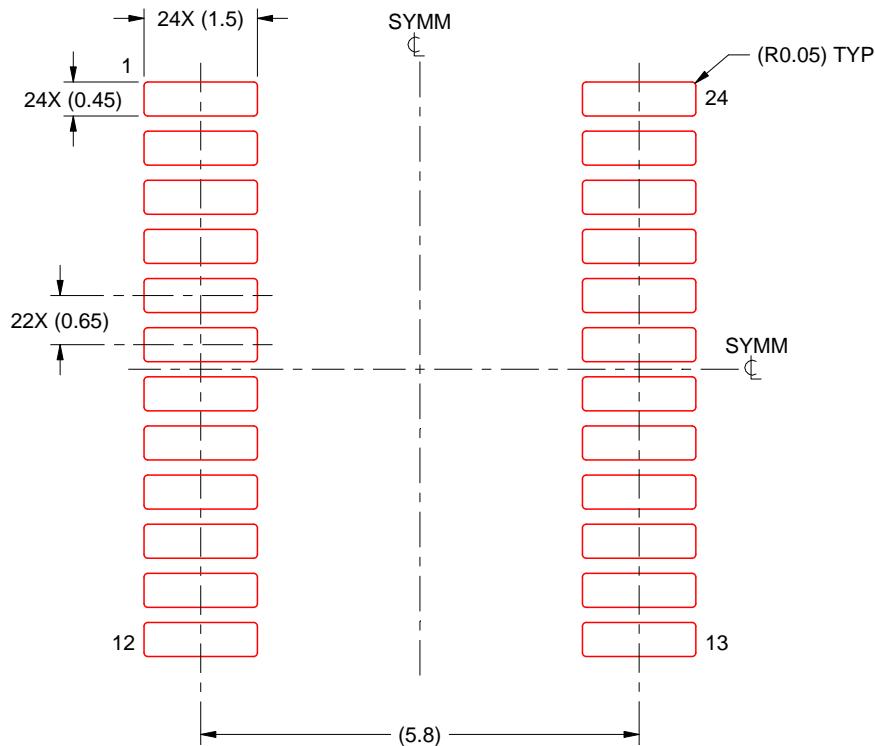
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

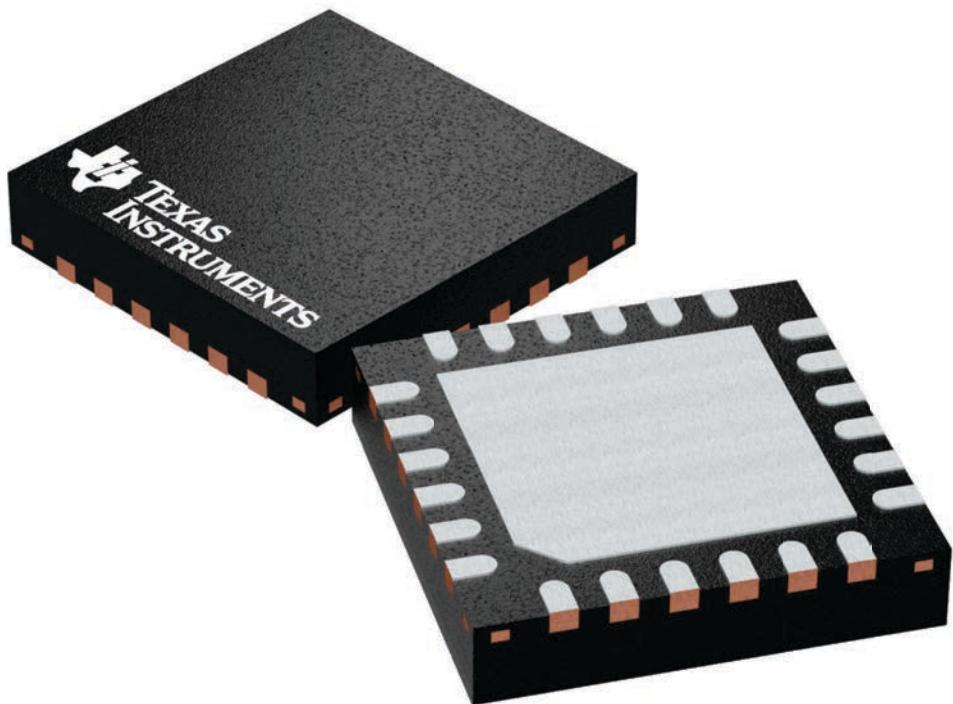
RTW 24

WQFN - 0.8 mm max height

4 x 4, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

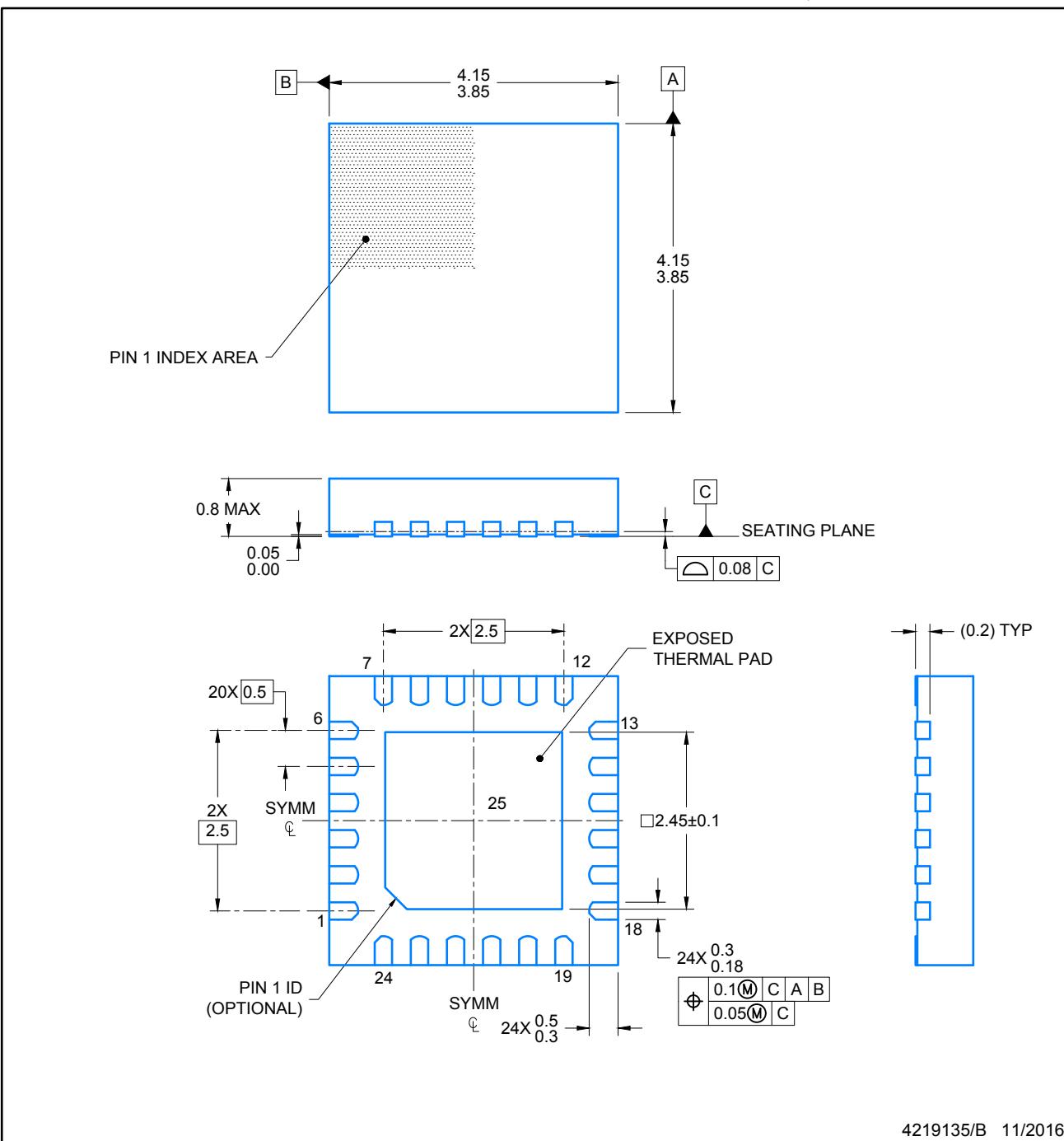


4224801/A

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



4219135/B 11/2016

NOTES:

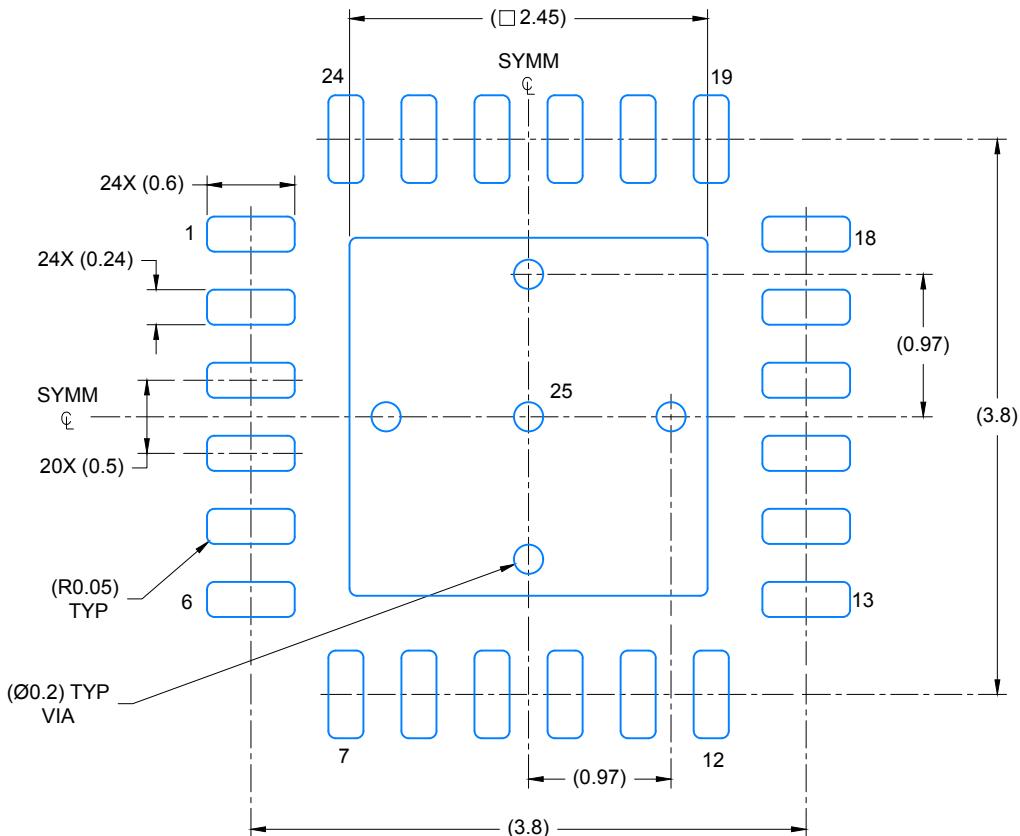
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

RTW0024B

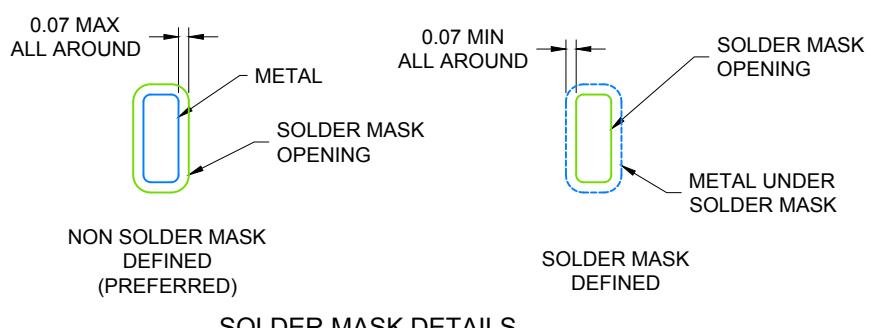
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



LAND PATTERN EXAMPLE

SCALE: 20X



4219135/B 11/2016

NOTES: (continued)

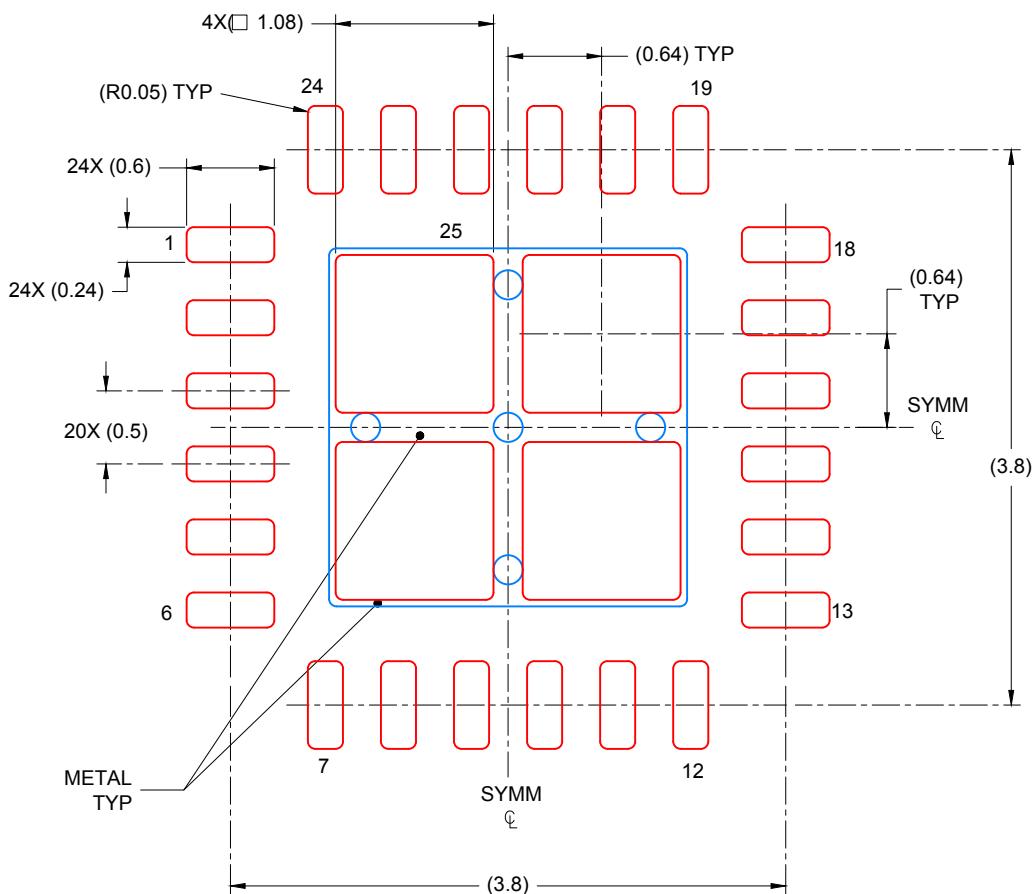
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RTW0024B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED COVERAGE BY AREA UNDER PACKAGE
SCALE: 20X

4219135/B 11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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