

THS3491 900-MHz, 500-mA High-Power Output Current Feedback Amplifier

1 Features

- Bandwidth:
 - 900 MHz ($V_O = 2 V_{PP}$, $A_V = 5 V/V$)
 - 320 MHz ($V_O = 10 V_{PP}$, $A_V = 5 V/V$)
- Slew rate: 8000 V/ μ s ($V_O = 20 V_{PP}$)
- Input voltage noise: 1.7 nV/ $\sqrt{Hz}$
- Bipolar supply range: $\pm 7 V$ to $\pm 16 V$
- Single-supply range: 14 V to 32 V
- Output swing: 28 V_{PP} (± 16 -V supplies, 100- Ω load)
- Linear output current: ± 420 mA (typical)
- 16.8-mA trimmed supply current (low temperature coefficient)
- HD2 and HD3: less than -75 dBc (50 MHz, $V_O = 10 V_{PP}$, 100- Ω load)
- Rise and fall time: 1.3 ns (10-V step)
- Overshoot: 1.5% (10-V step, $A_V = 5 V/V$)
- Current limit and thermal shutdown protection
- Power down feature

2 Applications

- High-voltage, arbitrary waveform generators
- Pattern generators for LCD testers
- Output drivers for LCR meters
- Power FET drivers
- High capacitive load piezo element drivers
- VDSL line drivers
- Pin-compatible upgrade to THS3095 (DDA)

3 Description

The THS3491 current feedback amplifier (CFA) provides a new level of performance for applications requiring the lowest distortion at high output power levels from DC through values greater than 100 MHz at 100- Ω loads. Although specified at a gain of 5 V/V, this current feedback design holds near constant bandwidth and distortion over a wide range of gains.

The 8000 V/ μ s of slew rate delivers an output of 10 V_{PP} into demanding loads with low distortion through 100 MHz. The 900-MHz, small-signal bandwidth delivers a low overshoot of less than 1.5% for a 10-V step, and rise and fall times of less than 1.3 ns. Peak output current drive values greater than 500 mA enable driving heavy capacitive loads with fast signals.

New designs benefit from the lowest distortion using the VQFN-16 (RGT) package, whereas the 8-pin HSOIC (DDA) package (with PowerPAD™) upgrades existing THS3091 or THS3095 designs. Lower output headroom for the THS3491 provides more output swing on the same ± 15 -V supplies versus legacy THS3091 or THS3095 options.

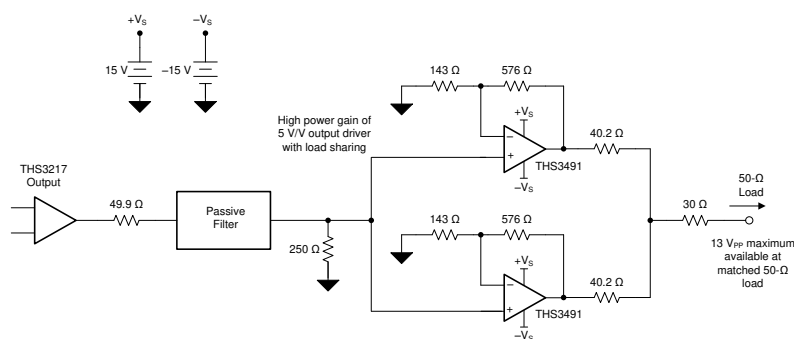
Package Information⁽¹⁾⁽²⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
THS3491	RGT (VQFN, 16)	3.00 mm $\times$ 3.00 mm
	DDA (HSOIC, 8)	4.89 mm $\times$ 3.90 mm

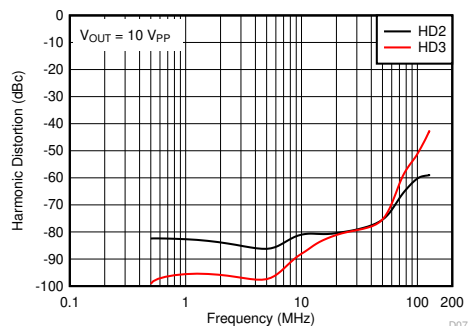
Device Information

PART NUMBER	PACKAGE	DIE SIZE (NOM)
THS3491	Bare die	1.02 mm $\times$ 1.06 mm

- For all available packages, see the package option addendum at the end of the data sheet.
- See the [Device Comparison Table](#)



Typical Arbitrary Waveform Generator Output Drive Circuit



Harmonic Distortion vs Frequency



Table of Contents

1 Features	1	9.2 Functional Block Diagram.....	24
2 Applications	1	9.3 Feature Description.....	25
3 Description	1	9.4 Device Functional Modes.....	27
4 Revision History	2	10 Application and Implementation	30
5 Device Comparison Table	4	10.1 Application Information.....	30
6 Pin Configuration and Functions	5	10.2 Typical Application.....	32
7 Bare Die Information	6	10.3 Power Supply Recommendations.....	34
8 Specifications	7	10.4 Layout.....	35
8.1 Absolute Maximum Ratings.....	7	11 Device and Documentation Support	40
8.2 ESD Ratings.....	7	11.1 Documentation Support.....	40
8.3 Recommended Operating Conditions.....	7	11.2 Receiving Notification of Documentation Updates.....	40
8.4 Thermal Information.....	7	11.3 Support Resources.....	40
8.5 Electrical Characteristics: $V_S = \pm 15\text{ V}$	8	11.4 Trademarks.....	40
8.6 Electrical Characteristics: $V_S = \pm 7.5\text{ V}$	11	11.5 Electrostatic Discharge Caution.....	40
8.7 Typical Characteristics: $\pm 15\text{ V}$	13	11.6 Glossary.....	40
8.8 Typical Characteristics: $\pm 7.5\text{ V}$	20	12 Mechanical, Packaging, and Orderable Information	40
9 Detailed Description	24		
9.1 Overview.....	24		

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (July 2018) to Revision C (February 2023)	Page
• Added bare die package details to the data sheet.....	1
• Removed <i>bipolar-supply operating range</i> and <i>single-supply operating range</i> specifications from <i>Electrical Characteristics: $V_S = \pm 15\text{ V}$</i>	8
• Added new test level A2 that clarifies what is tested for die sales.....	8
Changes from Revision A (March 2018) to Revision B (July 2018)	Page
• Changed resistor values in <i>Typical Arbitrary Waveform Generator Output Drive Circuit</i> from 49.9 Ω to 40.2 Ω	1
• Changed resistor values in <i>Typical Arbitrary Waveform Generator Output Drive Circuit</i> from 24.9 Ω to 30 Ω	1
• Changed $T_A = 25^\circ\text{C}$ to $T_A \approx 25^\circ\text{C}$ in <i>Electrical Characteristics: $\pm 15\text{ V}$</i> condition statement.....	8
• Changed <i>100% tested at 25°C</i> to <i>100% tested at $\approx 25^\circ\text{C}$</i> in the footnote of <i>Electrical Characteristics: $\pm 15\text{ V}$</i>	8
• Added <i>DDA package only</i> in Test Conditions column for " V_{OS} " specification.....	8
• Added new V_{OS} specification line for RGT package.....	8
• Added min/max values to R_{FB_TRACE} specification.....	8
• Changed units from: $pF \parallel k\Omega$ to: $k\Omega \parallel pF$ and changed typical spec accordingly.....	8
• Added min/max values to T_{J_SENSE} 25°C value specification.....	8
• Changed T_{J_SENSE} temperature coefficient specification's typical value from 3 mV/°C to 3.2 mV/°C.....	8
• Added min/max values to T_{J_SENSE} input impedance specification.....	8
• Changed " $T_A = 25^\circ\text{C}$ " to " $T_A \approx 25^\circ\text{C}$ " in <i>Electrical Characteristics: $\pm 7.5\text{ V}$</i> condition statement.....	11
• Changed " <i>100% tested at 25°C</i> " to " <i>100% tested at $\approx 25^\circ\text{C}$</i> " in the footnote of <i>Electrical Characteristics: $\pm 7.5\text{ V}$</i>	11
• Added "DDA package only" in Test Conditions column for " V_{OS} " specification.....	11
• Added new V_{OS} specification line for RGT package.....	11
• Changed units from " $pF \parallel k\Omega$ " to " $k\Omega \parallel pF$ " and changed typical values accordingly.....	11
• Added min/max values to " T_{J_SENSE} 25°C value" specification.....	11
• Added min/max values to " T_{J_SENSE} input impedance" specification.....	11
• Changed " $T_A = 25^\circ\text{C}$ " to " $T_A \approx 25^\circ\text{C}$ " in <i>Typical Characteristics: $\pm 15\text{ V}$</i> condition statement.....	13
• Changed Z_{OL} low frequency value from 160 dB to 138 dB in <i>Open-Loop Transimpedance Gain and Phase vs Frequency</i>	13
• Changed <i>Overdrive Recovery Time</i> grid lines and added gain information.....	13

• Added T_{J_SENSE} Voltage vs Ambient Temperature	13
• Changed " $T_A = 25^{\circ}\text{C}$ " to " $T_A \cong 25^{\circ}\text{C}$ " in <i>Typical Characteristics: ± 7.5 V</i> condition statement.....	20
• Changed <i>Overdrive Recovery Time</i> grid lines and added gain information.....	20
• Corrected polarity of negative supply capacitor in <i>Wideband Noninverting Gain Configuration (5 V/V)</i>	27
• Corrected negative supply capacitor polarity in <i>Wideband Inverting Gain Configuration (5 V/V)</i>	28
• Added " R_{ISO} " to " $1\ \Omega$ " in <i>Driving a Large Capacitive Load Using an Output Series Isolation Resistor</i>	30
• Added 1-k Ω resistor to <i>Driving a Large Capacitive Load Using an Output Series Isolation Resistor</i>	30
• Changed supply values from ± 15 V to ± 7.5 V in <i>Video Distribution Amplifier Application</i>	31
• Changed R_{S2} values from 100 Ω to 40.2 Ω in <i>Load-Sharing Driver Application</i>	32
• Added 30- Ω resistor to <i>Load-Sharing Driver Application</i>	32
• Added text to <i>Design Requirements</i> and <i>Detailed Design Procedure</i> sections	33
• Added <i>Application Curves</i> section	34

Changes from Revision * (August 2017) to Revision A (March 2018)	Page
---	-------------

• Changed device status from Advance Information to Production Data	1
---	---

5 Device Comparison Table

DEVICE	SUPPLY, V_S (V)	SSBW, $A_V = 5$ (MHz)	MAXIMUM ICC AT 25°C (mA)	INPUT NOISE V_n (nV/ $\sqrt{\text{Hz}}$)	HD2/3, 10 V_{PP} AT 50 MHz, $G = 5 \text{ V/V}$ (dBc)	SLEW RATE (V/ μs)	LINEAR OUTPUT CURRENT (mA)
THS3491	± 15	900	17.3	1.7	–76/–75	7100 ⁽¹⁾	± 420
THS3095	± 15	190	9.5	1.6	–40/–42	1200 ⁽²⁾	± 250
THS3001	± 15	350	9	1.6	N/A	1400 ⁽³⁾	± 120
THS3061	± 15	260	8.3	2.6	N/A	1060 ⁽⁴⁾	± 140

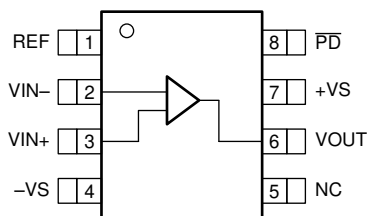
(1) Slew rate from FPBW of 320 MHz, 10 V_{PP}

(2) Slew rate from FPBW of 135 MHz, 4 V_{PP}

(3) Slew rate from FPBW of 32 MHz, 20 V_{PP}

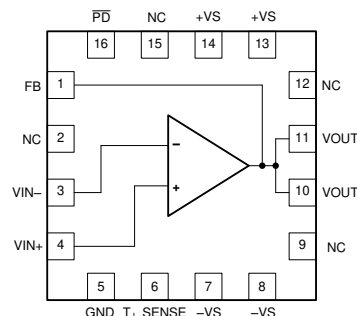
(4) Slew rate from FPBW of 120 MHz, 4 V_{PP}

6 Pin Configuration and Functions



NC - no internal connection

Figure 6-1. DDA Package, 8-Pin HSOIC With PowerPAD (Top View)



NC - no internal connection

Figure 6-2. RGT Package, 16-Pin VQFN With Exposed Thermal Pad (Top View)

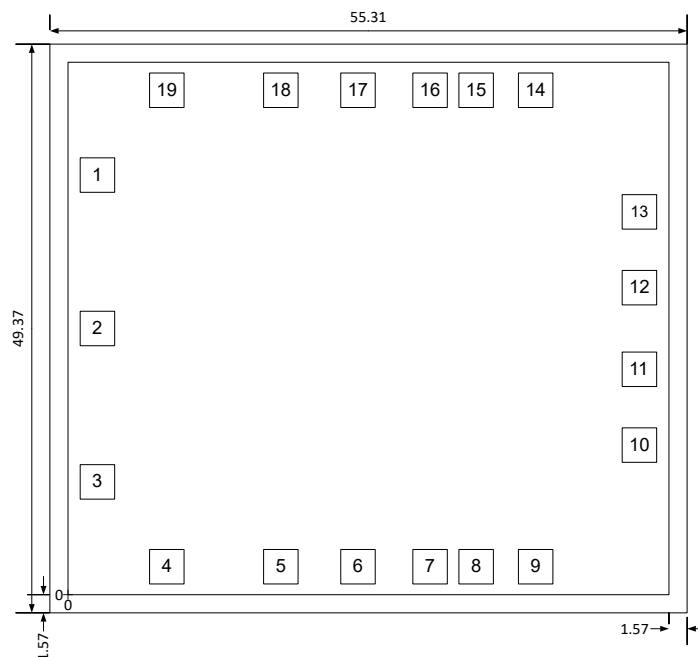
Table 6-1. Pin Functions

PIN ⁽¹⁾			TYPE ⁽²⁾	DESCRIPTION
NAME	HSOIC	VQFN		
FB	—	1	O	Input side feedback pin
GND	—	5	GND	Ground, $\overline{\text{PD}}$ logic reference on the VQFN-16 (RGT) package
NC	5	2, 9, 12, 15	—	No connect (there is no internal connection). Recommended connection to a heat spreading plane, typically GND.
$\overline{\text{PD}}$	8	16	I	Amplifier power down: low = amplifier disabled, high (default) = amplifier enabled
REF	1	—	I	$\overline{\text{PD}}$ logic reference on the SOIC-8 (DDA) package. Typically connected to GND.
T_J_SENSE	—	6	O	Voltage proportional to die temperature
VIN-	2	3	I	Inverting input
VIN+	3	4	I	Noninverting input
VOUT	6	10, 11	O	Amplifier output
-VS	4	7, 8	P	Negative power supply
+VS	7	13, 14	P	Positive power supply
Thermal pad			—	Thermal pad. Electrically isolated from the device. Recommended connection to a heat spreading plane, typically GND.

- (1) Both packages include a backside thermal pad. The thermal pad can be connected to a heat spreading plane that can be at any voltage because the device die is electrically isolated from this metal plate. The thermal pad can also be unused (not connected to any heat spreading plane or voltage) giving higher thermal impedance.
- (2) GND = ground, I = input, O = output, P = power

7 Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION	BOND PAD DIMENSIONS
15 mils (381 μm)	Silicon with backgrind	Wafer backside is electrically connected to -VS	Al	76.0 μm $\times$ 76.0 μm



Bond Pad Coordinates in Microns

NAME	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
FB	1	26.9	887	103	963
VIN-	2	26.9	549	103	625
VIN+	3	26.9	211	103	287
REF	4	180	23.7	256	99.7
DNC	5	431	23.7	507	99.7
T _J _SENSE	6	601	23.7	677	99.7
-VS	7	760	23.7	836	99.7
-VS	8	862	23.7	938	99.7
-VS	9	993	23.7	1069	99.7
-VS	10	1222	292	1298	368
VOUT	11	1222	459	1298	535
VOUT	12	1222	639	1298	715
+VS	13	1222	806	1298	882
+VS	14	993	1074	1069	1150
+VS	15	862	1074	938	1150
+VS	16	760	1074	836	1150
DNC	17	601	1074	677	1150
PD	18	431	1074	507	1150
REF	19	180	1074	256	1150

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage	Supply voltage, (+VS) – (–VS)		33	V
	Supply voltage turnon, turnoff maximum dV/dT ⁽²⁾		1	V/μs
	Input/output voltage range	(–VS) – 0.5	(+VS) + 0.5	V
	Differential input voltage		±0.5	
Current	Continuous input current ⁽³⁾		±10	mA
	Continuous output current ⁽³⁾		±100	
Temperature	Junction temperature, T _J ⁽⁴⁾	Maximum	150	°C
		Continuous operation, long-term reliability	125	
	Storage temperature, T _{stg} ⁽⁵⁾	–65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Stay below this dV/dT supply turnon and turnoff edge rate to make sure that the edge-triggered ESD absorption device across the supply pins remains open. Exceeding this supply edge rate may transiently show a short circuit across the supplies.
- (3) Long-term continuous current for electro-migration limits.
- (4) Thermal shutdown at approximately 160°C junction temperature and recovery at approximately 145°C.
- (5) See the MSL or reflow rating information provided with the material or see <https://www.ti.com> for the latest information.

8.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
(+VS) – (–VS)	Supply voltage	±7	±15	±16	V
	Dual-supply				
	Single-supply	14	30	32	
T _A	Operating free-air temperature	–40		85	°C

8.4 Thermal Information

THERMAL METRIC ⁽¹⁾		THS3491		UNIT
		DDA (HSOIC)	RGT (VQFN)	
		8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	44.5	49.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	66.8	55.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	19.2	23.1	°C/W
ψ _{JT}	Junction-to-top characterization parameter	6.4	1.8	°C/W
ψ _{JB}	Junction-to-board characterization parameter	19.5	23.2	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	7.5	7.8	°C/W

- (1) For more information about traditional and new thermalmetrics, see the [Semiconductor and IC Package ThermalMetrics](#) application report.

8.5 Electrical Characteristics: $V_S = \pm 15\text{ V}$

at $+V_S = +15\text{ V}$, $-V_S = -15\text{ V}$, $T_A \approx 25^\circ\text{C}$, $R_{LOAD} = 100\ \Omega$ to midsupply, noninverting gain (G) = 5 V/V, and RGT package: $R_F = 576\ \Omega$, $R_G = 143\ \Omega$, or DDA package: $R_F = 798\ \Omega$, $R_G = 200\ \Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level ⁽¹⁾
AC PERFORMANCE							
SSBW	Small-signal bandwidth	$V_O = 2\text{ V}_{PP}$, < 0.5-dB peaking		900		MHz	C
LSBW	Large-signal bandwidth	$V_O = 10\text{ V}_{PP}$, < 1-dB peaking		320		MHz	C
	Bandwidth for 0.2-dB flatness	$V_O = 2\text{ V}_{PP}$		350		MHz	C
SR	Slew rate (20% – 80%)	$V_O = 20\text{ V}_{PP}$		8000		V/ μs	C
	Overshoot and undershoot	$V_O = 10\text{-V}$ step (input $t_r/t_f = 1.0\text{ ns}$)		1.5%			C
t_r/t_f	Rise and fall time	$V_O = 10\text{-V}$ step (input $t_r/t_f = 1.0\text{ ns}$)		1.3		ns	C
t_s	Settling time to 0.1%	$V_O = 10\text{-V}$ step (input $t_r/t_f = 1.0\text{ ns}$)		7		ns	C
HD2	Second-order harmonic distortion	$f = 20\text{ MHz}$, $V_O = 10\text{ V}_{PP}$		–78		dBc	C
		$f = 50\text{ MHz}$, $V_O = 10\text{ V}_{PP}$		–76			
		$f = 70\text{ MHz}$, $V_O = 10\text{ V}_{PP}$		–68			
		$f = 100\text{ MHz}$, $V_O = 10\text{ V}_{PP}$		–60			
		$f = 20\text{ MHz}$, $V_O = 20\text{ V}_{PP}$		–75			
		$f = 50\text{ MHz}$, $V_O = 20\text{ V}_{PP}$		–65			
		$f = 70\text{ MHz}$, $V_O = 20\text{ V}_{PP}$		–61			
		$f = 100\text{ MHz}$, $V_O = 20\text{ V}_{PP}$		–51			
HD3	Third-order harmonic distortion	$f = 20\text{ MHz}$, $V_O = 10\text{ V}_{PP}$		–81		dBc	C
		$f = 50\text{ MHz}$, $V_O = 10\text{ V}_{PP}$		–75			
		$f = 70\text{ MHz}$, $V_O = 10\text{ V}_{PP}$		–61			
		$f = 100\text{ MHz}$, $V_O = 10\text{ V}_{PP}$		–51			
		$f = 20\text{ MHz}$, $V_O = 20\text{ V}_{PP}$		–64			
		$f = 50\text{ MHz}$, $V_O = 20\text{ V}_{PP}$		–55			
		$f = 70\text{ MHz}$, $V_O = 20\text{ V}_{PP}$		–48			
		$f = 100\text{ MHz}$, $V_O = 20\text{ V}_{PP}$		–47			
IMD2	2nd-order two-tone intermodulation distortion	$f = 20\text{ MHz}$, $V_O = 5\text{ V}_{PP}$ per tone, 100-kHz tone spacing		–79		dBc	C
IMD3	3rd-order two-tone intermodulation distortion	$f = 20\text{ MHz}$, $V_O = 5\text{ V}_{PP}$ per tone, 100-kHz tone spacing		–68		dBc	C
e_n	Input-referred voltage noise	$f \geq 100\text{ kHz}$		1.7		nV/ $\sqrt{\text{Hz}}$	C
i_{np}	Noninverting, input-referred current noise	$f \geq 100\text{ kHz}$		15		pA/ $\sqrt{\text{Hz}}$	C
i_{nn}	Inverting, input-referred current noise	$f \geq 100\text{ kHz}$		20		pA/ $\sqrt{\text{Hz}}$	C
Z_{OUT}	Closed-loop output impedance	$f = 50\text{ MHz}$		1		Ω	C
DC PERFORMANCE							
Z_{OL}	Open-loop transimpedance gain	$V_O = \pm 10\text{ V}$, $R_{LOAD} = 500\ \Omega$	5	8		M Ω	A1
V_{OS}	Input offset voltage	DDA package only	–2	1	2	mV	A1
		RGT package & DIE sales	–2.5	1	2.5	mV	A1
	Input offset voltage drift ⁽²⁾	$-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$		3		$\mu\text{V}/^\circ\text{C}$	B
I_{B+}	Noninverting input bias current ⁽³⁾		–7	–2	7	μA	A1
	Noninverting input bias current drift ⁽²⁾	$-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$		–8		nA/ $^\circ\text{C}$	B
I_{B-}	Inverting input bias current ⁽³⁾		–20	–7	20	μA	A1
	Inverting input bias current drift ⁽²⁾	$-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$		–116		nA/ $^\circ\text{C}$	B

8.5 Electrical Characteristics: $V_S = \pm 15\text{ V}$ (continued)

at $+V_S = +15\text{ V}$, $-V_S = -15\text{ V}$, $T_A \approx 25^\circ\text{C}$, $R_{\text{LOAD}} = 100\ \Omega$ to midsupply, noninverting gain (G) = 5 V/V, and RGT package: $R_F = 576\ \Omega$, $R_G = 143\ \Omega$, or DDA package: $R_F = 798\ \Omega$, $R_G = 200\ \Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level ⁽¹⁾
$R_{\text{FB_TRACE}}$	Internal trace resistance to feedback pin	RGT only, pins 10 and 11 to pin 1	1.1	1.5	1.9	Ω	A2
CMRR	Common-mode rejection ratio	$f = \text{DC}$	69	75		dB	A1
INPUT							
HR_{IN}	Headroom to either supply	CMRR > 60 dB		4.1	4.3	V	A2
$Z_{\text{IN}+}$	Noninverting input impedance	Closed-loop measurement	$50 \parallel 1.2$			$\text{k}\Omega \parallel \text{pF}$	C
$Z_{\text{IN}-}$	Inverting input impedance	Open-loop measurement	8	15	18	Ω	B
OUTPUT							
HR_{OUT}	Headroom to either supply		1.2	1.5	1.7	V	A1
I_{outMAX}	Maximum current output	$R_{\text{LOAD}} = 24\ \Omega$, $V_O = \pm 12.67\text{ V}$, magnitude, both polarities	480	520	550	mA	A2
$\text{I}_{\text{outLINEAR}}$	Linear output current	$R_{\text{LOAD}} = 24\ \Omega$, $V_O = \pm 9.4\text{ V}$, $Z_{\text{OL}} > 1\text{ M}\Omega$, source and sink	380	420		mA	A2
$\text{I}_{\text{outPEAK}}$	Peak output current in transition (transition peak at zero-crossing I_{OUT})	$V_O = 0\text{ V}$, $R_O < 0.5\ \Omega$, magnitude, both polarities	500	540		mA	B
I_{SC}	Output short-circuit current	$V_S = \pm 9\text{ V}$, $V_O = \pm 6\text{ V}$, magnitude, both polarities	550	620		mA	B
Z_{OUT}	DC output impedance	Closed-loop ($\pm 50\text{ mA}$)		0.17		Ω	C
POWER SUPPLY							
I_Q	Quiescent current	$V_S = \pm 15\text{ V}$, No load	16.1	16.7	17.3	mA	A1
		$V_S = \pm 16\text{ V}$, No load	16.2	16.8	17.4	mA	A2
		$V_S = \pm 7\text{ V}$, No load	15.2	15.8	16.3	mA	A1
$\text{I}_Q\text{ TC}$		$V_S = \pm 15\text{ V}$, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, No load		5		$\mu\text{A}/^\circ\text{C}$	B
PSRR+	Positive power supply rejection ratio	$+V_S \pm 1.5\text{ V}$, $-V_S$	78	82		dB	A1
PSRR–	Negative power supply rejection ratio	$+V_S$, $-V_S \pm 1.5\text{ V}$	77	80		dB	A1
POWER DOWN							
$\text{REF}_{\text{RANGE}}$	REF pin voltage range	Do NOT float the REF pin.	$-V_S$ GND	$+V_S - 5\text{ V}$		V	A2
$\text{I}_{\text{REF_BIAS}}$	REF pin bias current	REF = 0 V, $\overline{\text{PD}} = \text{REF} + 3\text{ V}$, positive out of the pin.	35	46	52	μA	A2
V_{IL}	Disable voltage threshold	REF = 0 V, guaranteed off below			0.8	V	A1
V_{IH}	Enable voltage threshold	REF = 0 V, guaranteed on above	1.5			V	A1
$\overline{\text{PD}}_{\text{LOW_BIAS}}$	$\overline{\text{PD}}$ pin low input bias current	$\overline{\text{PD}} = \text{REF} = \text{GND}$, positive out of the pin.	17	21	25	μA	A2
$\overline{\text{PD}}_{\text{HIGH_BIAS}}$	$\overline{\text{PD}}$ pin high input bias current	$\overline{\text{PD}} = \text{REF} + 3\text{ V}$, REF = GND, positive out of the pin.	–1	0	1	μA	A2
$\text{I}_{\text{Q_OFF_}+V_S}$	$+V_S$ disabled supply current		650	780	880	μA	A1
$\text{I}_{\text{Q_OFF_} -V_S}$	$-V_S$ disabled supply current		600	723	820	μA	A2
t_{ON}	Turnon time delay	DC output to 90% of final value		50		ns	C
t_{OFF}	Turnoff time delay	DC output to 10% of final value		4		μs	C
JUNCTION-TEMPERATURE SENSE, $T_{\text{J_SENSE}}$ (QFN-16 ONLY, PIN 6)							
	$T_{\text{J_SENSE}}$ 25°C value	Device disabled (22°C to 32°C ATE ambient temperature)	0.915	1.06	1.15	V	A2
	$T_{\text{J_SENSE}}$ temperature coefficient	$T_J = 0^\circ\text{C}$ to 125°C		3.2		$\text{mV}/^\circ\text{C}$	B

8.5 Electrical Characteristics: $V_S = \pm 15\text{ V}$ (continued)

at $+V_S = +15\text{ V}$, $-V_S = -15\text{ V}$, $T_A \cong 25^\circ\text{C}$, $R_{\text{LOAD}} = 100\ \Omega$ to midsupply, noninverting gain (G) = 5 V/V, and RGT package: $R_F = 576\ \Omega$, $R_G = 143\ \Omega$, or DDA package: $R_F = 798\ \Omega$, $R_G = 200\ \Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level ⁽¹⁾
	T_{J_SENSE} input impedance	Internally connected to REF pin	32.4	35	38	k Ω	A2

- (1) Test levels (all values set by characterization and simulation): (A1) 100% tested at $\approx 25^\circ\text{C}$ for all devices, overtemperature limits by characterization and simulation; (A2) 100% tested at $\approx 25^\circ\text{C}$ for packaged devices, not tested in production for die sales (B) Not tested in production, limits set by characterization and simulation; (C) Typical value only for information;
- (2) Input offset voltage drift and input bias current drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range.
- (3) Current is considered positive out of the pin.

8.6 Electrical Characteristics: $V_S = \pm 7.5\text{ V}$

at $+V_S = +7.5\text{ V}$, $-V_S = -7.5\text{ V}$, $T_A \approx 25^\circ\text{C}$, $R_{LOAD} = 100\ \Omega$ to midsupply, noninverting gain (G) = 5 V/V, and RGT package: $R_F = 576\ \Omega$, $R_G = 143\ \Omega$, or DDA package: $R_F = 798\ \Omega$, $R_G = 200\ \Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level ⁽¹⁾
AC PERFORMANCE							
SSBW	Small-signal bandwidth	$V_O = 2\text{ V}_{PP}$, < 0.5-dB peaking		800		MHz	C
LSBW	Large-signal bandwidth	$V_O = 5\text{ V}_{PP}$, < 1-dB peaking		550		MHz	C
SR	Slew rate (20%-80%)	$V_O = 10\text{ V}_{PP}$		6000		V/ μs	C
HD2	Second-order harmonic distortion	$f = 20\text{ MHz}$, $V_O = 5\text{ V}_{PP}$		-83		dBc	C
HD3	Third-order harmonic distortion	$f = 20\text{ MHz}$, $V_O = 5\text{ V}_{PP}$		-78		dBc	C
e_n	Input-referred voltage noise	$f \geq 100\text{ kHz}$		1.7		nV/ $\sqrt{\text{Hz}}$	C
i_{np}	Noninverting, input-referred current noise	$f \geq 100\text{ kHz}$		15		pA/ $\sqrt{\text{Hz}}$	C
i_{nn}	Inverting, input-referred current noise	$f \geq 100\text{ kHz}$		20		pA/ $\sqrt{\text{Hz}}$	C
Z_{OUT}	Closed-loop output impedance	$f = 50\text{ MHz}$		1		Ω	C
DC PERFORMANCE							
Z_{OL}	Open-loop transimpedance gain	$V_O = \pm 2.5\text{ V}$, $R_{LOAD} = 500\ \Omega$	6	14		M Ω	A1
V_{OS}	Input offset voltage	DDA package limits	-2	1	2	mV	A1
		RGT package & die sales limits	-2.5	1	2.5	mV	A1
	Input offset-voltage drift ⁽²⁾	$-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$		3		$\mu\text{V}/^\circ\text{C}$	B
I_{B+}	Noninverting input bias current ⁽³⁾		-7	-2	7	μA	A1
	Noninverting input bias current drift ⁽²⁾	$-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$		-10		nA/ $^\circ\text{C}$	B
I_{B-}	Inverting input bias current ⁽³⁾		-19	-6	19	μA	A1
	Inverting input bias current drift ⁽²⁾	$-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$		-112		nA/ $^\circ\text{C}$	B
INPUT							
Z_{IN+}	Noninverting input impedance	Closed-loop measurement	35 1.2			k Ω pF	C
Z_{IN-}	Inverting input impedance	Open-loop measurement		15		Ω	C
HR_{IN}	Headroom to either supply	CMRR > 60 dB		4.1	4.3	V	B
OUTPUT							
HR_{OUT}	Headroom to either supply		1.2	1.5	1.7	V	A1
I_{OUT_LINEAR}	Linear output current	$R_{LOAD} = 24\ \Omega$, $V_O = \pm 5\text{ V}$, $Z_{OL} > 1\text{ M}\Omega$, source and sink	200	230		mA	A2
POWER SUPPLY							
I_Q	Quiescent current	No load	15.2	15.8	16.4	mA	A1
POWER DOWN							
REF_{RANGE}	REF pin voltage range	Do NOT float the REF pin.	$-V_S$	GND	$+V_S - 5\text{ V}$	V	B
I_{REF_BIAS}	REF pin bias current	REF = 0 V, $\overline{PD} = \text{REF} + 3\text{ V}$, positive out of the pin	35	37	52	μA	A2
V_{IL}	Disable voltage threshold	REF = 0 V, guaranteed off below			0.8	V	A1
V_{IH}	Enable voltage threshold	REF = 0 V, guaranteed on above	1.5			V	A1
$\overline{PD}_{LOW_BIAS}$	$\overline{PD}$ pin low input bias current	$\overline{PD} = \text{REF} = \text{GND}$, positive out of the pin.	17	21	25	μA	A2
$\overline{PD}_{HIGH_BIAS}$	$\overline{PD}$ pin high input bias current	$\overline{PD} = \text{REF} + 3\text{ V}$, REF = GND, positive out of the pin.	-1	0	1	μA	A2
$I_{Q_OFF_+VS}$	+Vs disabled supply current		600	700	850	μA	A1
$I_{Q_OFF_ -VS}$	-Vs disabled supply current		550	642	770	μA	A2
JUNCTION-TEMPERATURE SENSE, T_{J_SENSE} (QFN-16 ONLY, PIN 6)							

8.6 Electrical Characteristics: $V_S = \pm 7.5\text{ V}$ (continued)

at $+V_S = +7.5\text{ V}$, $-V_S = -7.5\text{ V}$, $T_A \cong 25^\circ\text{C}$, $R_{\text{LOAD}} = 100\ \Omega$ to midsupply, noninverting gain (G) = 5 V/V, and RGT package: $R_F = 576\ \Omega$, $R_G = 143\ \Omega$, or DDA package: $R_F = 798\ \Omega$, $R_G = 200\ \Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level ⁽¹⁾
	T_{J_SENSE} 25°C value	Device disabled (22°C to 32°C ATE ambient temperature)	0.915	1.06	1.15	V	A2
	T_{J_SENSE} temperature coefficient	$T_J = 0^\circ\text{C}$ to 125°C		3.2		mV/°C	B
	T_{J_SENSE} input impedance	Internally connected to REF pin	32.4	35	38	k Ω	B

- (1) Test levels (all values set by characterization and simulation): (A1) 100% tested at $\cong 25^\circ\text{C}$ for all devices, overtemperature limits by characterization and simulation; (A2) 100% tested at $\cong 25^\circ\text{C}$ for packaged devices, not tested in production for die sales (B) Not tested in production, limits set by characterization and simulation; (C) Typical value only for information;
- (2) Input offset voltage drift and input bias current drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range.
- (3) Current is considered positive out of the pin.

8.7 Typical Characteristics: ± 15 V

at $+V_S = 15$ V, $-V_S = -15$ V, $T_A \cong 25^\circ\text{C}$, $R_{\text{LOAD}} = 100\ \Omega$ to midsupply, noninverting gain (G) = 5 V/V. RGT package : $R_F = 576\ \Omega$, $R_G = 143\ \Omega$, or DDA package: $R_F = 798\ \Omega$, $R_G = 200\ \Omega$ (unless otherwise noted)

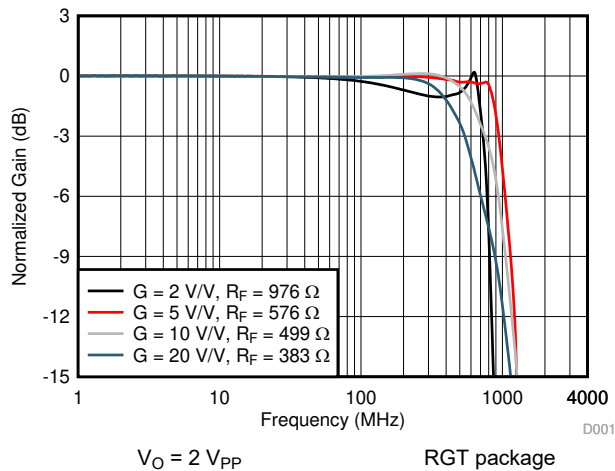


Figure 8-1. Noninverting Small-Signal Frequency Response

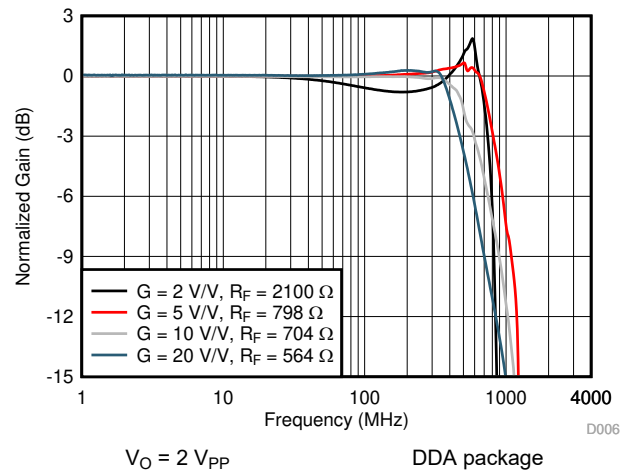


Figure 8-2. Noninverting Small-Signal Frequency Response

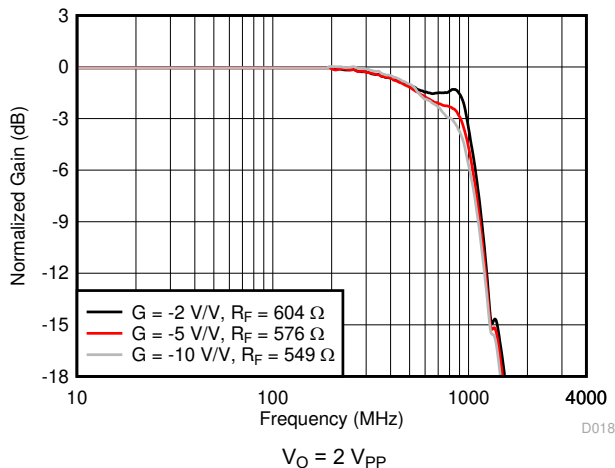


Figure 8-3. Inverting Small-Signal Frequency Response

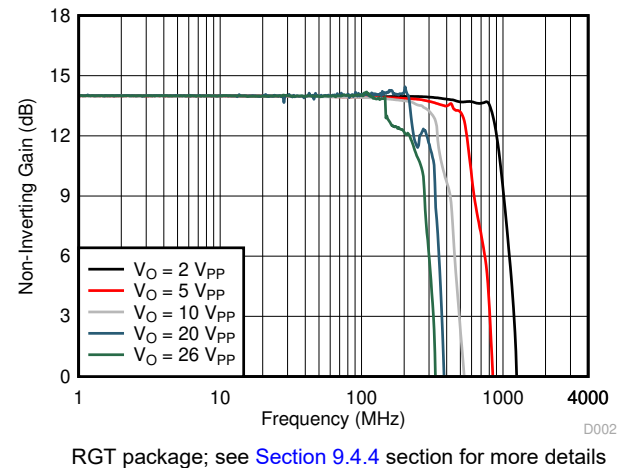


Figure 8-4. Frequency Response vs Output Swing

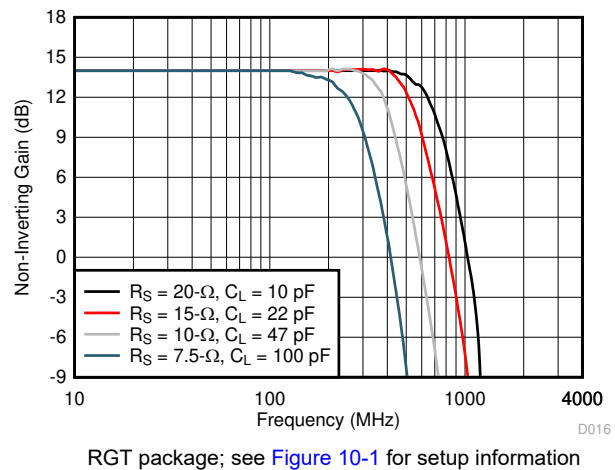


Figure 8-5. Frequency Response vs C_{LOAD}

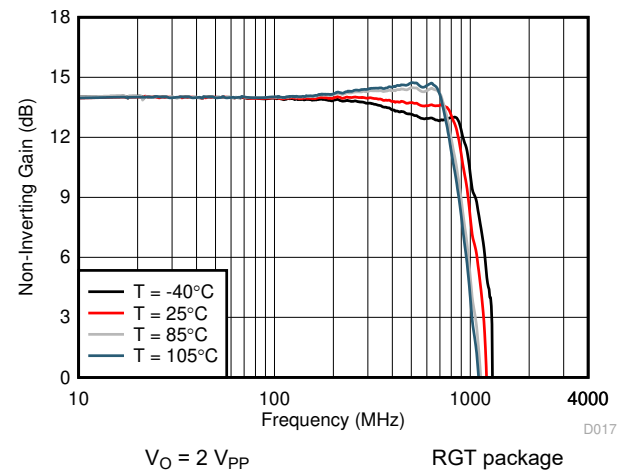


Figure 8-6. Frequency Response vs Temperature

8.7 Typical Characteristics: ± 15 V (continued)

at $+V_S = 15$ V, $-V_S = -15$ V, $T_A \cong 25^\circ\text{C}$, $R_{\text{LOAD}} = 100\ \Omega$ to midsupply, noninverting gain (G) = 5 V/V. RGT package : $R_F = 576\ \Omega$, $R_G = 143\ \Omega$, or DDA package: $R_F = 798\ \Omega$, $R_G = 200\ \Omega$ (unless otherwise noted)

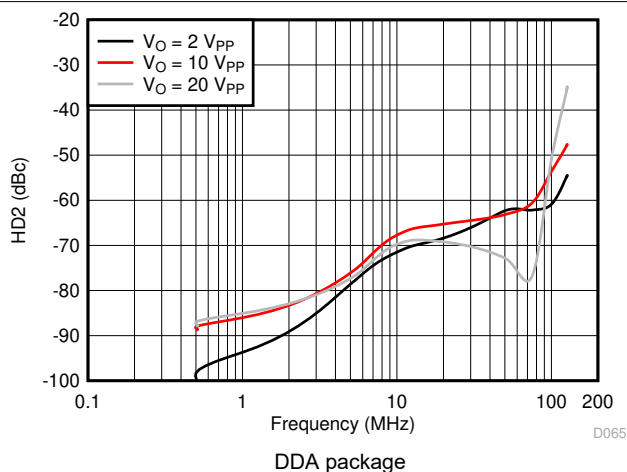


Figure 8-7. HD2 vs Frequency

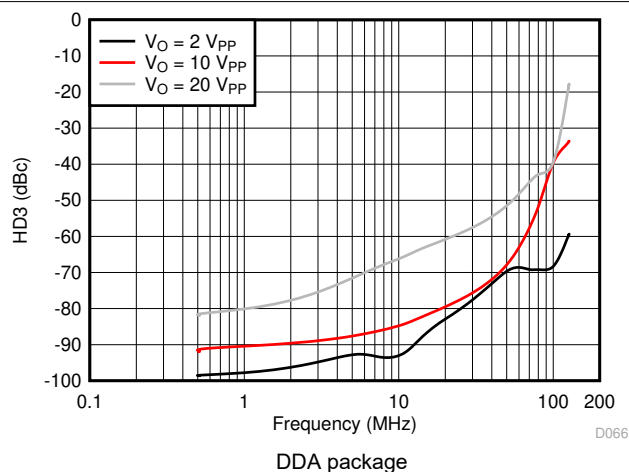


Figure 8-8. HD3 vs Frequency

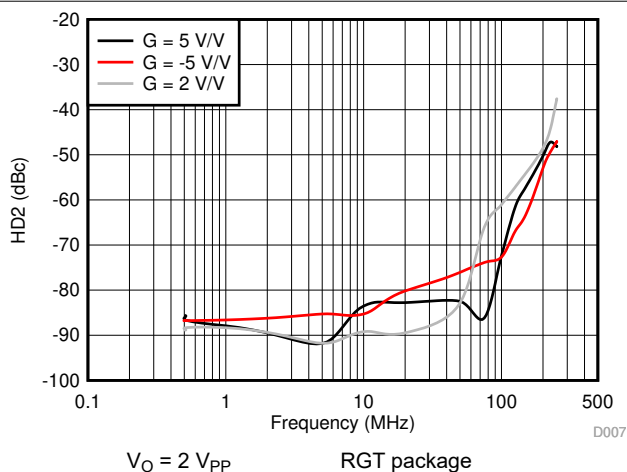


Figure 8-9. HD2 vs Frequency

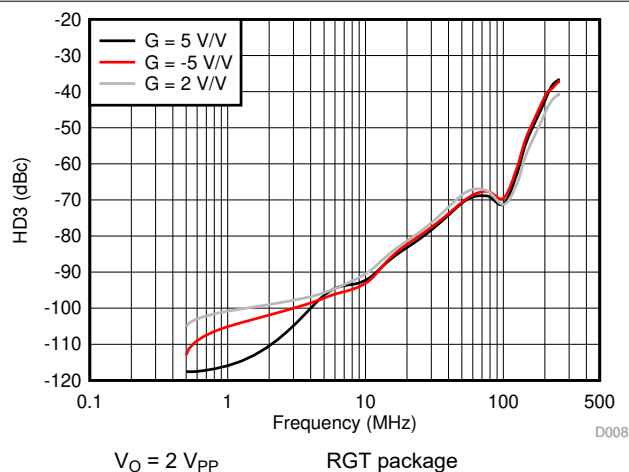


Figure 8-10. HD3 vs Frequency

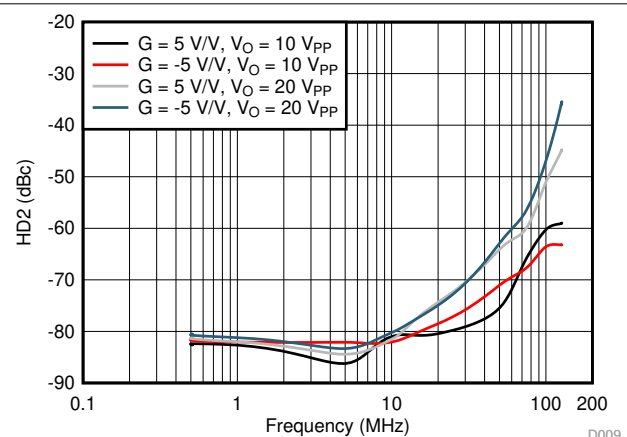


Figure 8-11. HD2 vs Frequency Across Output Swing

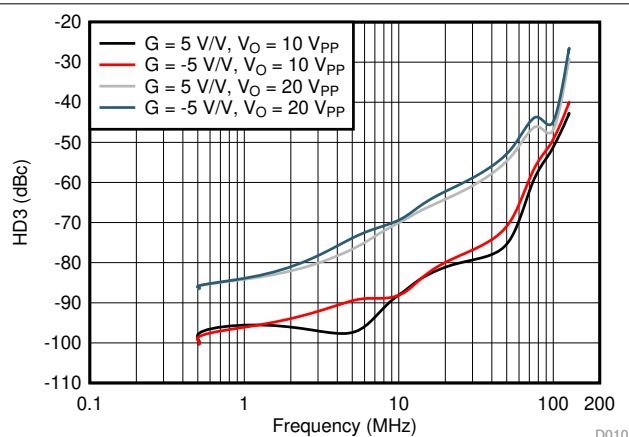


Figure 8-12. HD3 vs Frequency Across Output Swing

8.7 Typical Characteristics: ± 15 V (continued)

at $+V_S = 15$ V, $-V_S = -15$ V, $T_A \cong 25^\circ\text{C}$, $R_{LOAD} = 100\ \Omega$ to midsupply, noninverting gain (G) = 5 V/V. RGT package : $R_F = 576\ \Omega$, $R_G = 143\ \Omega$, or DDA package: $R_F = 798\ \Omega$, $R_G = 200\ \Omega$ (unless otherwise noted)

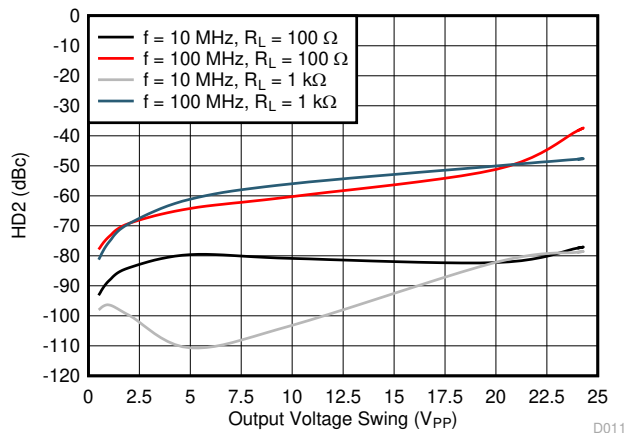


Figure 8-13. HD2 vs Output Swing

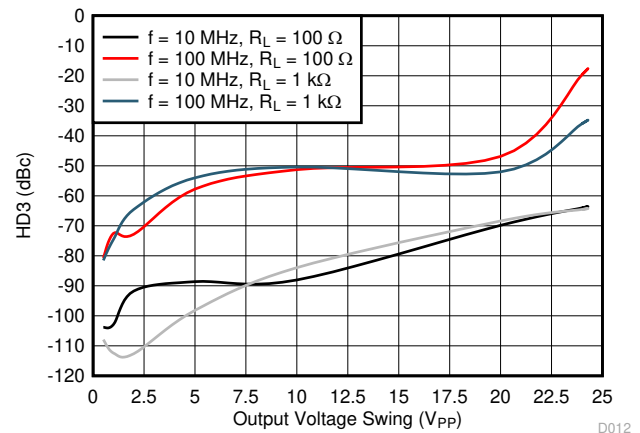


Figure 8-14. HD3 vs Output Swing

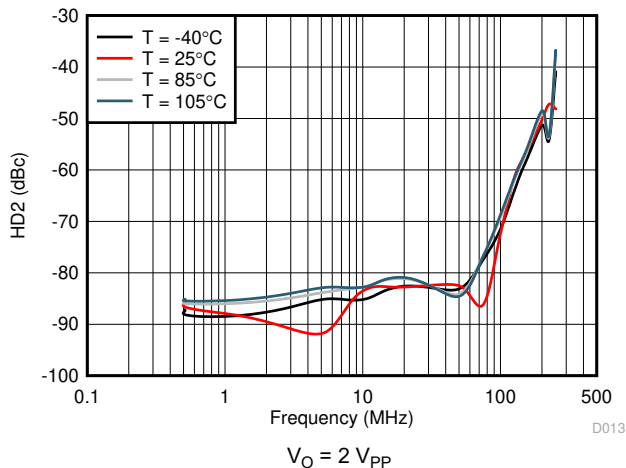


Figure 8-15. HD2 vs Frequency Across Temperature

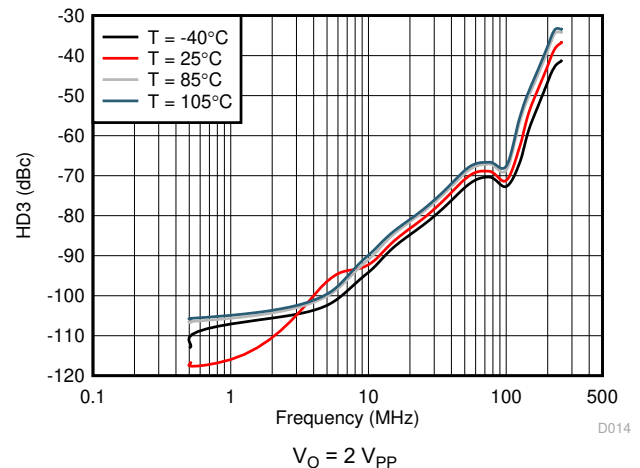


Figure 8-16. HD3 vs Frequency Across Temperature

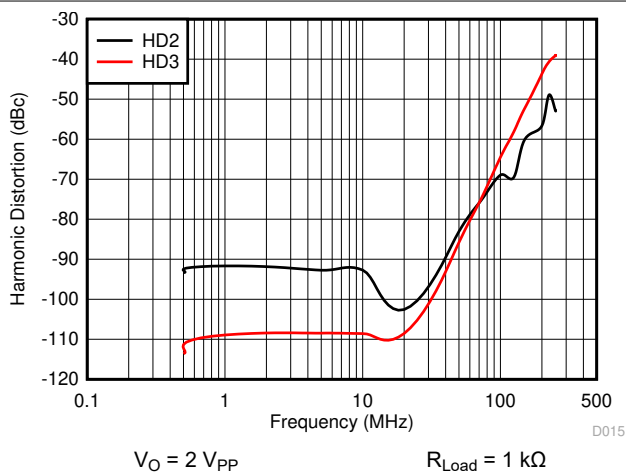


Figure 8-17. Harmonic Distortion vs Frequency

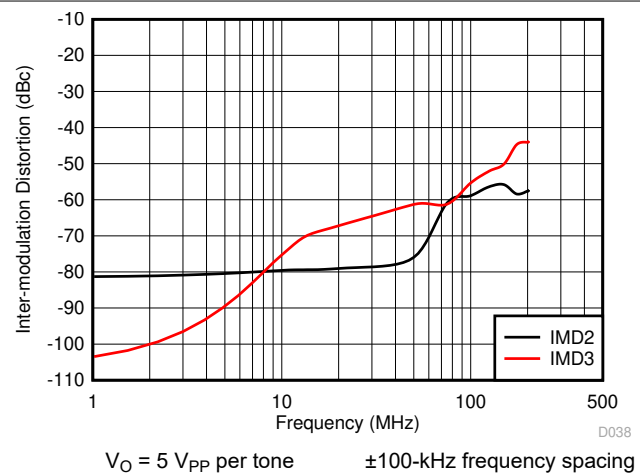
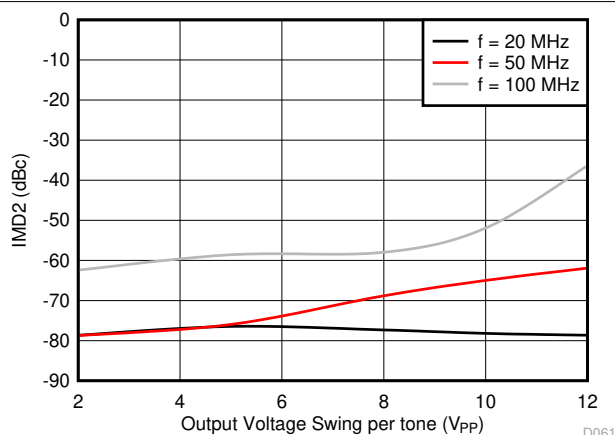


Figure 8-18. Intermodulation Distortion vs Frequency

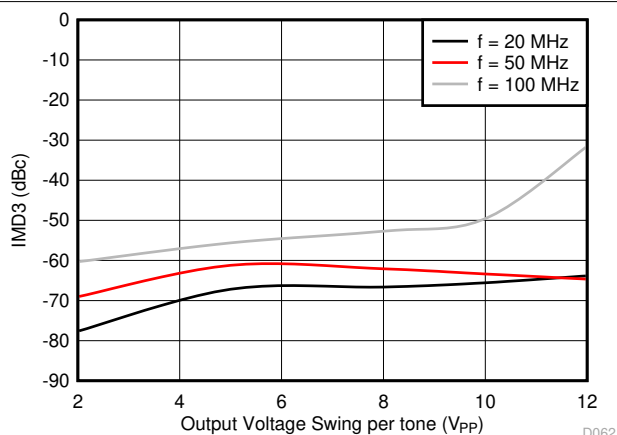
8.7 Typical Characteristics: ± 15 V (continued)

at $+V_S = 15$ V, $-V_S = -15$ V, $T_A \cong 25^\circ\text{C}$, $R_{\text{LOAD}} = 100\ \Omega$ to midsupply, noninverting gain (G) = 5 V/V. RGT package : $R_F = 576\ \Omega$, $R_G = 143\ \Omega$, or DDA package: $R_F = 798\ \Omega$, $R_G = 200\ \Omega$ (unless otherwise noted)



± 100 -kHz frequency spacing

Figure 8-19. IMD2 vs Output Voltage Swing



± 100 -kHz frequency spacing

Figure 8-20. IMD3 vs Output Voltage Swing

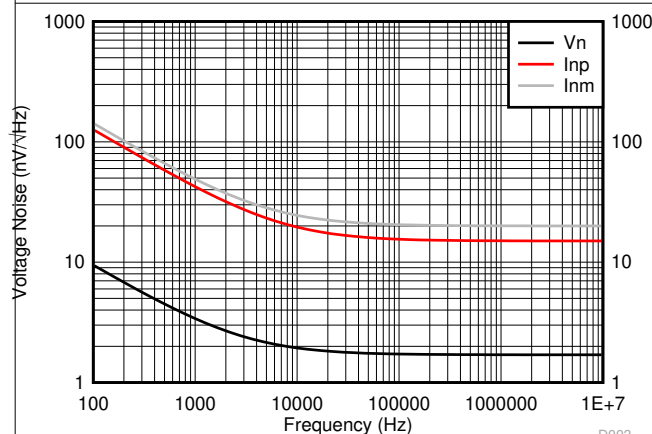
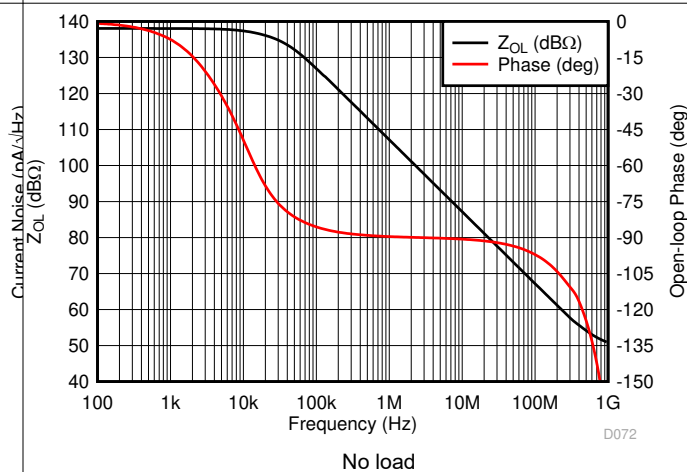
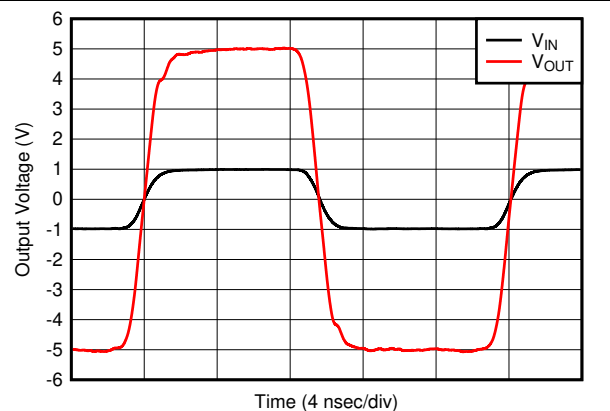


Figure 8-21. Spot Input Noise vs Frequency



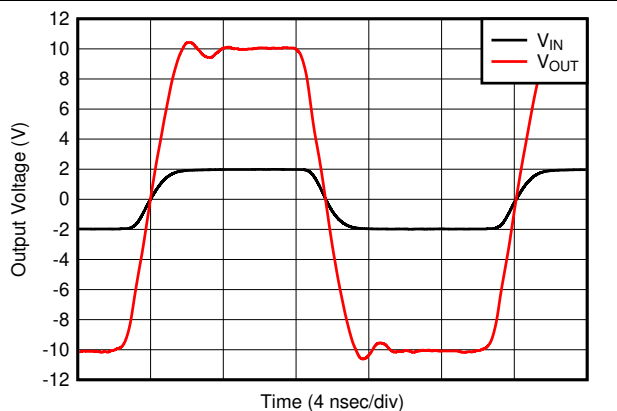
No load

Figure 8-22. Open-Loop Transimpedance Gain and Phase vs Frequency



$V_O = 10\ V_{PP}$

Figure 8-23. $G = 5$ V/V Pulse Response

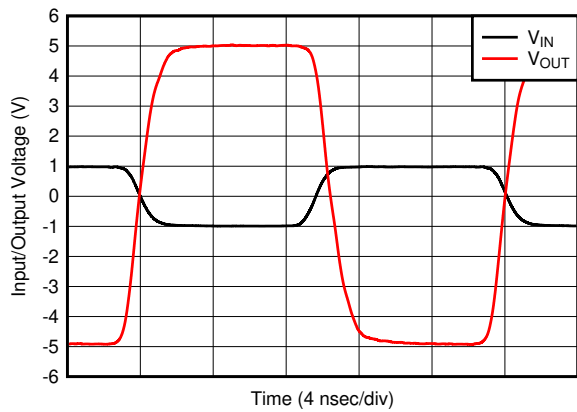


$V_O = 20\ V_{PP}$

Figure 8-24. $G = 5$ V/V Pulse Response

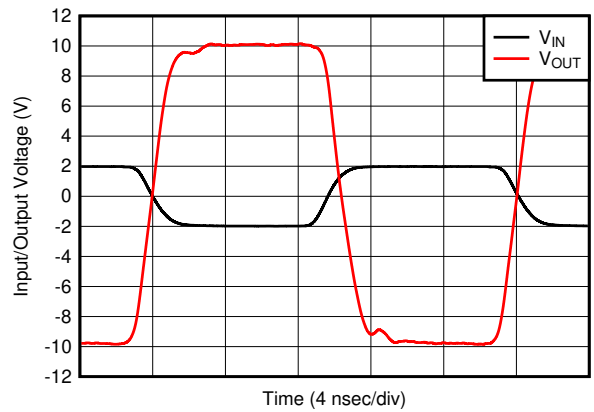
8.7 Typical Characteristics: ± 15 V (continued)

at $+V_S = 15$ V, $-V_S = -15$ V, $T_A \cong 25^\circ\text{C}$, $R_{\text{LOAD}} = 100\ \Omega$ to midsupply, noninverting gain (G) = 5 V/V. RGT package : $R_F = 576\ \Omega$, $R_G = 143\ \Omega$, or DDA package: $R_F = 798\ \Omega$, $R_G = 200\ \Omega$ (unless otherwise noted)



$V_O = 10\text{ V}_{\text{PP}}$

Figure 8-25. $G = -5$ V/V Pulse Response



$V_O = 20\text{ V}_{\text{PP}}$

Figure 8-26. $G = -5$ V/V Pulse Response

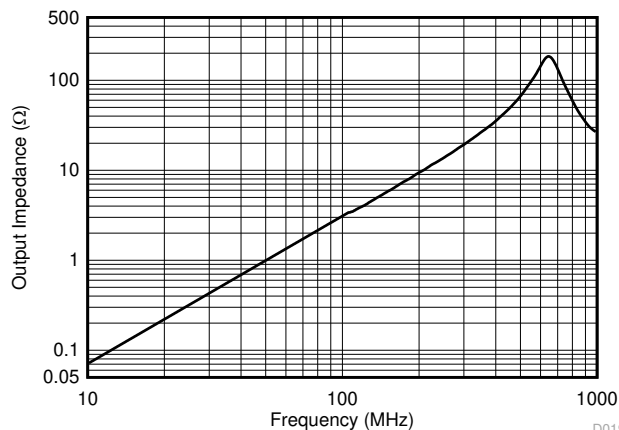


Figure 8-27. Output Impedance vs Frequency

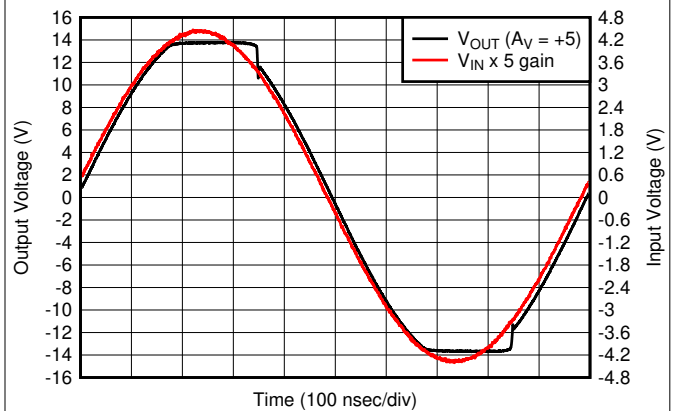


Figure 8-28. Overdrive Recovery Time

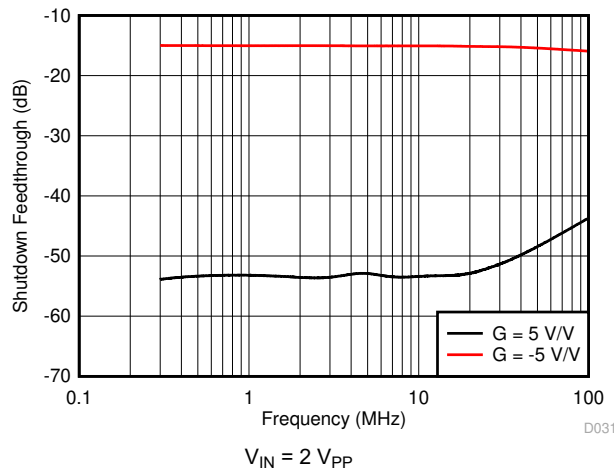


Figure 8-29. Shutdown Feedthrough vs Frequency

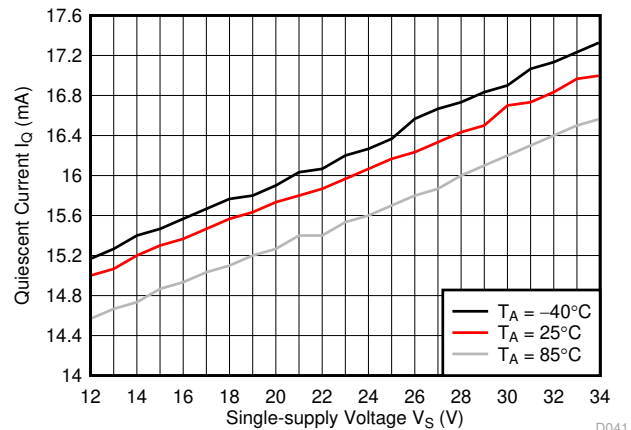
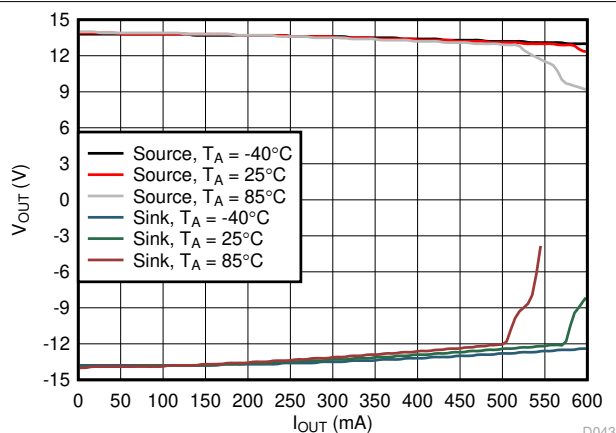


Figure 8-30. Quiescent Current vs Supply Voltage

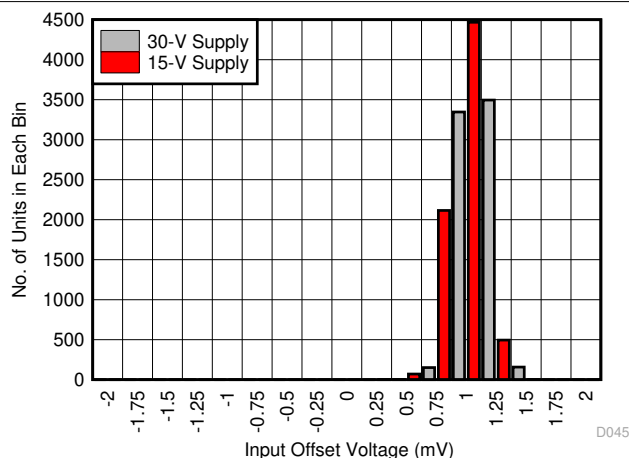
8.7 Typical Characteristics: ± 15 V (continued)

at $+V_S = 15$ V, $-V_S = -15$ V, $T_A \cong 25^\circ\text{C}$, $R_{\text{LOAD}} = 100\ \Omega$ to midsupply, noninverting gain (G) = 5 V/V. RGT package : $R_F = 576\ \Omega$, $R_G = 143\ \Omega$, or DDA package: $R_F = 798\ \Omega$, $R_G = 200\ \Omega$ (unless otherwise noted)



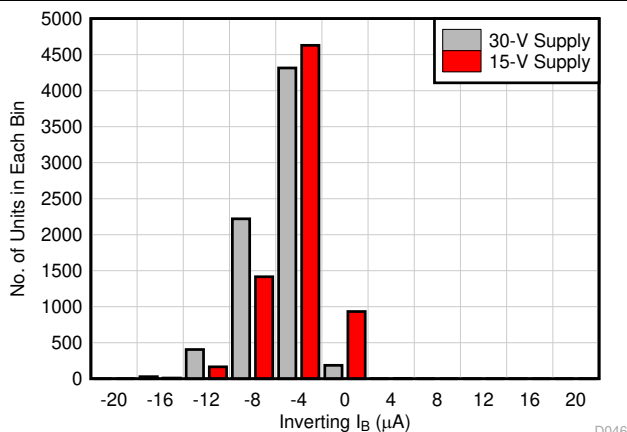
A. Measured with devices soldered on TI EVM. Devices not turned off at any read points but load applied for a few milliseconds to measure V_{OUT} and then removed.

Figure 8-31. Output Voltage Swing vs Output Current



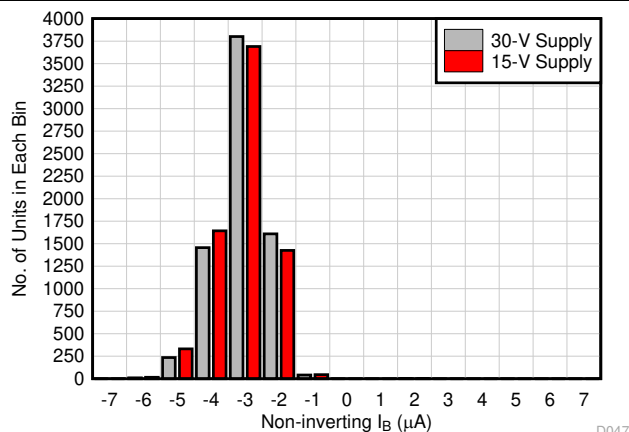
7100 units at each supply

Figure 8-32. Input Offset Voltage Distribution



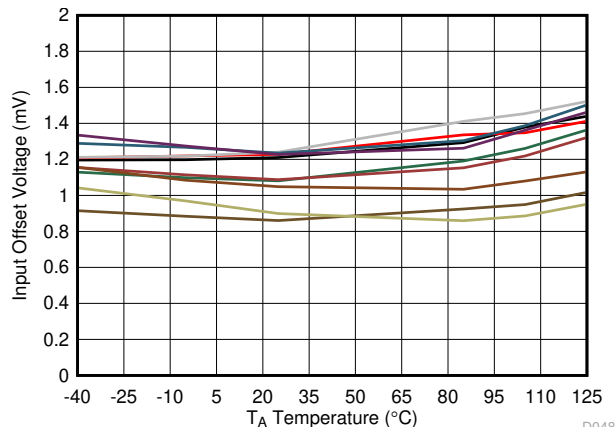
7100 units at each supply

Figure 8-33. Inverting I_B Distribution



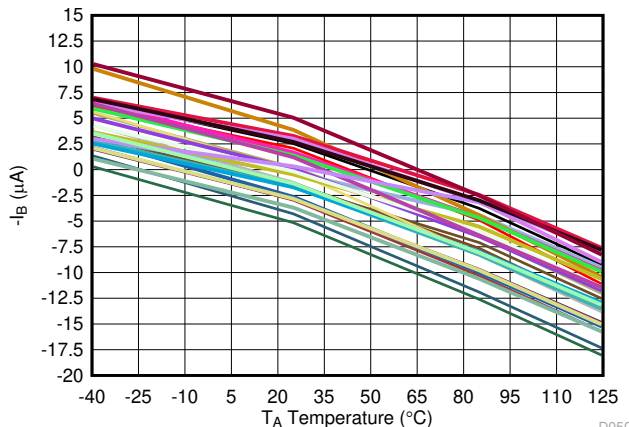
7100 units at each supply

Figure 8-34. Noninverting I_B Distribution



Flash tested to keep T_J as close to T_A as possible

Figure 8-35. Input Offset Voltage Over Temperature



Flash tested to keep T_J as close to T_A as possible

Figure 8-36. Inverting I_B Over Temperature

8.7 Typical Characteristics: ± 15 V (continued)

at $+V_S = 15$ V, $-V_S = -15$ V, $T_A \cong 25^\circ\text{C}$, $R_{\text{LOAD}} = 100\ \Omega$ to midsupply, noninverting gain (G) = 5 V/V. RGT package : $R_F = 576\ \Omega$, $R_G = 143\ \Omega$, or DDA package: $R_F = 798\ \Omega$, $R_G = 200\ \Omega$ (unless otherwise noted)

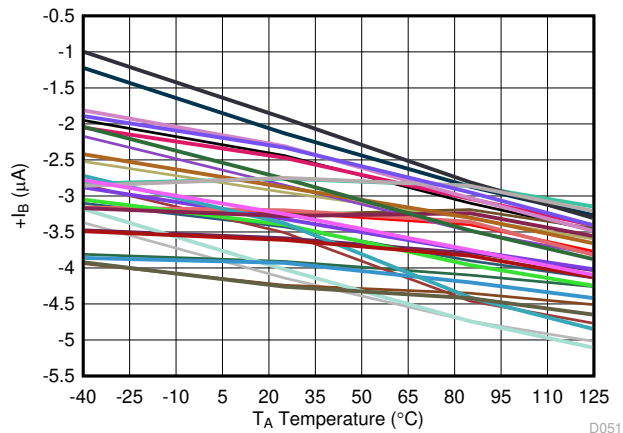


Figure 8-37. Noninverting I_B Over Temperature

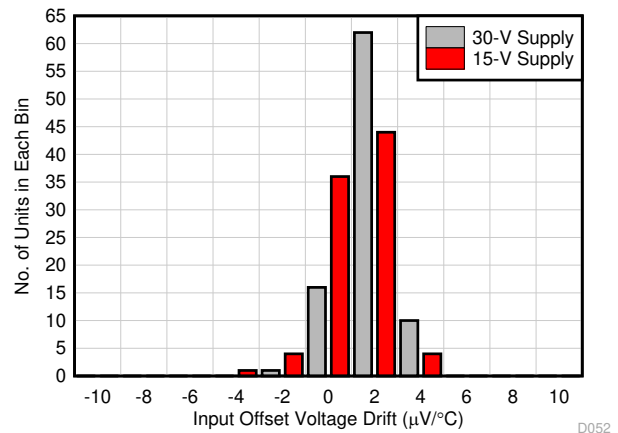


Figure 8-38. Input Offset Voltage Drift Histogram

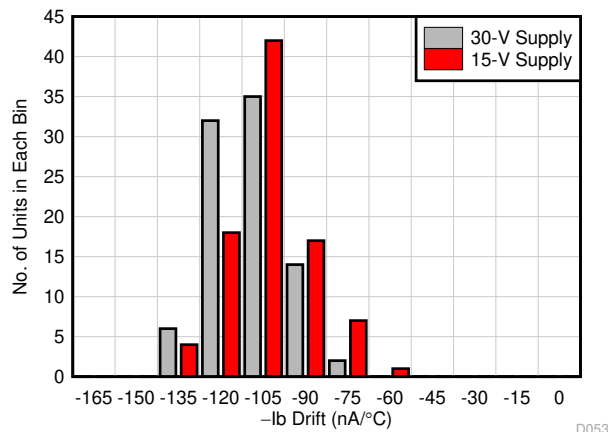


Figure 8-39. Inverting I_B Drift Histogram

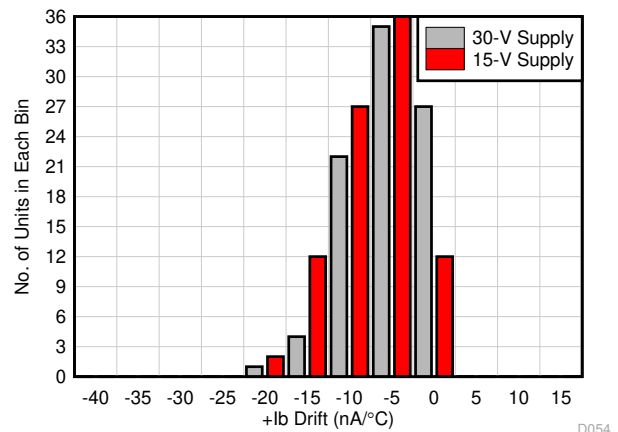
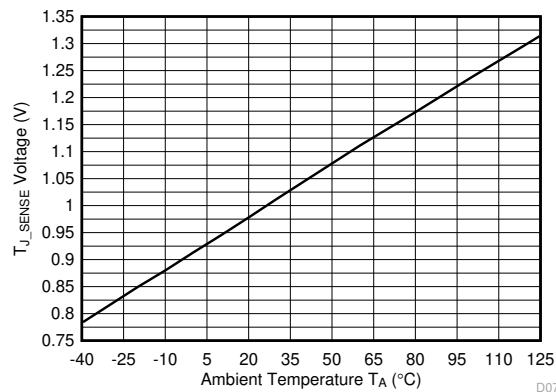


Figure 8-40. Noninverting I_B Drift Histogram



Device in shutdown mode to minimize self-heating, RGT package

Figure 8-41. T_{J_SENSE} Voltage vs Ambient Temperature

8.8 Typical Characteristics: ± 7.5 V

at $+V_S = 7.5$ V, $-V_S = -7.5$ V, $T_A \cong 25^\circ\text{C}$, $R_{\text{LOAD}} = 100\ \Omega$ to midsupply, noninverting gain (G) = 5 V/V RGT package: $R_F = 576\ \Omega$, $R_G = 143\ \Omega$, or DDA package: $R_F = 798\ \Omega$, $R_G = 200\ \Omega$ (unless otherwise noted)

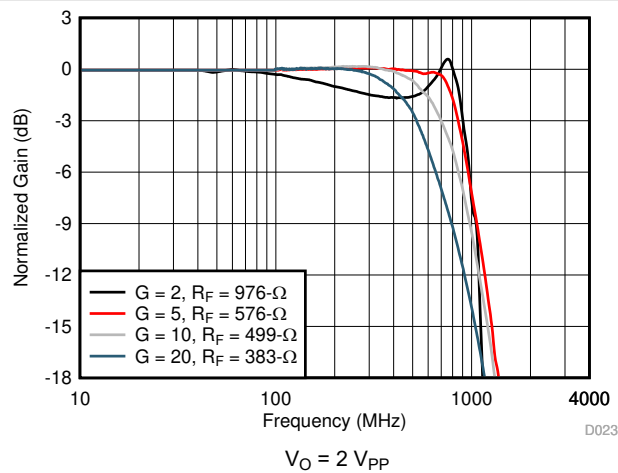


Figure 8-42. Noninverting Small-Signal Frequency Response

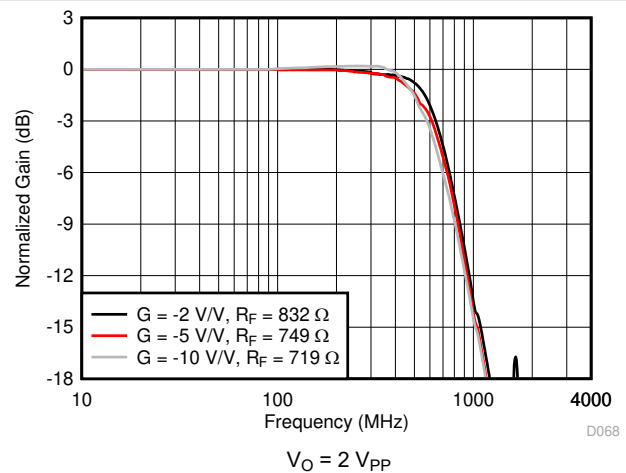


Figure 8-43. Inverting Small-Signal Frequency Response

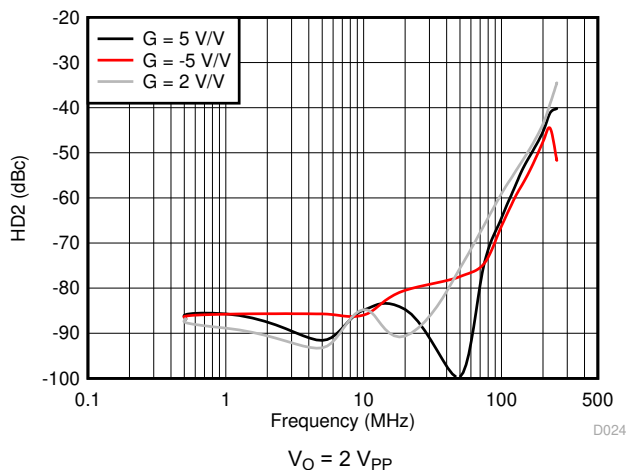


Figure 8-44. HD2 vs Frequency

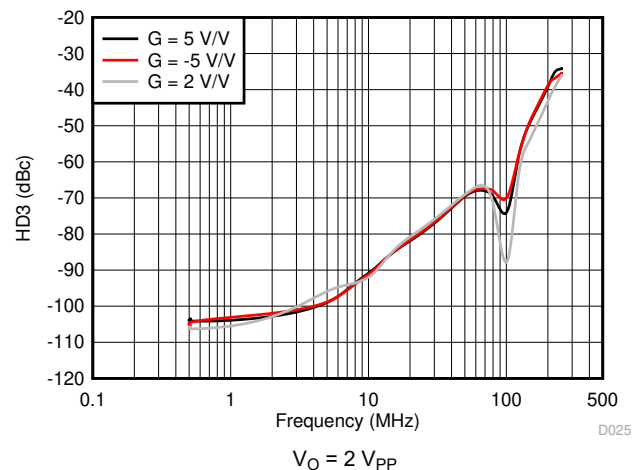


Figure 8-45. HD3 vs Frequency

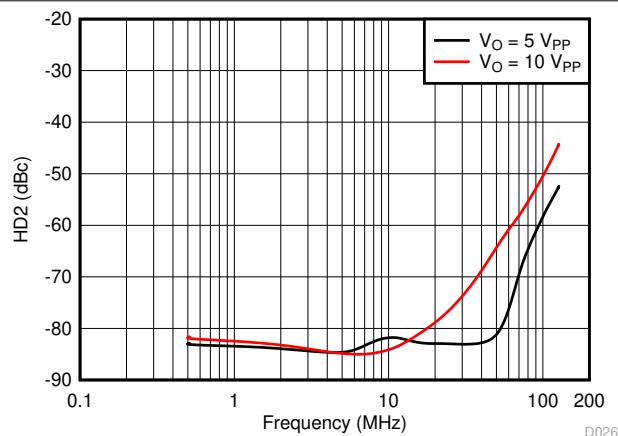


Figure 8-46. HD2 vs Frequency Across Output Swing

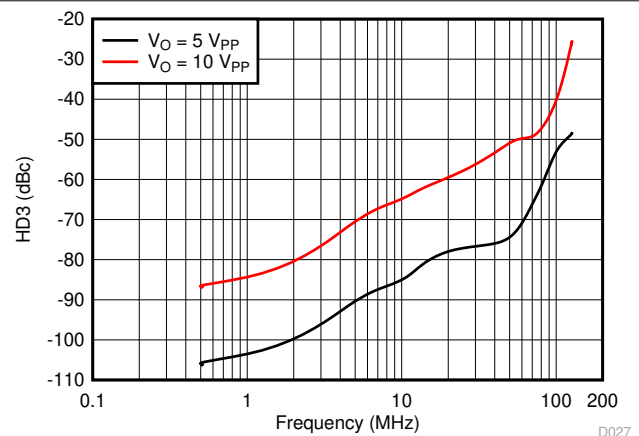


Figure 8-47. HD3 vs Frequency Across Output Swing

8.8 Typical Characteristics: ± 7.5 V (continued)

at $+V_S = 7.5$ V, $-V_S = -7.5$ V, $T_A \cong 25^\circ\text{C}$, $R_{LOAD} = 100\ \Omega$ to midsupply, noninverting gain (G) = 5 V/V RGT package: $R_F = 576\ \Omega$, $R_G = 143\ \Omega$, or DDA package: $R_F = 798\ \Omega$, $R_G = 200\ \Omega$ (unless otherwise noted)

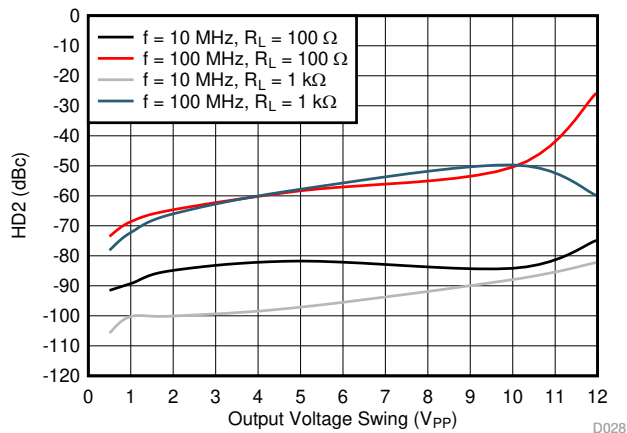


Figure 8-48. HD2 vs Output Swing

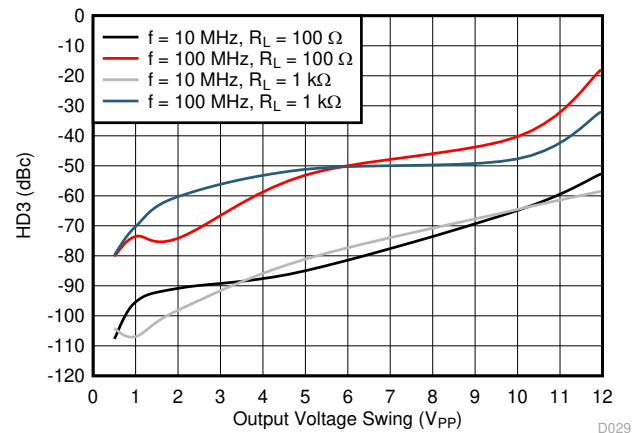


Figure 8-49. HD3 vs Output Swing

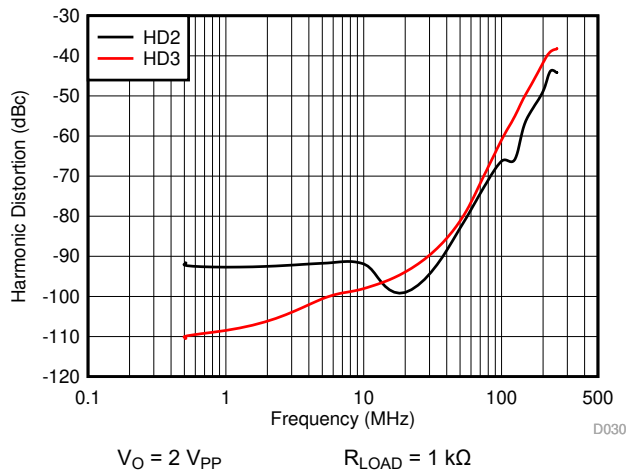


Figure 8-50. Harmonic Distortion vs Frequency

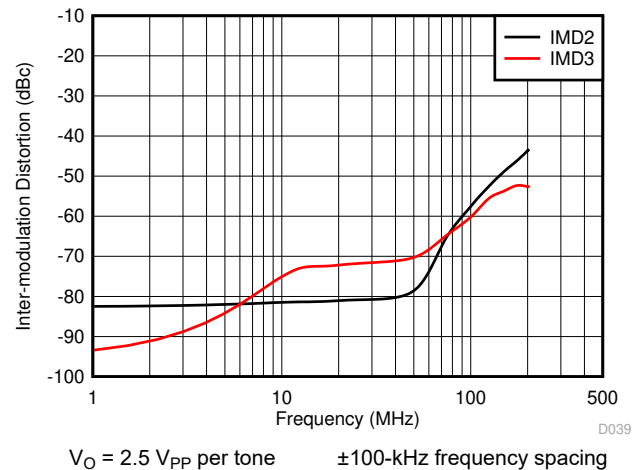


Figure 8-51. Intermodulation Distortion vs Frequency

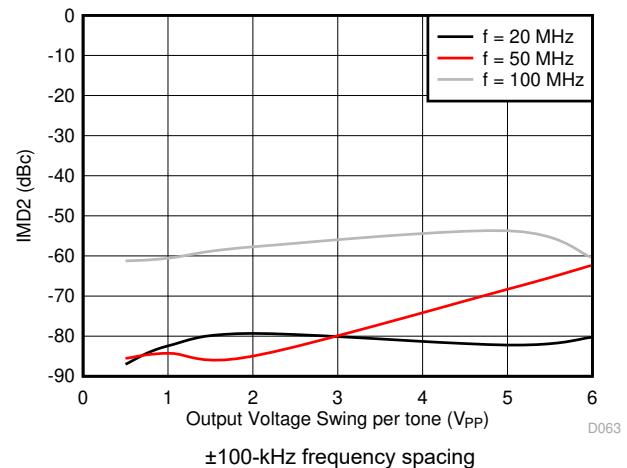


Figure 8-52. IMD2 vs Output Voltage Swing

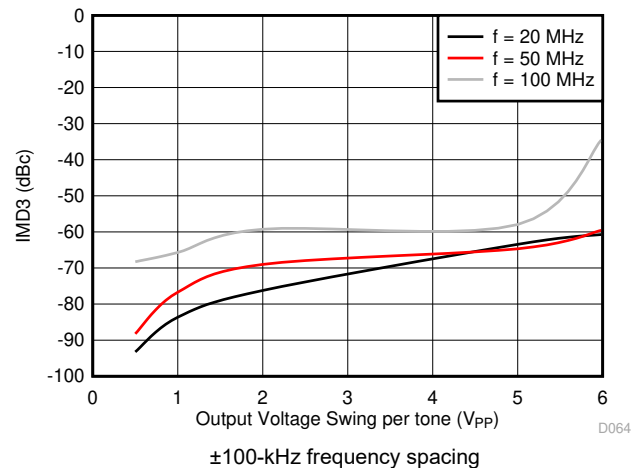


Figure 8-53. IMD3 vs Output Voltage Swing

8.8 Typical Characteristics: ± 7.5 V (continued)

at $+V_S = 7.5$ V, $-V_S = -7.5$ V, $T_A \cong 25^\circ\text{C}$, $R_{LOAD} = 100\ \Omega$ to midsupply, noninverting gain (G) = 5 V/V RGT package: $R_F = 576\ \Omega$, $R_G = 143\ \Omega$, or DDA package: $R_F = 798\ \Omega$, $R_G = 200\ \Omega$ (unless otherwise noted)

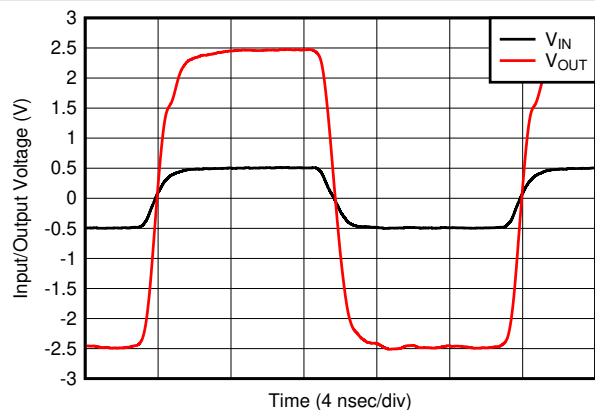

 $V_O = 5\text{ V}_{PP}$

Figure 8-54. $G = 5$ V/V Pulse Response

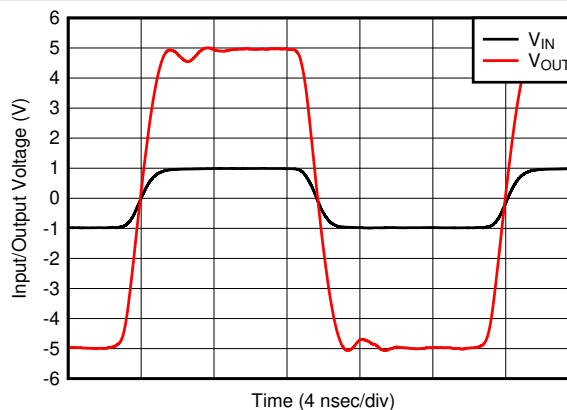

 $V_O = 10\text{ V}_{PP}$

Figure 8-55. $G = 5$ V/V Pulse Response

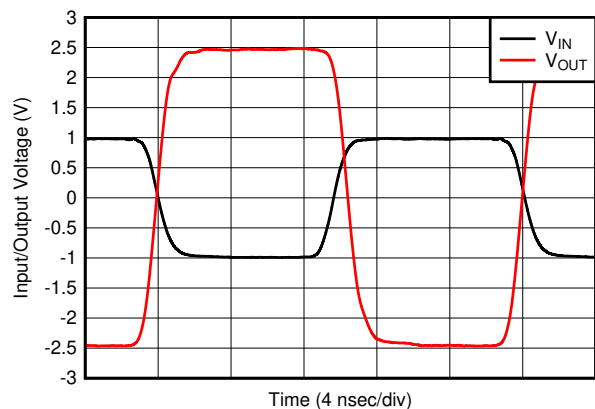

 $V_O = 5\text{ V}_{PP}$

Figure 8-56. $G = -5$ V/V Pulse Response

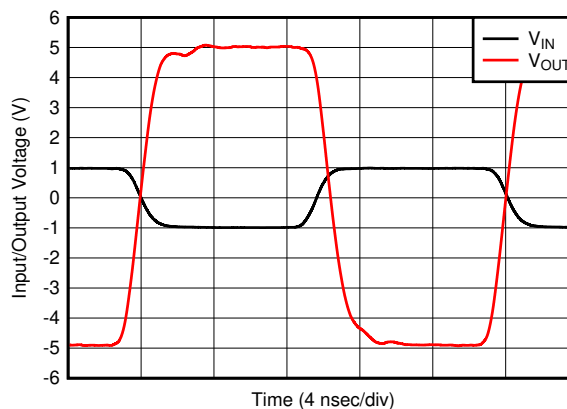

 $V_O = 10\text{ V}_{PP}$

Figure 8-57. $G = -5$ V/V Pulse Response

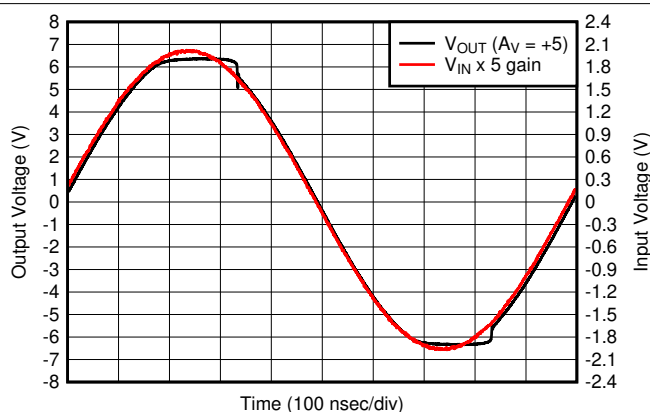
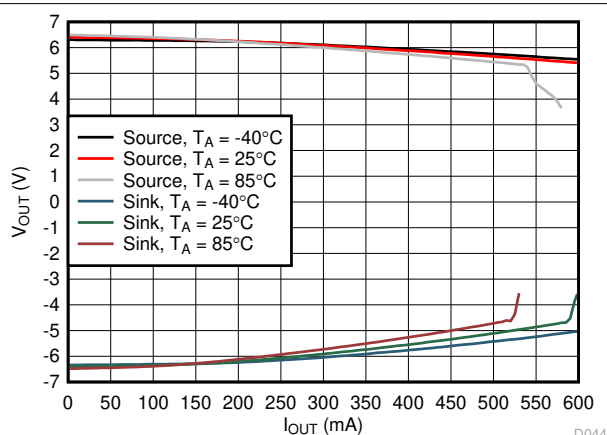


Figure 8-58. Overdrive Recovery Time

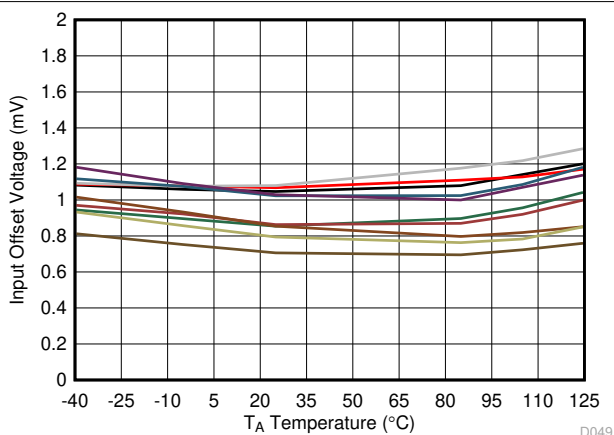


Measured with devices soldered on TI EVM. Devices not turned off at any read points but load applied for a few msec to measure V_{OUT} and then removed.

Figure 8-59. Output Voltage Swing vs Output Current

8.8 Typical Characteristics: ± 7.5 V (continued)

at $+V_S = 7.5$ V, $-V_S = -7.5$ V, $T_A \cong 25^\circ\text{C}$, $R_{\text{LOAD}} = 100\ \Omega$ to midsupply, noninverting gain (G) = 5 V/V RGT package: $R_F = 576\ \Omega$, $R_G = 143\ \Omega$, or DDA package: $R_F = 798\ \Omega$, $R_G = 200\ \Omega$ (unless otherwise noted)



Flash tested to keep T_J as close to T_A as possible

Figure 8-60. Input Offset Voltage Over Temperature

9 Detailed Description

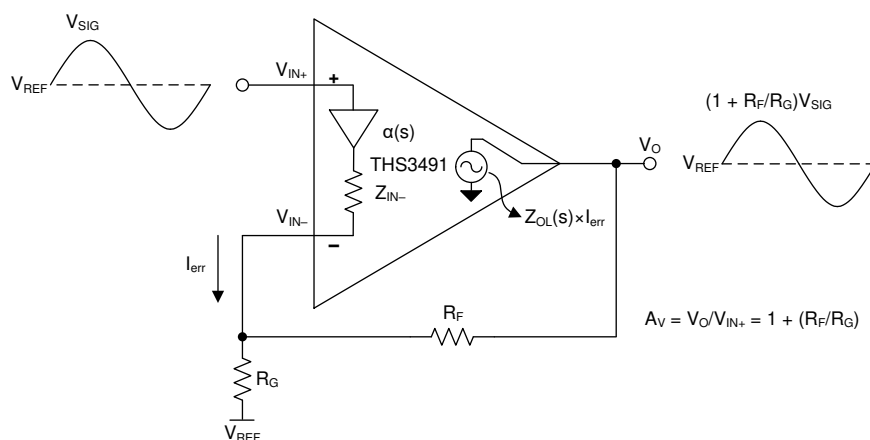
9.1 Overview

The THS3491 is a high-voltage, low-distortion, high-speed, current-feedback amplifier designed to operate over a wide supply range of ± 7 V to ± 16 V for applications requiring large, linear output swings such as arbitrary waveform generators.

The THS3491 features a power-down pin that puts the amplifier in low power standby mode and lowers the quiescent current from 16.7 mA to 750 μ A.

The RGT package also features a feedback pin (pin 1). Internally on the die this pin is connected to the amplifier's output. This feedback pin arrangement minimizes the PCB trace lengths in the feedback path for the connection from the feedback resistor to the inverting input and output pins. This in turn minimizes the board parasitics in the feedback path, thus allowing to maximize bandwidth with minimal peaking.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Power-Down ($\overline{\text{PD}}$) Pin

The THS3491 features a power-down ($\overline{\text{PD}}$) pin that lowers the quiescent current from 16.7 mA down to 750 μA , which is designed to reduce system power.

The power-down pin of the amplifier defaults to 2 V below the positive supply voltage in the absence of an externally applied voltage, which places the amplifier in the power-on mode of operation. To turn off the amplifier in an effort to conserve power, the power-down pin can be pulled low. The $\overline{\text{PD}}$ pin threshold voltages are specified with respect to the REF pin voltage. The threshold voltages for power on and power down are relative to the REF pin and are shown in the [Section 8.5](#) and [Section 8.6](#) tables. Above the enable threshold voltage, the device is on. Below the disable threshold voltage, the device is off. The behavior is not specified between these threshold voltages.

This power-down functionality helps the amplifier consume less power in power-down mode. Power-down mode is not intended to provide a high-impedance output. The power-down functionality is not intended for use as a tri-state bus driver. In power-down mode, the impedance looking back into the output of the amplifier is dominated by the feedback and gain-setting resistors, but the output impedance of the device varies depending on the voltage applied to the outputs.

As with most current-feedback amplifiers, the internal architecture places limitations on the system in power-down mode. The most common limitation is that the amplifier turns on if there is a ± 1 V or greater difference between the two input nodes ($\text{VIN}+$ and $\text{VIN}-$) of the amplifier. If this difference exceeds ± 1 V, the amplifier creates an output voltage equal to approximately $[(\text{VIN}+ - \text{VIN}-) - 0.7 \text{ V}] \times \text{gain}$. Conversely if a voltage is applied to the output while in power-down mode, the $\text{VIN}-$ node voltage is equal to $V_{\text{O}(\text{applied})} \times R_{\text{G}} / (R_{\text{F}} + R_{\text{G}})$. For low-gain configurations and a large applied voltage at the output, the amplifier may turn on because of the aforementioned behavior.

The time delays associated with turning the device on and off are specified as the time it takes for the amplifier to reach 10% or 90% of the final output voltage. The time delays are in nanoseconds during power on and microseconds during power off because the amplifier moves out of linear operating mode for power-off conditions.

9.3.2 Power-Down Reference (REF) Pin

In addition to the power-down pin, the DDA package features a reference pin (REF) that allows control over the enable or disable power-down voltage levels applied to the $\overline{\text{PD}}$ pin. This reference pin is explicitly pinned out on the DDA package as the REF pin. However, on the RGT package, the reference pin refers to pin 5 (GND), which must be connected to GND. In most split-supply applications, the reference pin is connected to ground. In either case, be aware of voltage-level thresholds that apply to the power-down pin. Table 9-1 provides examples and shows the relationship between the reference voltage and the power-down thresholds. In Table 9-1, the threshold levels are derived by the conditions that follow:

- $\overline{\text{PD}} \leq \text{REF} + 0.8 \text{ V}$ (Disable)
- $\overline{\text{PD}} \geq \text{REF} + 1.5 \text{ V}$ (Enable)

where the usable range at the REF pin is:

- $V_{S-} \leq V_{\text{REF}} \leq (V_{S+} - 5 \text{ V})$

Table 9-1. Example Power-Down Threshold Voltage Levels

SUPPLY VOLTAGE (V)	REFERENCE PIN VOLTAGE (V)	ENABLE LEVEL (V)	DISABLE LEVEL (V)
$\pm 15, \pm 7, 30$	0	1.5	0.8
± 15	2	3.5	2.8
± 15	-2	-0.5	-1.2
± 7	1	2.5	1.8
± 7	-1	0.5	-0.2
30	15	16.5	15.8
14	7	8.5	7.8

The recommended operating mode is to tie the REF pin to ground for single and split-supply operations, which sets the enable and disable thresholds to 1.5 V and 0.8 V, respectively.

The REF pin must be tied to a valid potential within the recommended operating range of $(-V_S \leq V_{(\text{REF})} \leq +V_S - 5 \text{ V})$. Although the $\overline{\text{PD}}$ pin can be floated, TI does not recommend floating the $\overline{\text{PD}}$ pin in case stray signals couple into the pin and cause unintended turnon or turnoff device behavior. However, if the $\overline{\text{PD}}$ pin is left unterminated, the $\overline{\text{PD}}$ pin floats to 2 V below the positive rail and the device remains enabled. As a result, the THS3491 DDA package is a drop-in replacement for the THS3091 DDA pinout if the REF pin (pin 1) is tied to a valid potential. If balanced, split supplies are used ($\pm V_S$) and the REF and $\overline{\text{PD}}$ pins are grounded, the device is disabled.

9.3.3 Internal Junction Temperature Sense ($T_{\text{J_SENSE}}$) Pin

The RGT package includes an internal, junction-temperature sense pin ($T_{\text{J_SENSE}}$). This pin is a temperature-dependent current source from the positive supply into one side of the internal resistor, where the other side of the internal resistor is connected to pin 5 (GND), the $\overline{\text{PD}}$ logic reference pin on the die. For simplicity, and to keep the $T_{\text{J_SENSE}}$ output ground referenced, tie pin 5 to ground (internally, the $\overline{\text{PD}}$ logic reference pin). If pin 5 is tied to a voltage in the same range as the REF pin voltage for the DDA package, the output of the $T_{\text{J_SENSE}}$ voltage and input threshold voltages of the $\overline{\text{PD}}$ pin are level shifted.

9.4 Device Functional Modes

9.4.1 Wideband Noninverting Operation

The THS3491 is a 900-MHz current-feedback operational amplifier that is designed to operate from a power supply of ± 7 V to ± 16 V.

Figure 9-1 shows the THS3491 in a noninverting gain configuration of 5 V/V which is used to generate the majority of the performance curves. Most of the curves are characterized using signal sources with a 50- Ω source impedance and measurement equipment presenting a 50- Ω load impedance.

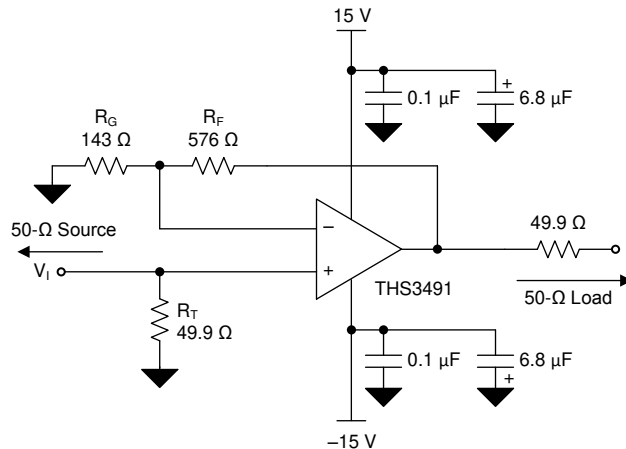


Figure 9-1. Wideband Noninverting Gain Configuration (5 V/V)

Current-feedback amplifiers are highly dependent on the R_F feedback resistor for maximum performance and stability. Table 9-2 provides the optimal resistor values for R_F and R_G at different gains to achieve maximum bandwidth with minimal peaking in the frequency response. Use lower R_F values for higher bandwidth. Note that this can cause additional peaking and a reduction in phase margin. Conversely, increasing R_F decreases the bandwidth but phase margin increases and stability improves. To gain further insight on the feedback and stability analysis of current-feedback amplifiers like the THS3491, see the [Current-feedback Amplifiers](#) section of [TI Precision Labs](#).

**Table 9-2. Recommended Resistor Values for Minimum Peaking and Optimal Frequency Response
With $R_{LOAD} = 100 \Omega$**

GAIN (V/V)	RGT PACKAGE		DDA PACKAGE	
	$R_G (\Omega)$	$R_F (\Omega)$	$R_G (\Omega)$	$R_F (\Omega)$
2	976	976	2.1k	2.1k
5	143	576	200	798
10	54.9	499	78.7	704
20	20	383	29.4	564

9.4.2 Wideband, Inverting Operation

Figure 9-2 shows the THS3491 in a typical inverting gain configuration where the input and output impedances and signal gain from Figure 9-1 are retained in an inverting circuit configuration.

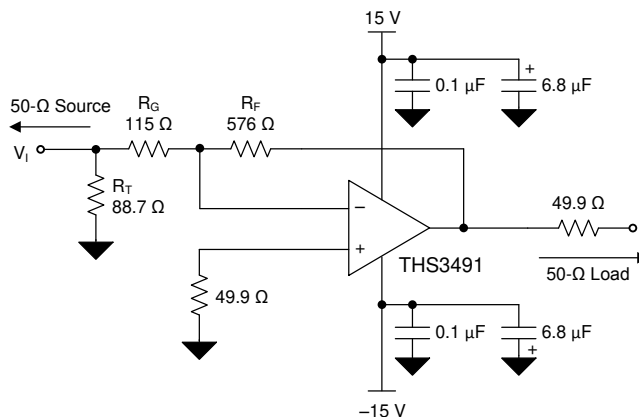


Figure 9-2. Wideband Inverting Gain Configuration (5 V/V)

9.4.3 Single-Supply Operation

The THS3491 operates from a single-supply voltage ranging from 14 V to 32 V. When operating from a single power supply, biasing the input and output at midsupply allows for the maximum output voltage swing. Figure 9-3 shows circuits that display noninverting (a) and inverting (b) amplifiers that are configured for single-supply operation.

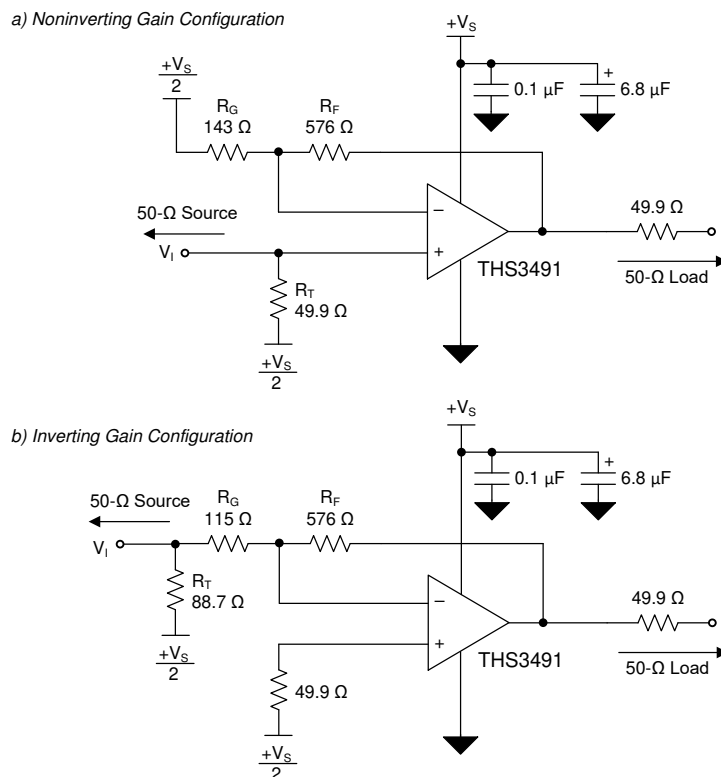


Figure 9-3. DC-Coupled, Single-Supply Operation

9.4.4 Maximum Recommended Output Voltage

The THS3491 is designed to produce better than 40 dB SFDR while driving a 100-MHz, 20-V_{pp} signal into a 100-Ω load. To accomplish this, the geometries of certain signal path transistors must be limited. As a result of this limitation, some internal devices begin to saturate when large signal levels are input at frequencies greater than 100 MHz. When these devices saturate, the loop opens and the amplifier is no longer in linear operation. This appears as a gain step-up in the frequency response curve. To avoid this phenomenon, applications must comply with the recommended linear operating region shown in Figure 9-4. Figure 9-4 shows the maximum output voltage vs frequency that is permitted to keep the amplifier in linear operation.

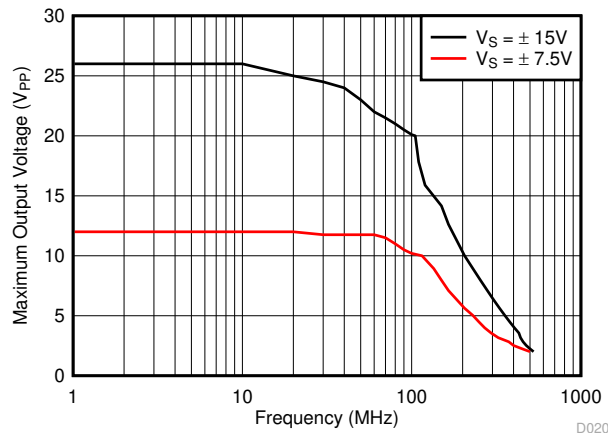


Figure 9-4. Maximum Recommended Output Voltage vs Frequency

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Driving Capacitive Loads

Applications such as power JFET and MOSFET (power FET) drivers are highly capacitive and cause stability problems for high-speed amplifiers.

Figure 10-1 and Figure 10-2 show recommended methods for driving capacitive loads. The basic idea is to use a resistor or ferrite chip to isolate the phase shift at high frequency caused by the capacitive load from the amplifier feedback path. The output impedance of the amplifier in conjunction with C_{LOAD} introduces a pole in the open-loop transimpedance gain response and if the pole is at a frequency lower than the non-dominant pole of the amplifier, then this results in a reduced loop gain and a reduced phase margin. The isolation resistor introduces a zero in the response, which counteracts the effect of the pole. The location of the zero is dependent on the values of R_{ISO} and C_{LOAD} . Figure 8-5 shows examples of the recommended R_{ISO} values to achieve flat frequency response while driving certain capacitive loads. See [Effect of Parasitic Capacitance in Op Amp Circuits](#) for a detailed analysis of selecting isolation resistor values while driving capacitive loads.

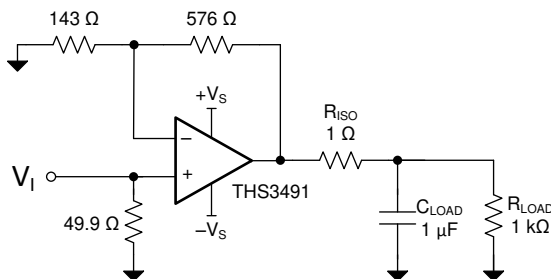


Figure 10-1. Driving a Large Capacitive Load Using an Output Series Isolation Resistor

Placing a small series resistor (R_{ISO}) between the output of the amplifier and the capacitive load as Figure 10-1 shows is a simple way to isolate the load capacitance.

Figure 10-2 shows two amplifiers in parallel to double the output drive current in order to drive larger capacitive loads. This technique is used when more output current is required to charge and discharge the load faster, such as driving large FET transistors.

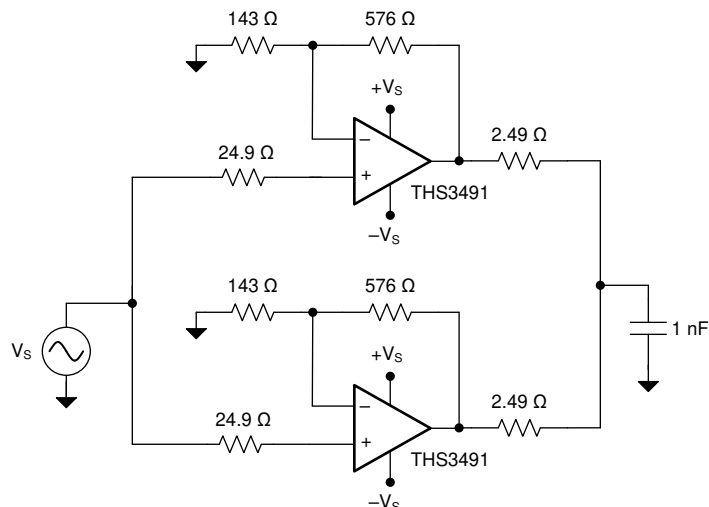


Figure 10-2. Driving a Large Capacitive Load Using Two Parallel Amplifier Channels

Figure 10-3 shows a push-pull FET driver circuit commonly used in ultrasound applications with isolation resistors to isolate the gate capacitance from the amplifier.

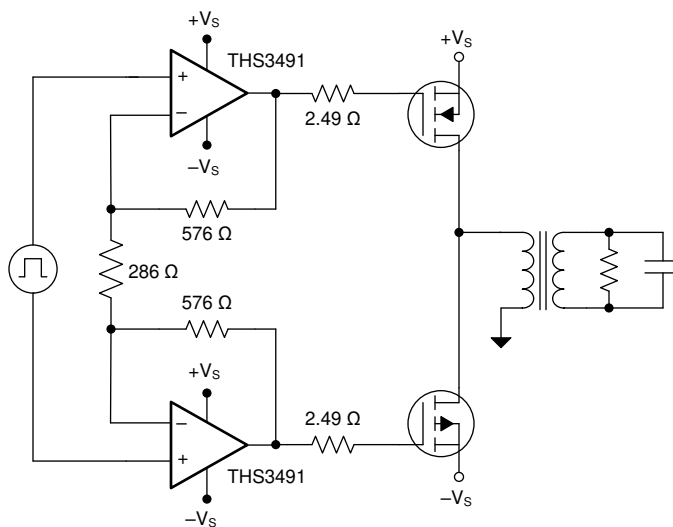


Figure 10-3. Power FET Drive Circuit

10.1.2 Video Distribution

The wide bandwidth, high slew rate, and high output drive current of the THS3491 meets the demands for video distribution by delivering video signals down multiple cables. For high signal quality with minimal degradation of performance, use a 0.1-dB gain flatness that is at least seven times the pass-band frequency to minimize group delay variations from the amplifier. A high slew rate minimizes distortion of the video signal and supports component video and RGB video signals that require fast transition and settling times for high signal quality.

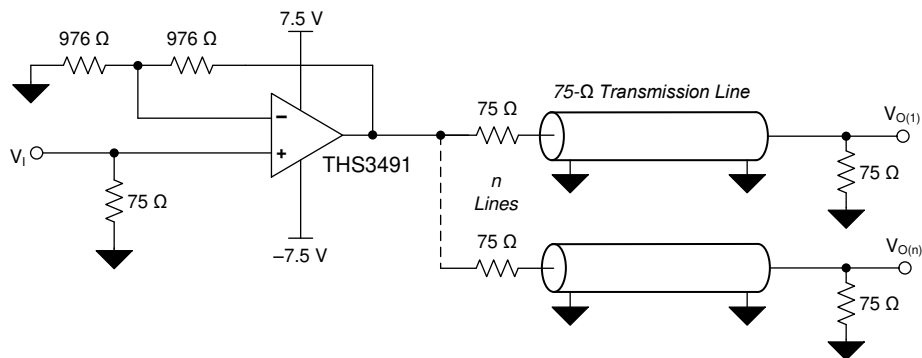
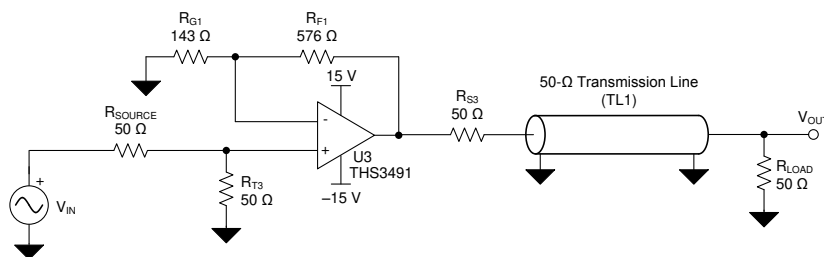


Figure 10-4. Video Distribution Amplifier Application

10.2 Typical Application

The fundamental concept of load sharing is to drive a load using two or more of the same operational amplifier. Each amplifier is driven by the same source. [Figure 10-5](#) shows two THS3491 amplifiers sharing the same load. This concept effectively reduces the current load of each amplifier by $1/N$, where N is the number of amplifiers.

a) Single THS3491 Amplifier Driving a Transmission Line



b) Two THS3491 Amplifiers Driving a Transmission Line

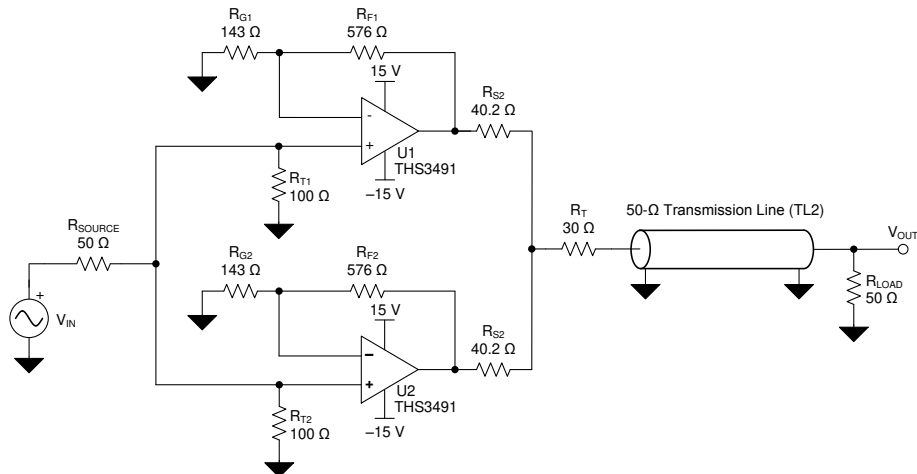


Figure 10-5. Load-Sharing Driver Application

10.2.1 Design Requirements

Use two THS3491 amplifiers in a parallel load-sharing circuit to improve distortion performance.

Table 10-1. Design Parameters

DESIGN PARAMETER	VALUE
V_O (At amplifier output)	20 V _{PP}
R_{LOAD}	100 Ω
Gain flatness at 100 MHz	Less than 0.5 dB

10.2.2 Detailed Design Procedure

In addition to providing higher output current drive to the load, the load-sharing configuration provides improved distortion performance. In many cases, an operational amplifier shows greater distortion performance as the load current decreases (that is, for higher resistive loads) until the feedback resistor dominates the current load. In a load-sharing configuration of N amplifiers in parallel, the equivalent current load that each amplifier drives is $1/N$ times the total load current. For example, in a two amplifier load-sharing configuration with matching resistance (see [Figure 10-5](#)) driving a resistive load (R_{LOAD}), the total series resistance (R_{TOT_SERIES}) at the output of the amplifiers is $2 \times R_{LOAD}$ and each amplifier drives $2 \times R_{LOAD}$. The total series resistance in the two-amplifier configuration shown in [Figure 10-5](#) is the parallel combination of R_{S2} resistors in series with R_T resistor ($R_{TOT_SERIES} = R_{S2} \parallel R_{S2} + R_T$). Such configuration of resistors at the output allows for fault detection if the load is shorted to GND and can be used for filtering the signal going to the load.

[Figure 10-5](#) shows two circuits: one of a single THS3491 amplifier driving a double-terminated, 50- Ω cable and one of two THS3491 amplifiers in a load-sharing configuration. In the load-sharing configuration, the two 40.2- Ω series output resistors act in parallel and in conjunction with the 30- Ω terminating resistor provide 50- Ω back-matching to the 50- Ω cable.

[Figure 10-6](#) shows the normalized frequency response for the two-amplifier load-sharing configuration. The total load, R_{TOT_LOAD} , for the configuration is the sum of R_{TOT_SERIES} and R_{LOAD} which is 100 Ω for the two-amplifier configuration in [Figure 10-5](#). [Figure 10-7](#) shows the distortion performance of the two-amplifier configuration.

Benefit of the multiple amplifier's in load-sharing configuration becomes even more evident when the total load increases. [Figure 10-8](#) and [Figure 10-9](#) show the HD2 and HD3 performance, respectively, in two, three, and four amplifier configurations when the $R_{TOT_LOAD} = 20 \Omega$. HD2 improves by almost 13 dB and 24 dB, respectively in the three and four amplifier configuration from the two-amplifier configuration, and HD3 shows an improvement of almost 15 and 19 dB in the three and four amplifier configurations, respectively.

10.2.3 Application Curves

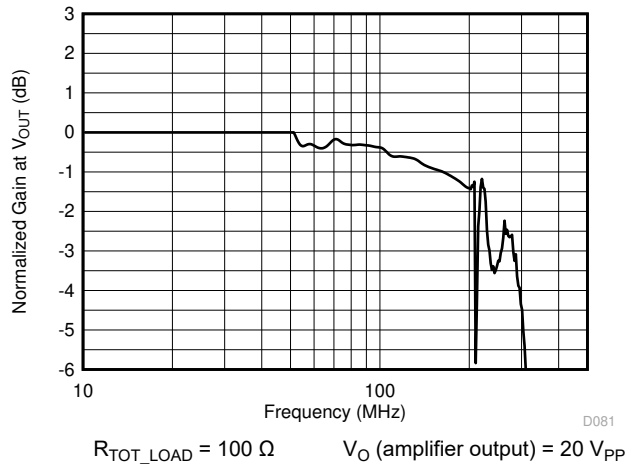


Figure 10-6. Frequency Response Of Two-Amplifier Configuration in Figure 10-5 (Gain = 5 V/V, Measured At V_{OUT})

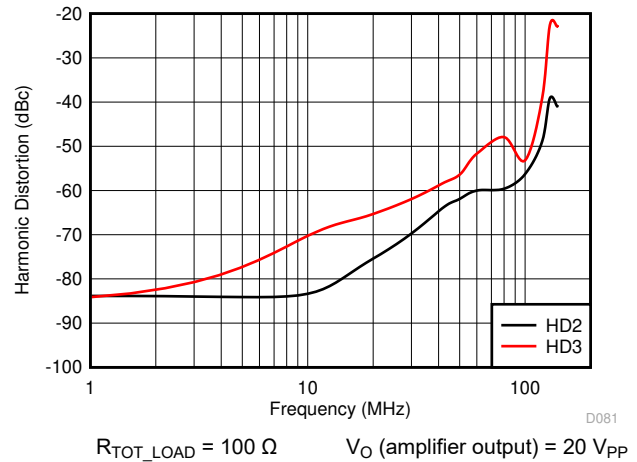


Figure 10-7. Distortion Of Two-Amplifier Configuration in Figure 10-5 (Gain = 5 V/V, Measured At V_{OUT})

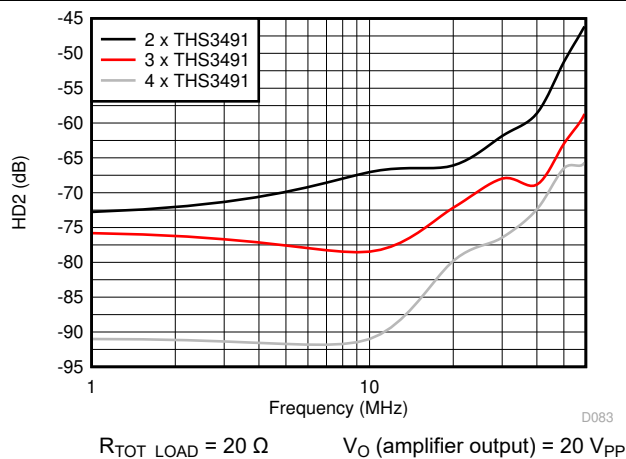


Figure 10-8. HD2 For Amplifier Load-Sharing Configuration (Gain = 5 V/V)

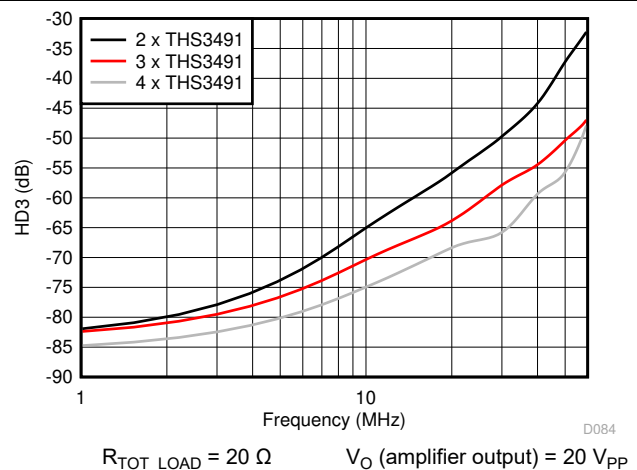


Figure 10-9. HD3 For Amplifier Load-Sharing Configuration (Gain = 5 V/V)

10.3 Power Supply Recommendations

The THS3491 operates from a single supply or with dual supplies if the input common-mode voltage range (CMIR) has the required headroom (4.3 V) to either supply rail. Supplies must be decoupled with low inductance (often ceramic) capacitors to ground less than 0.5 inches from the device pins. TI recommends using ground planes, and as in most high-speed devices, removing ground planes close to device sensitive pins such as input pins is advisable. An optional supply decoupling capacitor across the two power supplies (for split-supply operation) improves second harmonic distortion performance.

10.4 Layout

10.4.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the THS3491 requires careful attention to board layout parasitic and external component types.

Recommendations that optimize performance include:

- Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and input pins can cause instability. To reduce unwanted capacitance, a window around the signal I/O pins must be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes must be unbroken elsewhere on the board.
- Minimize the distance (< 0.25 of an inch [6.35 mm]) from the power supply pins to high-frequency 0.1- μ F and 100-pF decoupling capacitors. At the device pins, the ground and power plane layout must not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power supply connections must always be decoupled with these capacitors. Use larger tantalum decoupling capacitors (with a value of 6.8 μ F or more) that are effective at lower frequencies on the main supply pins. These can be placed further from the device and can be shared among several devices in the same area of the printed circuit board (PCB).
- Careful selection and placement of external components preserve the high-frequency performance of the THS3491. Resistors must be a low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Keep leads and PCB trace length as short as possible. Never use wire-bound type resistors in a high-frequency application. Because the output pin and inverting input pins are the most sensitive to parasitic capacitance, always position the feedback and series output resistors, if any, as close to the inverting input pins and output pins as possible, respectively. Place other network components such as input termination resistors close to the gain setting resistors. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values create significant time **constants** constraints? that can degrade performance. Good axial metal film or surface-mount resistors feature approximately 0.2 pF capacitance in shunt with the resistor. For resistor values greater than 2 k Ω , this parasitic capacitance adds a pole or a zero that can effect circuit operation. Keep resistor values as low as possible and consistent with load-driving considerations.
- Make connections to other wideband devices on the board with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Use relatively wide traces of 0.05 inch to 0.1 inch (1.3 mm to 2.54 mm), preferably with open ground and power planes around the traces. Estimate the total capacitive load and determine if isolation resistors on the outputs are required. Low parasitic capacitive loads (less than 4 pF) may not require series resistance because the THS3491 is nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without a series resistance are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required and the 6-dB signal loss intrinsic to a twice-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques).
- A 50- Ω environment is not required onboard, and a higher impedance environment improves distortion as shown in the distortion versus load plots; see [Figure 8-7](#) and [Figure 8-8](#). With a characteristic board trace impedance based on board material and trace dimensions, a matching series resistor into the trace from the output of the THS3491 is used. A terminating shunt resistor at the input of the destination device is also used. The terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device. This total effective impedance must be set to match the trace impedance. If the 6-dB attenuation of a twice-terminated transmission line is unacceptable, a long trace can be series terminated at the source end only. Treat the trace as a capacitive load in this case. This termination does not preserve signal integrity as well as a twice-terminated line. If the input impedance of the destination device is low, there is some signal attenuation because of the voltage divider formed by the series output into the terminating impedance.
- Do not socket a high-speed device like the THS3491. The socket introduces additional lead lengths and pin-to-pin capacitance, which can create a troublesome parasitic network. This can make it achieving a smooth, stable frequency response impossible. Obtain better results by soldering the THS3491 devices directly onto the board.

10.4.1.1 PowerPAD™ Integrated Circuit Package Design Considerations (DDA Package Only)

The THS3491 is available in a thermally-enhanced PowerPAD integrated circuit package. These packages are constructed using a downset leadframe on which the die is mounted, as shown in the (a) and (b) sections of Figure 10-10. This arrangement results in the lead frame that is exposed as a thermal pad on the underside of the package, as shown in Figure 10-10(c). Because this thermal pad directly contacts the die, achieve efficient thermal performance by providing a good thermal path away from the thermal pad. Devices such as the THS3491 have no electrical connection between the PowerPAD and the die.

The PowerPAD integrated circuit package allows for assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are soldered), the thermal pad can be soldered to a copper area underneath the package. By using thermal paths within this copper area, heat is conducted away from the package into a ground plane or other heat-dissipating device.

The PowerPAD integrated circuit package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.

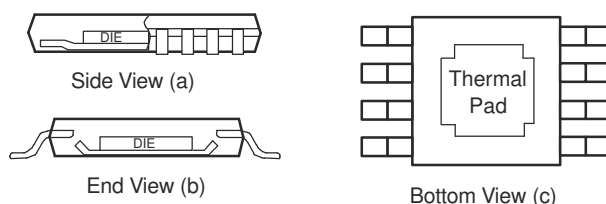


Figure 10-10. Views of Thermally Enhanced Package

Although there are many ways to properly heat sink the PowerPAD integrated circuit package, see Section 10.4.1.1.1 for the recommended approach.

10.4.1.1.1 PowerPAD™ Integrated Circuit Package Layout Considerations

The DDA package top-side etch and via pattern is shown in Figure 10-11.

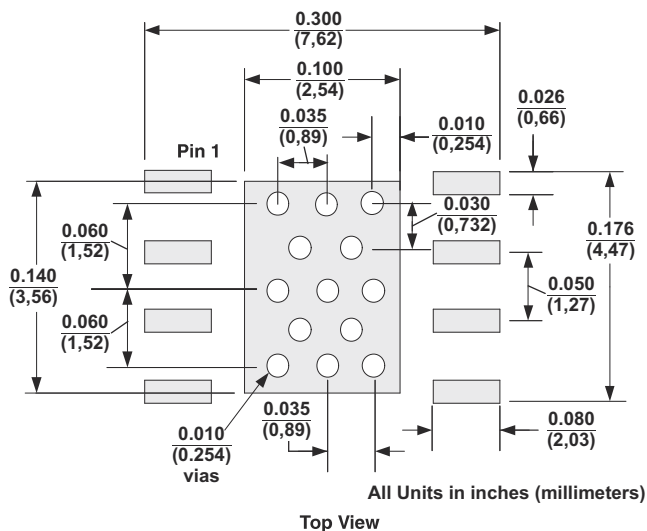


Figure 10-11. DDA PowerPAD™ Integrated Circuit Package PCB Etch and Via Pattern

1. Use etch for the leads and the thermal pad.
2. Place 13 vias in the thermal pad area. These vias must be 0.01 inch (0.254 mm) in diameter. Keep the vias small so that solder wicking through the vias is not a problem during reflow.

3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area, and help dissipate the heat generated by the THS3491 device. These additional vias may be larger than the 0.01-inch (0.254 mm) diameter vias directly under the thermal pad because they are not in the area that requires soldering. As a result, wicking is not a problem.
4. Connect all vias to the internal ground plane. The PowerPAD integrated circuit package is electrically isolated from the silicon and all leads. Connecting the PowerPAD integrated circuit package to any potential voltage such as $-V_S$ is acceptable because there is no electrical connection to the silicon.
5. When connecting these vias to the ground plane, do not use the typical web or spoke through connection methodology. Web and spoke connections have a high thermal resistance that slows the heat transfer during soldering. Avoiding these connection methods makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the vias under the THS3491 PowerPAD integrated circuit package must connect to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask must leave the pins of the package and the thermal pad area with the 13 vias exposed.
7. Apply solder paste to the exposed thermal pad area and all of the device pins.
8. With these preparatory steps in place, the device is placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a device that is properly installed.

10.4.1.1.2 Power Dissipation and Thermal Considerations

The THS3491 includes automatic thermal shutoff protection. This protection circuitry shuts down the amplifier if the junction temperature exceeds approximately 160°C. When the junction temperature decreases to approximately 145°C, the amplifier turns on again. However, for maximum performance and reliability, make sure that the design does not exceed a junction temperature of 125°C. Between 125°C and 150°C, damage does not occur, but the performance of the amplifier begins to degrade and long-term reliability suffers. The package and the PCB dictate the thermal characteristics of the device. Maximum power dissipation for a particular package is calculated using the following formula.

$$P_{Dmax} = \frac{T_{max} - T_A}{\theta_{JA}} \quad (1)$$

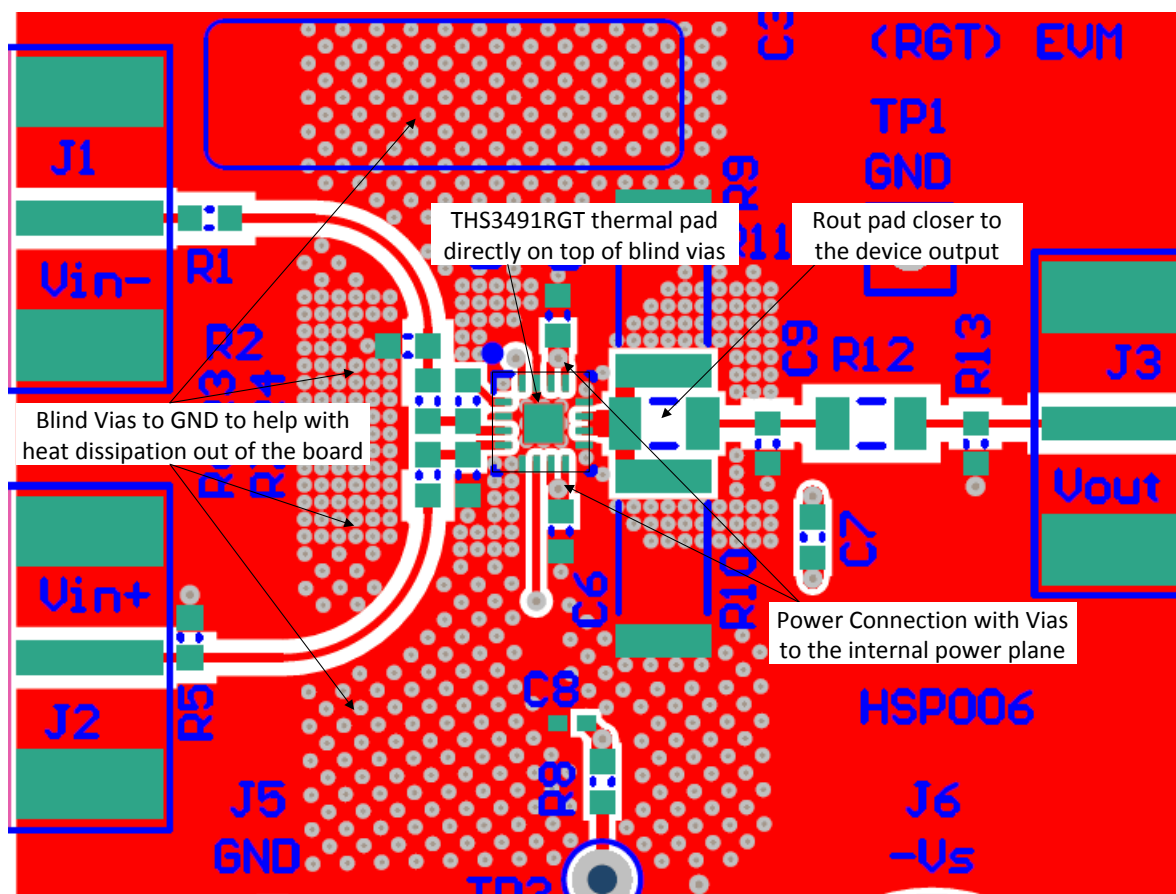
where

- P_{Dmax} is the maximum power dissipation in the amplifier (W).
- T_{max} is the absolute maximum junction temperature (°C).
- T_A is the ambient temperature (°C).
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W).
- θ_{CA} is the thermal coefficient from the case to ambient air (°C/W).

The thermal coefficient for the PowerPAD integrated circuit packages are substantially improved over the traditional SOIC package. The data for the PowerPAD packages assume a board layout that follows the PowerPAD package layout guidelines referenced above and detailed in [PowerPAD™ Thermally Enhanced Package](#). Maximum power dissipation levels are shown in *Comparison of θ_{JA} for Various Packages*. If the PowerPAD integrated circuit package is not soldered to the PCB, the thermal impedance increases substantially and may cause serious heat and performance issues. Take care to always solder the PowerPAD integrated circuit package to the PCB for optimum performance.

When determining whether or not the device satisfies the maximum power dissipation requirement, make sure to consider not only quiescent power dissipation, but dynamic power dissipation. Often times, this dissipation is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation provides visibility into a possible problem.

10.4.2 Layout Example



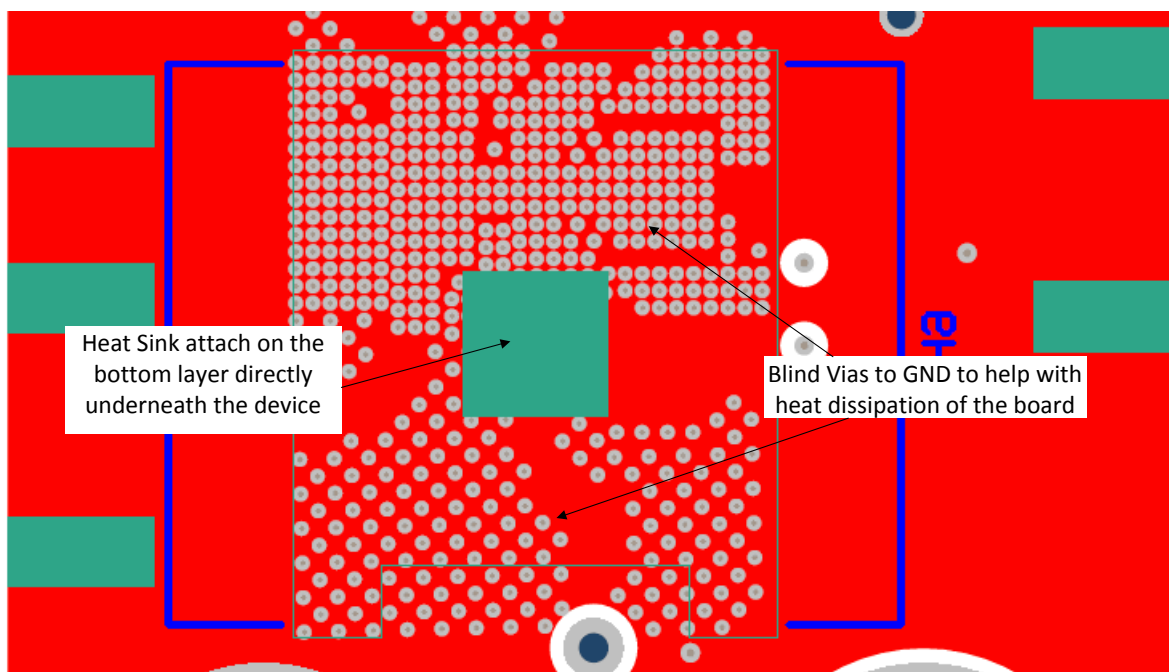


Figure 10-14. Heat Sink Attachment to Bottom Layer

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [PowerPAD™ Made Easy](#)
- Texas Instruments, [PowerPAD™ Thermally Enhanced Package](#)
- Texas Instruments, [Voltage Feedback vs Current Feedback Op Amps](#)
- Texas Instruments, [Current Feedback Amplifier Analysis and Compensation](#)
- Texas Instruments, [Current Feedback Amplifiers: Review, Stability Analysis, and Applications](#)
- Texas Instruments, [Effect of Parasitic Capacitance in Op Amp Circuits](#)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

11.4 Trademarks

PowerPAD™ is a trademark of Texas Instruments.

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS3491IDDAR	Active	Production	SO PowerPAD (DDA) 8	2500 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	HS3491
THS3491IDDAR.B	Active	Production	SO PowerPAD (DDA) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	HS3491
THS3491IDDAT	Active	Production	SO PowerPAD (DDA) 8	250 SMALL T&R	Yes	NIPDAU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	HS3491
THS3491IDDAT.B	Active	Production	SO PowerPAD (DDA) 8	250 SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	HS3491
THS3491IRGTR	Active	Production	VQFN (RGT) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS3491
THS3491IRGTR.B	Active	Production	VQFN (RGT) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS3491
THS3491IRGTRG4	Active	Production	VQFN (RGT) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS3491
THS3491IRGTRG4.B	Active	Production	VQFN (RGT) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS3491
THS3491IRGTT	Active	Production	VQFN (RGT) 16	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS3491
THS3491IRGTT.B	Active	Production	VQFN (RGT) 16	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS3491
THS3491YR	Active	Production	DIESALE (Y) 0	3000 LARGE T&R	Yes	Call TI	N/A for Pkg Type	-40 to 85	
THS3491YR.B	Active	Production	DIESALE (Y) 0	3000 LARGE T&R	Yes	Call TI	N/A for Pkg Type	-40 to 85	

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

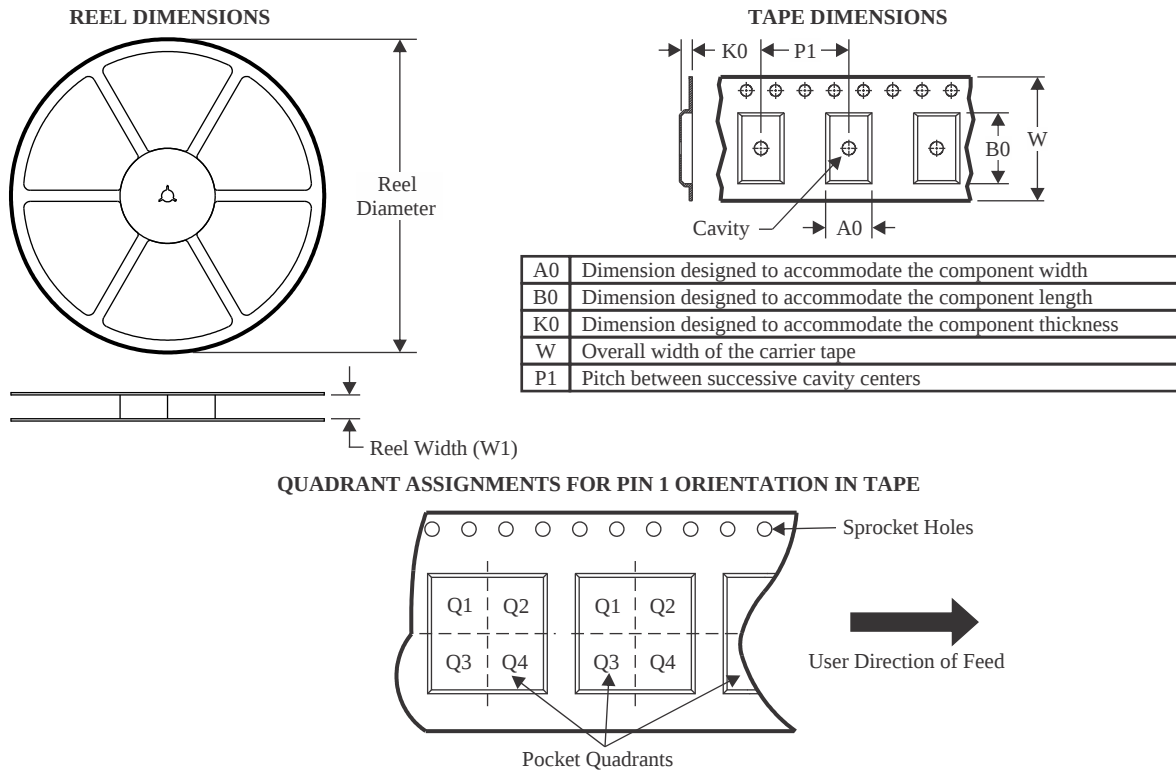
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

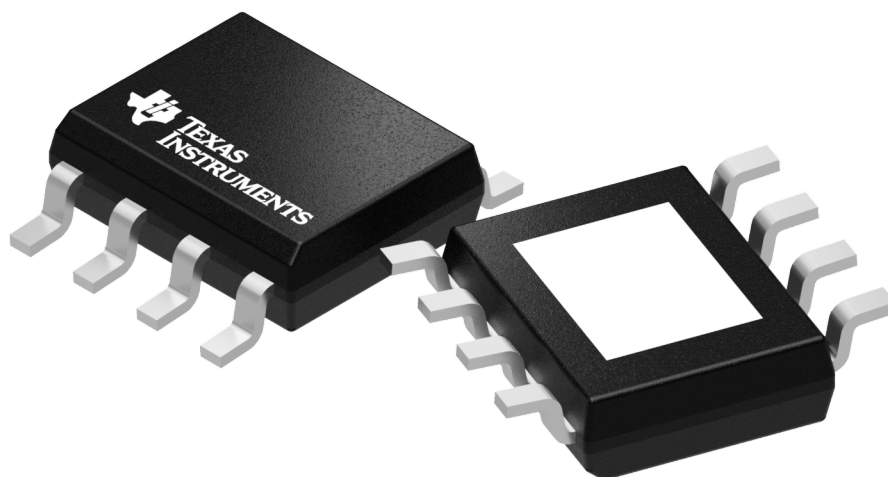
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS3491IDDAT	SO PowerPAD	DDA	8	250	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
THS3491IRGTR	VQFN	RGT	16	2500	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THS3491IRGTRG4	VQFN	RGT	16	2500	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THS3491IRGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

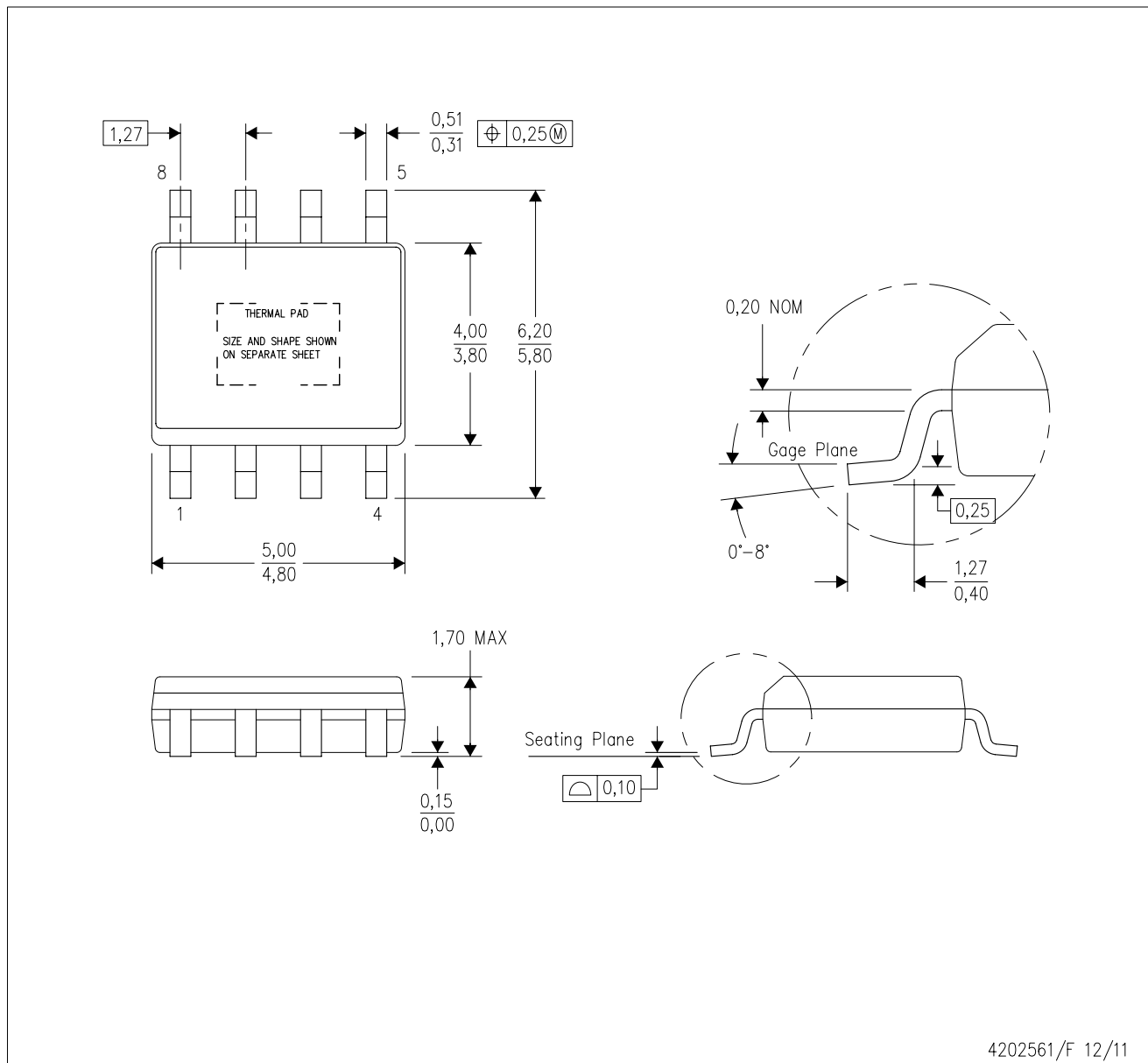
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS3491IDDAT	SO PowerPAD	DDA	8	250	366.0	364.0	50.0
THS3491IRGTR	VQFN	RGT	16	2500	346.0	346.0	33.0
THS3491IRGTRG4	VQFN	RGT	16	2500	346.0	346.0	33.0
THS3491IRGTT	VQFN	RGT	16	250	210.0	185.0	35.0



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - This package complies to JEDEC MS-012 variation BA

PowerPAD is a trademark of Texas Instruments.

DDA (R-PDSO-G8)

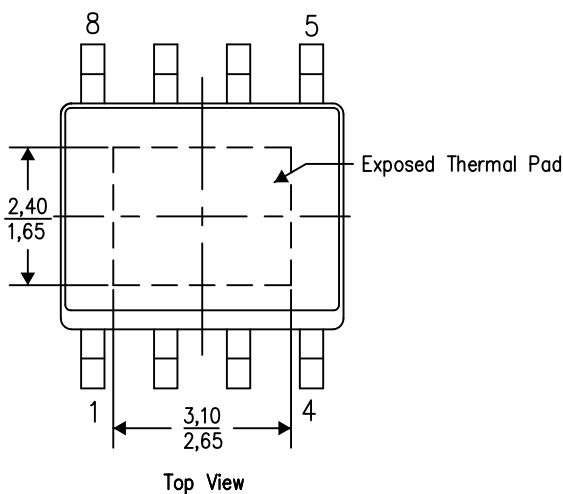
PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



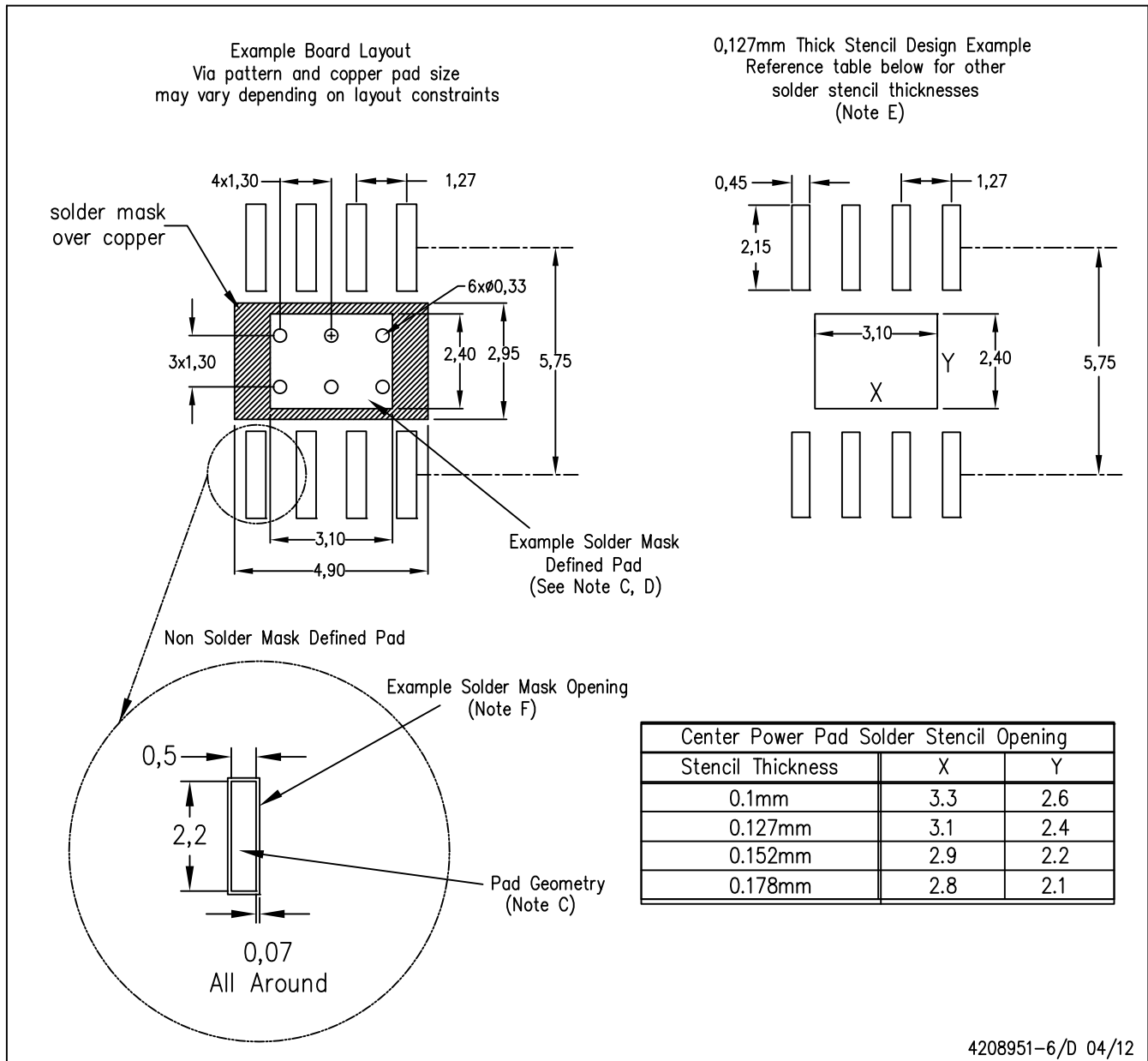
4206322-6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

PowerPAD™ SOIC - 1.7 mm max height

Technical drawing of a microelectronic package showing top, side, and detail views with dimensions and callouts.

Top View:

- Overall width: 6.2 TYP, 5.8
- Overall height: 5.0, 4.8, NOTE 3
- Pin 1 ID AREA (hatched)
- Pin 1 location: 1
- Pin 8 location: 8
- Pin 5 location: 5
- Pin 4 location: 4
- Pin 3 location: 3
- Pin 2 location: 2
- Pin 7 location: 7
- Pin 6 location: 6
- Pin 9 location: 9
- Pin 10 location: 10
- Pin 11 location: 11
- Pin 12 location: 12
- Pin 13 location: 13
- Pin 14 location: 14
- Pin 15 location: 15
- Pin 16 location: 16
- Pin 17 location: 17
- Pin 18 location: 18
- Pin 19 location: 19
- Pin 20 location: 20
- Pin 21 location: 21
- Pin 22 location: 22
- Pin 23 location: 23
- Pin 24 location: 24
- Pin 25 location: 25
- Pin 26 location: 26
- Pin 27 location: 27
- Pin 28 location: 28
- Pin 29 location: 29
- Pin 30 location: 30
- Pin 31 location: 31
- Pin 32 location: 32
- Pin 33 location: 33
- Pin 34 location: 34
- Pin 35 location: 35
- Pin 36 location: 36
- Pin 37 location: 37
- Pin 38 location: 38
- Pin 39 location: 39
- Pin 40 location: 40
- Pin 41 location: 41
- Pin 42 location: 42
- Pin 43 location: 43
- Pin 44 location: 44
- Pin 45 location: 45
- Pin 46 location: 46
- Pin 47 location: 47
- Pin 48 location: 48
- Pin 49 location: 49
- Pin 50 location: 50
- Pin 51 location: 51
- Pin 52 location: 52
- Pin 53 location: 53
- Pin 54 location: 54
- Pin 55 location: 55
- Pin 56 location: 56
- Pin 57 location: 57
- Pin 58 location: 58
- Pin 59 location: 59
- Pin 60 location: 60
- Pin 61 location: 61
- Pin 62 location: 62
- Pin 63 location: 63
- Pin 64 location: 64
- Pin 65 location: 65
- Pin 66 location: 66
- Pin 67 location: 67
- Pin 68 location: 68
- Pin 69 location: 69
- Pin 70 location: 70
- Pin 71 location: 71
- Pin 72 location: 72
- Pin 73 location: 73
- Pin 74 location: 74
- Pin 75 location: 75
- Pin 76 location: 76
- Pin 77 location: 77
- Pin 78 location: 78
- Pin 79 location: 79
- Pin 80 location: 80
- Pin 81 location: 81
- Pin 82 location: 82
- Pin 83 location: 83
- Pin 84 location: 84
- Pin 85 location: 85
- Pin 86 location: 86
- Pin 87 location: 87
- Pin 88 location: 88
- Pin 89 location: 89
- Pin 90 location: 90
- Pin 91 location: 91
- Pin 92 location: 92
- Pin 93 location: 93
- Pin 94 location: 94
- Pin 95 location: 95
- Pin 96 location: 96
- Pin 97 location: 97
- Pin 98 location: 98
- Pin 99 location: 99
- Pin 100 location: 100
- Pin 101 location: 101
- Pin 102 location: 102
- Pin 103 location: 103
- Pin 104 location: 104
- Pin 105 location: 105
- Pin 106 location: 106
- Pin 107 location: 107
- Pin 108 location: 108
- Pin 109 location: 109
- Pin 110 location: 110
- Pin 111 location: 111
- Pin 112 location: 112
- Pin 113 location: 113
- Pin 114 location: 114
- Pin 115 location: 115
- Pin 116 location: 116
- Pin 117 location: 117
- Pin 118 location: 118
- Pin 119 location: 119
- Pin 120 location: 120
- Pin 121 location: 121
- Pin 122 location: 122
- Pin 123 location: 123
- Pin 124 location: 124
- Pin 125 location: 125
- Pin 126 location: 126
- Pin 127 location: 127
- Pin 128 location: 128
- Pin 129 location: 129
- Pin 130 location: 130
- Pin 131 location: 131
- Pin 132 location: 132
- Pin 133 location: 133
- Pin 134 location: 134
- Pin 135 location: 135
- Pin 136 location: 136
- Pin 137 location: 137
- Pin 138 location: 138
- Pin 139 location: 139
- Pin 140 location: 140
- Pin 141 location: 141
- Pin 142 location: 142
- Pin 143 location: 143
- Pin 144 location: 144
- Pin 145 location: 145
- Pin 146 location: 146
- Pin 147 location: 147
- Pin 148 location: 148
- Pin 149 location: 149
- Pin 150 location: 150
- Pin 151 location: 151
- Pin 152 location: 152
- Pin 153 location: 153
- Pin 154 location: 154
- Pin 155 location: 155
- Pin 156 location: 156
- Pin 157 location: 157
- Pin 158 location: 158
- Pin 159 location: 159
- Pin 160 location: 160
- Pin 161 location: 161
- Pin 162 location: 162
- Pin 163 location: 163
- Pin 164 location: 164
- Pin 165 location: 165
- Pin 166 location: 166
- Pin 167 location: 167
- Pin 168 location: 168
- Pin 169 location: 169
- Pin 170 location: 170
- Pin 171 location: 171
- Pin 172 location: 172
- Pin 173 location: 173
- Pin 174 location: 174
- Pin 175 location: 175
- Pin 176 location: 176
- Pin 177 location: 177
- Pin 178 location: 178
- Pin 179 location: 179
- Pin 180 location: 180
- Pin 181 location: 181
- Pin 182 location: 182
- Pin 183 location: 183
- Pin 184 location: 184
- Pin 185 location: 185
- Pin 186 location: 186
- Pin 187 location: 187
- Pin 188 location: 188
- Pin 189 location: 189
- Pin 190 location: 190
- Pin 191 location: 191
- Pin 192 location: 192
- Pin 193 location: 193
- Pin 194 location: 194
- Pin 195 location: 195
- Pin 196 location: 196
- Pin 197 location: 197
- Pin 198 location: 198
- Pin 199 location: 199
- Pin 200 location: 200
- Pin 201 location: 201
- Pin 202 location: 202
- Pin 203 location: 203
- Pin 204 location: 204
- Pin 205 location: 205
- Pin 206 location: 206
- Pin 207 location: 207
- Pin 208 location: 208
- Pin 209 location: 209
- Pin 210 location: 210
- Pin 211 location: 211
- Pin 212 location: 212
- Pin 213 location: 213
- Pin 214 location: 214
- Pin 215 location: 215
- Pin 216 location: 216
- Pin 217 location: 217
- Pin 218 location: 218
- Pin 219 location: 219
- Pin 220 location: 220
- Pin 221 location: 221
- Pin 222 location: 222
- Pin 223 location: 223
- Pin 224 location: 224
- Pin 225 location: 225
- Pin 226 location: 226
- Pin 227 location: 227
- Pin 228 location: 228
- Pin 229 location: 229
- Pin 230 location: 230
- Pin 231 location: 231
- Pin 232 location: 232
- Pin 233 location: 233
- Pin 234 location: 234
- Pin 235 location: 235
- Pin 236 location: 236
- Pin 237 location: 237
- Pin 238 location: 238
- Pin 239 location: 239
- Pin 240 location: 240
- Pin 241 location: 241
- Pin 242 location: 242
- Pin 243 location: 243
- Pin 244 location: 244
- Pin 245 location: 245
- Pin 246 location: 246
- Pin 2

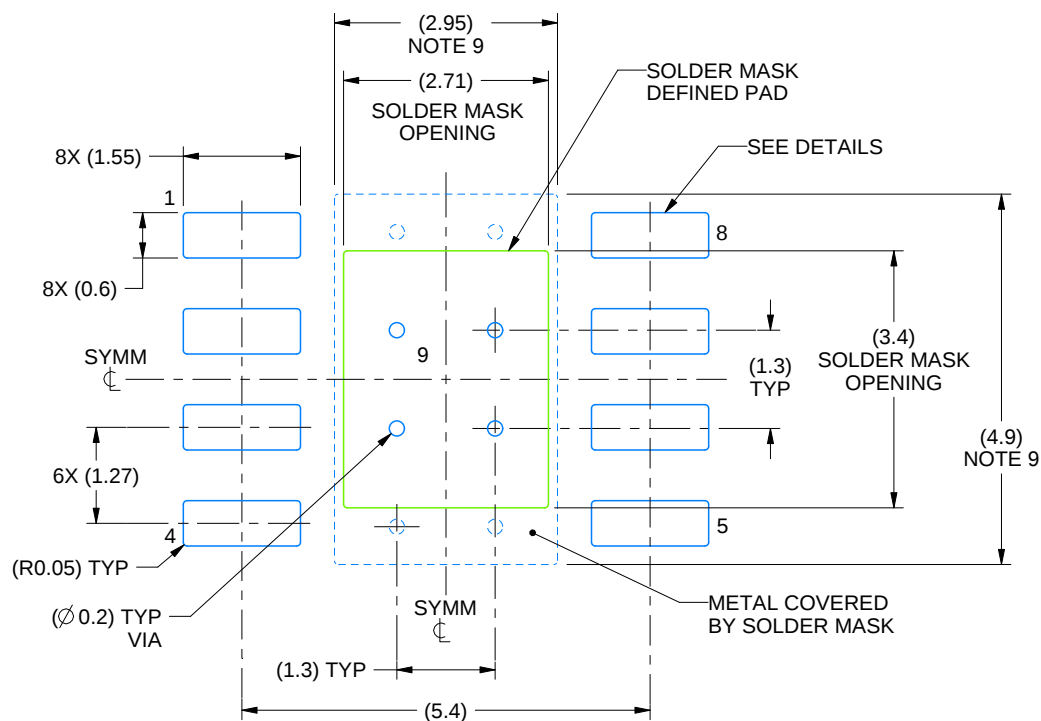
PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.

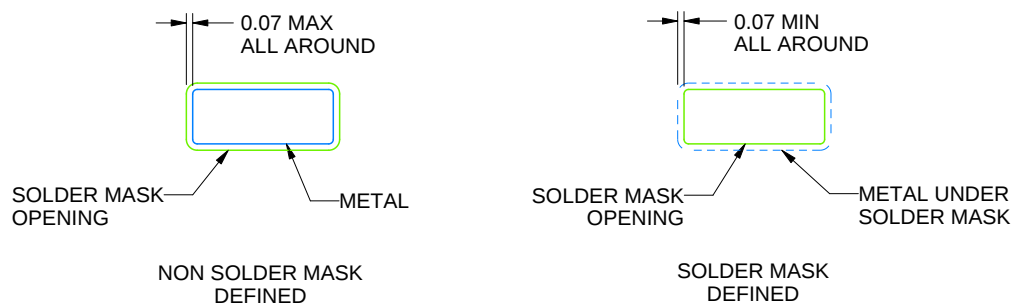
DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/B 09/2025

NOTES: (continued)

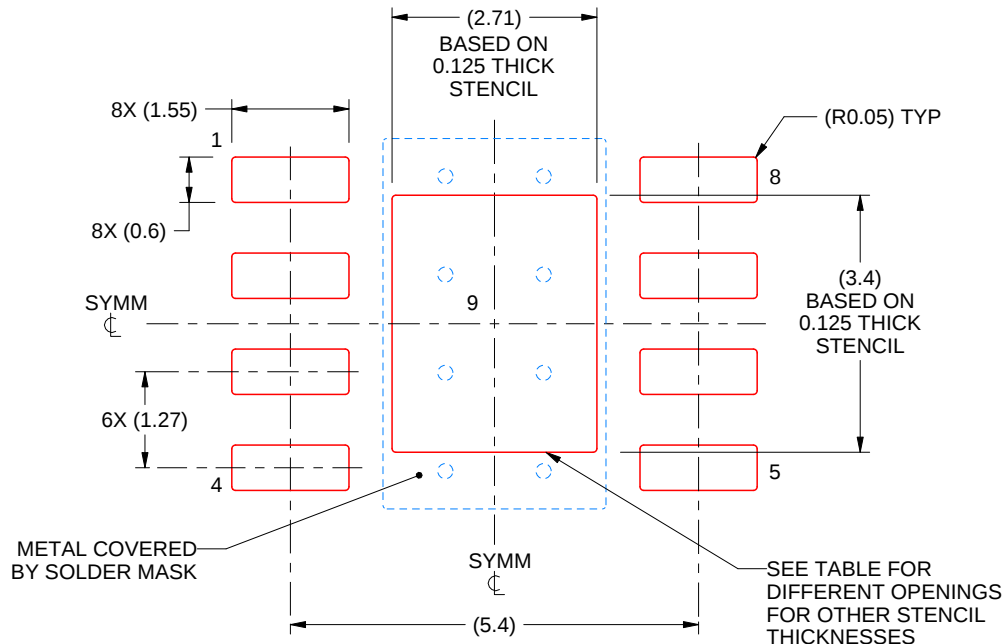
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/B 09/2025

NOTES: (continued)

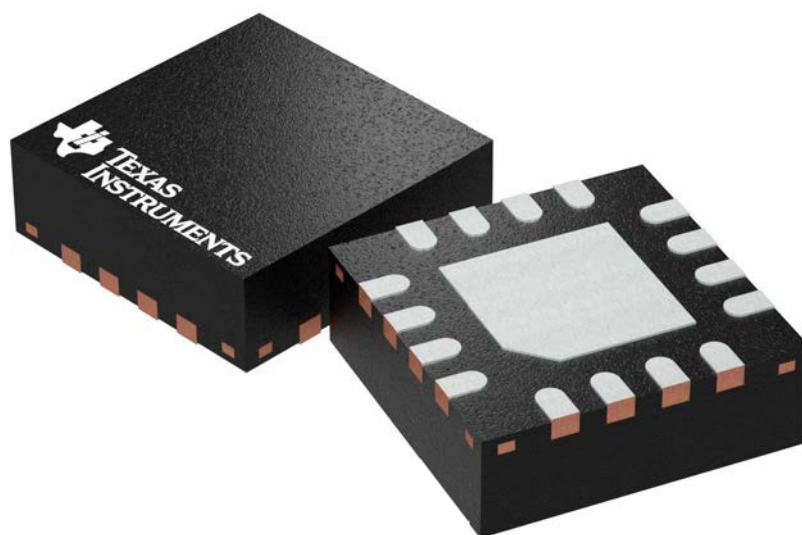
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

RGT 16

GENERIC PACKAGE VIEW

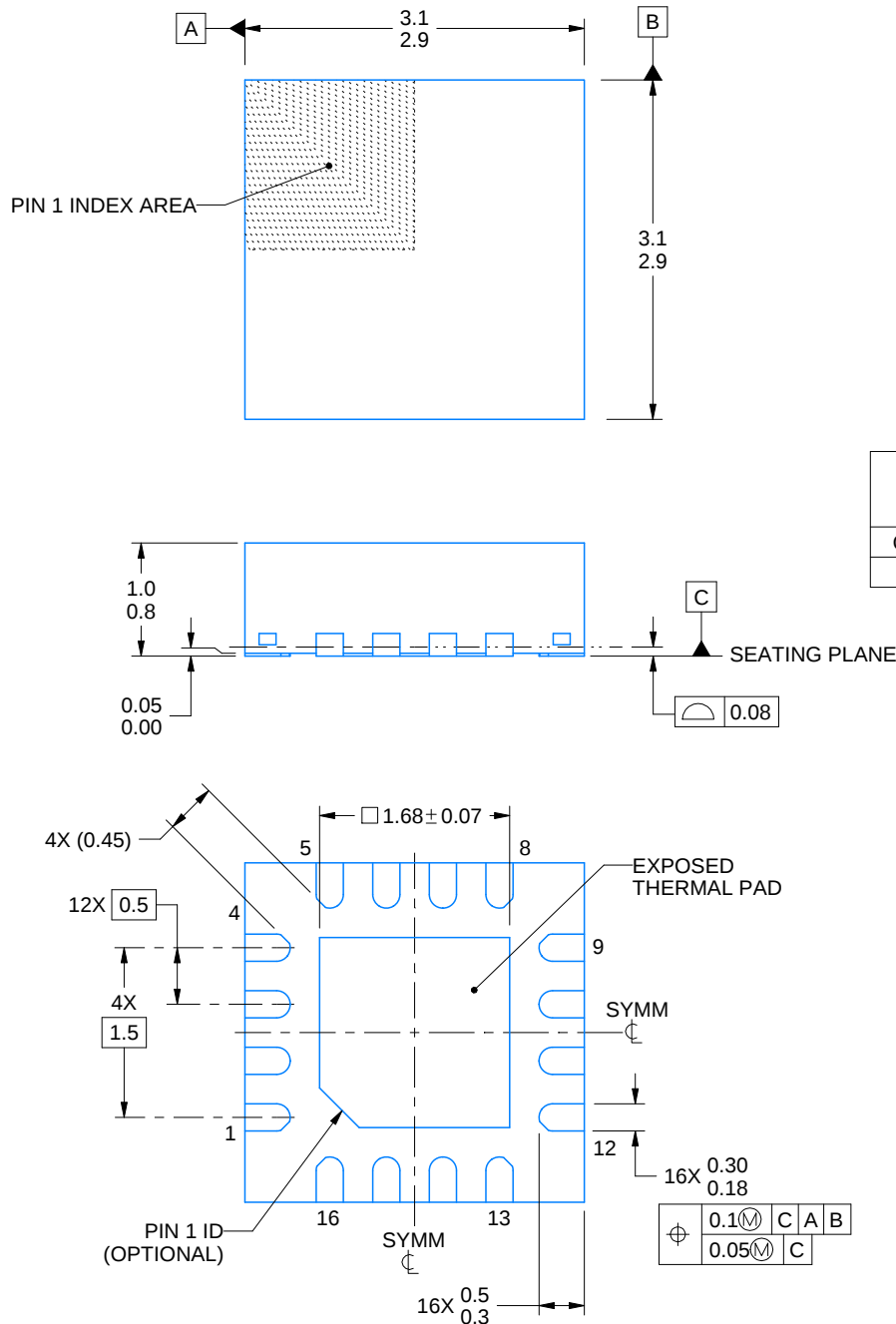
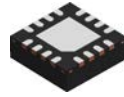
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203495/1



4222419/E 07/2025

NOTES:

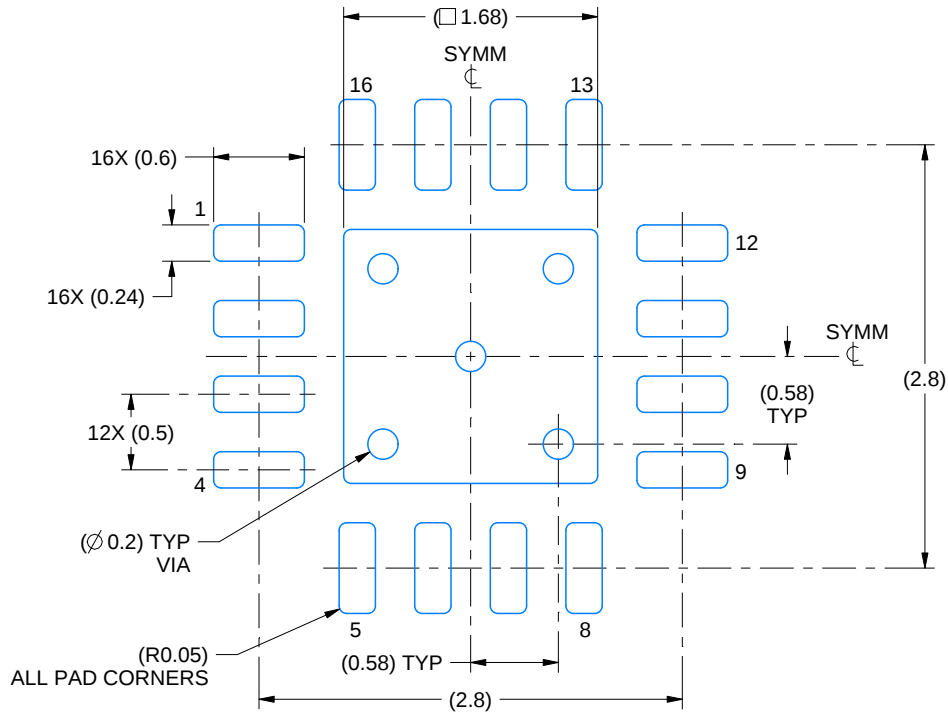
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

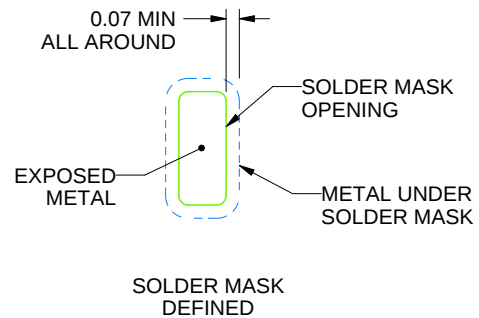
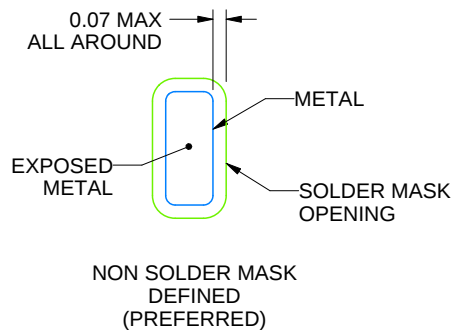
RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4222419/E 07/2025

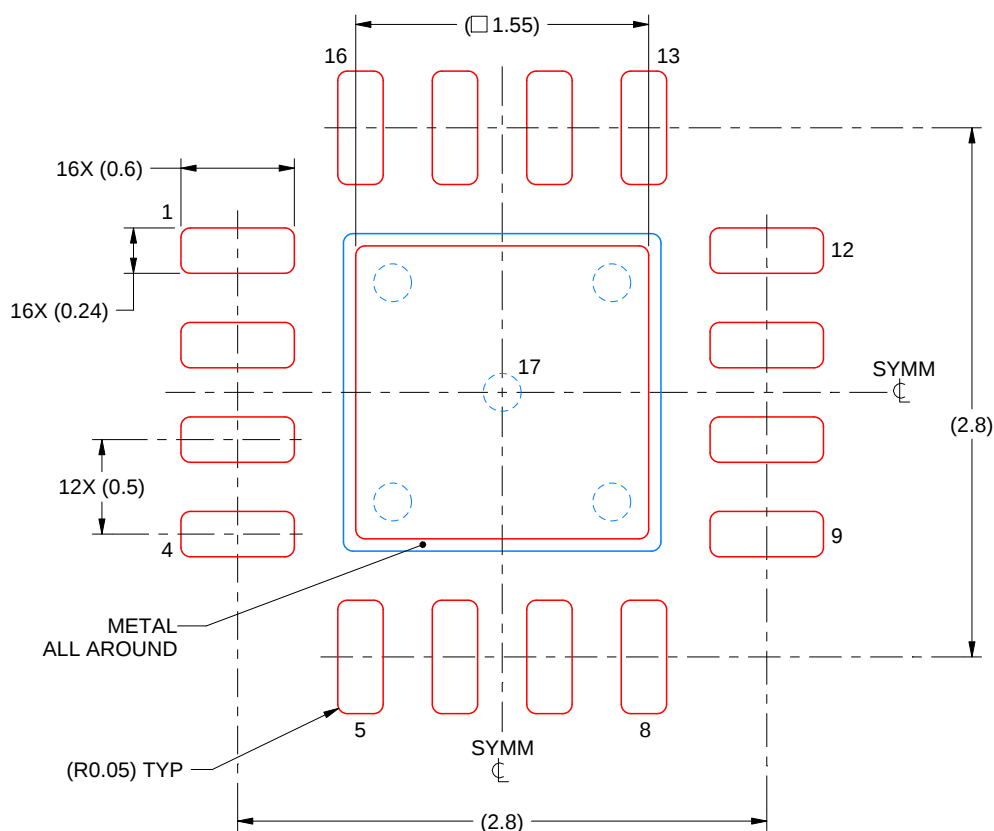
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/E 07/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025