

# FAN7528

## Dual-Output, Critical Conduction Mode PFC Controller

### Features

- Low Total Harmonic Distortion (THD)
- Dual Output Voltage Control
- Precise Adjustable Output Over-Voltage Protection
- Open-Feedback Protection and Disable Function
- Zero Current Detector
- 160μs Internal Start-up Timer
- MOSFET Over-Current Protection
- Under-Voltage Lockout with 3.5V Hysteresis
- Low Start-up (40μA) and Operating Current (1.5mA)
- Totem-Pole Output with High State Clamp
- ±400mA Peak Gate Drive Current
- 8-Pin DIP or 8-Pin SOP

### Applications

- Adapter

### Related Application Notes

- **AN-6012:** Design of Power Factor Correction Circuit Using FAN7528

### Description

The FAN7528 is an active power factor correction (PFC) controller for boost PFC applications that operates in critical conduction mode (CRM). It uses voltage mode PWM that compares an internal ramp signal with the error amplifier output to generate MOSFET turn-off signal. Because the voltage mode CRM PFC controller does not need the rectified AC line voltage information, it can save the power loss of the input voltage sensing network necessary for the current mode CRM PFC controller.

The FAN7528 provides the dual-output voltage control function without the AC line voltage sensing for adapter applications. It changes the PFC output voltage according to the AC line voltage.

It provides protection functions such as over-voltage protection, open-feedback protection, over-current protection, and under-voltage lockout protection. The FAN7528 can be disabled if the INV pin voltage is lower than 0.45V and the operating current decreases to 65μA. Using a new variable on-time control method, THD is lower than the conventional CRM boost PFC ICs.

### Ordering Information

| Part Number | Operating Temp. Range | Pb-Free | Package | Packing Method | Marking Code |
|-------------|-----------------------|---------|---------|----------------|--------------|
| FAN7528N    | -40°C to +125°C       | Yes     | 8-DIP   | Rail           | FAN7528      |
| FAN7528M    | -40°C to +125°C       | Yes     | 8-SOP   | Rail           | FAN7528      |
| FAN7528MX   | -40°C to +125°C       | Yes     | 8-SOP   | Tape & Reel    | FAN7528      |

## Typical Application Diagrams

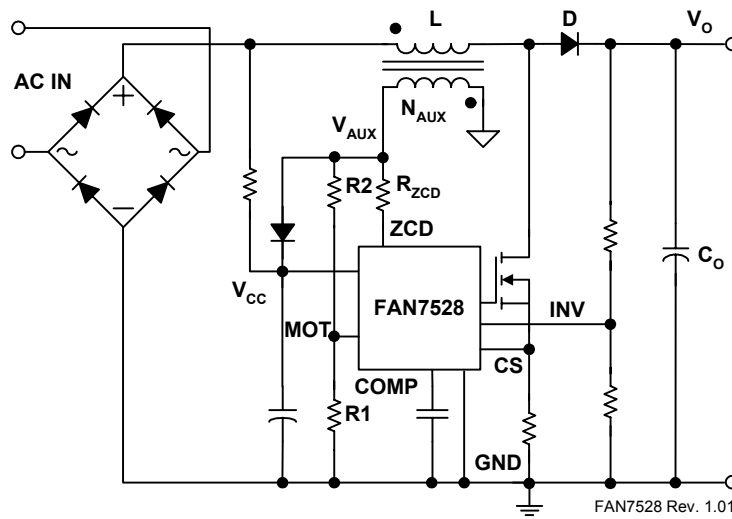


Figure 1. Typical Boost PFC Application

## Internal Block Diagram

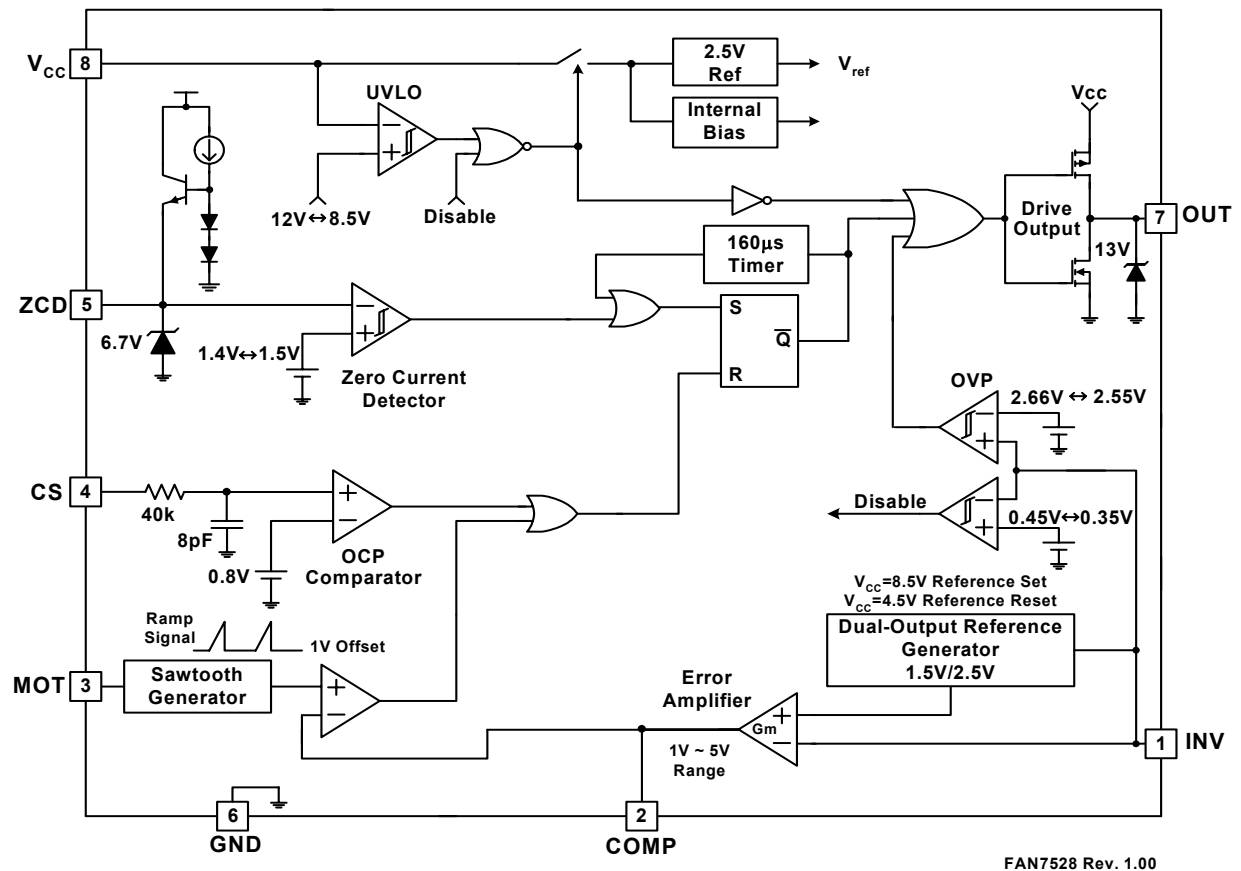


Figure 2. Functional Block Diagram of FAN7528

## Pin Assignments

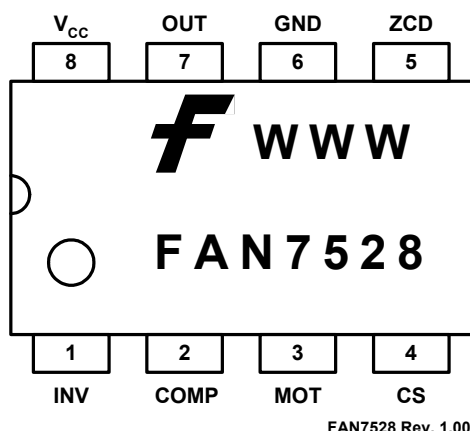


Figure 3. Pin Configuration (Top View)

## Pin Definitions

| Pin # | Name            | Description                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | INV             | This pin is the inverting input of the error amplifier. The output voltage of the boost PFC converter should be resistively divided to 2.5V at the high line condition and connected to this pin. If this pin voltage is controlled to be lower than 0.45V, the device is disabled.                                                                                                                                           |
| 2     | COMP            | This pin is the output of the transconductance error amplifier. Some components for the output voltage compensation should be connected between this pin and GND.                                                                                                                                                                                                                                                             |
| 3     | MOT             | This pin is used to set the slope of the internal ramp. The voltage of this pin is maintained to be 1V. If a resistor is connected between this pin and GND, current flows out of the pin and the slope of the internal ramp is proportional to this current.                                                                                                                                                                 |
| 4     | CS              | This pin is the input of the over-current protection comparator. The MOSFET current is sensed using a sensing resistor and the resulting voltage is applied to this pin. An internal RC filter is included to filter switching noise. This pin is sensitive to the negative voltage below -0.3V. For proper operation, the stray inductance in the sensing path and the inductance of the sensing resistor must be minimized. |
| 5     | ZCD             | This pin is the input of the zero current detection block. If the voltage of this pin goes higher than 1.5V, then lower than 1.4V, the MOSFET is turned on.                                                                                                                                                                                                                                                                   |
| 6     | GND             | This pin is used for the ground potential of all the pins. For proper operation, the signal ground and the power ground should be separated.                                                                                                                                                                                                                                                                                  |
| 7     | OUT             | This pin is the gate drive output. The peak sourcing and sinking current level is 400mA. For proper operation, the stray inductance in the gate driving path must be minimized.                                                                                                                                                                                                                                               |
| 8     | V <sub>CC</sub> | This pin is the IC supply pin. IC current and MOSFET drive current are supplied using this pin.                                                                                                                                                                                                                                                                                                                               |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.  $T_A = 25^\circ\text{C}$  unless otherwise specified.

| Symbol           | Parameter                                                     | Value      | Unit             |
|------------------|---------------------------------------------------------------|------------|------------------|
| $V_{CC}$         | Supply Voltage                                                | 23         | V                |
| $I_{OH}, I_{OL}$ | Peak Drive Output Current                                     | $\pm 400$  | mA               |
| $I_{clamp}$      | Driver Output Clamping Diodes $V_O > V_{CC}$ or $V_O < -0.3V$ | $\pm 10$   | mA               |
| $I_{det}$        | Detector Clamping Diodes                                      | $\pm 10$   | mA               |
| $V_{IN}$         | Error Amp, MOT, CS Input Voltages                             | -0.3 to 6  | V                |
| $T_J$            | Operating Junction Temperature                                | 150        | $^\circ\text{C}$ |
| $T_A$            | Operating Temperature Range                                   | -40 to 125 | $^\circ\text{C}$ |
| $T_{STG}$        | Storage Temperature Range                                     | -65 to 150 | $^\circ\text{C}$ |
| ESD              | Human Body Model                                              | 2.0        | kV               |
|                  | Machine Model                                                 | 300        | V                |

## Thermal Impedance

| Symbol        | Parameter                               |       | Value | Unit               |
|---------------|-----------------------------------------|-------|-------|--------------------|
| $\theta_{JA}$ | Thermal Resistance, Junction-to-Ambient | 8-DIP | 110   | $^\circ\text{C/W}$ |
|               |                                         | 8-SOP | 150   | $^\circ\text{C/W}$ |

### Note:

- Regarding the test environment and PCB type, please refer to JESD51-2 and JESD51-10.

## Electrical Characteristics

$V_{CC} = 14V$ ,  $T_A = -40^{\circ}C \sim 125^{\circ}C$ , unless otherwise specified.

| Symbol                               | Parameter                                     | Condition                               | Min.  | Typ.  | Max.  | Unit      |
|--------------------------------------|-----------------------------------------------|-----------------------------------------|-------|-------|-------|-----------|
| <b>Under-Voltage Lockout Section</b> |                                               |                                         |       |       |       |           |
| $V_{TH(start)}$                      | Start Threshold Voltage                       | $V_{CC}$ increasing                     | 11    | 12    | 13    | V         |
| $V_{TH(stop)}$                       | Stop Threshold Voltage                        | $V_{CC}$ decreasing                     | 8.0   | 8.5   | 9.0   | V         |
| $H_{Y(uvlo)}$                        | UVLO Hysteresis                               |                                         | 3.0   | 3.5   | 4.0   | V         |
| <b>Supply Current Section</b>        |                                               |                                         |       |       |       |           |
| $I_{ST}$                             | Start-up Supply Current                       | $V_{CC} = V_{TH(start)} - 0.2V$         |       | 40    | 70    | $\mu A$   |
| $I_{CC}$                             | Operating Supply Current                      | Output no switching                     |       | 1.5   | 3.0   | mA        |
| $I_{DCC}$                            | Dynamic Operating Supply Current              | 50kHz, $C_L = 1nF$                      |       | 2.5   | 4.0   | mA        |
| $I_{CC(dis)}$                        | Operating Current at Disable                  | $V_{inv} = 0V$                          | 40    | 65    | 90    | $\mu A$   |
| <b>Error Amplifier Section</b>       |                                               |                                         |       |       |       |           |
| $V_{ref1}$                           | Voltage Feedback Input Threshold1             | $T_A = 25^{\circ}C$                     | 2.465 | 2.500 | 2.535 | V         |
|                                      |                                               |                                         | 2.435 | 2.500 | 2.565 | V         |
| $V_{ref2}$                           | Voltage Feedback Input Threshold2             |                                         | 1.45  | 1.50  | 1.55  | V         |
| $\Delta V_{ref1}$                    | Line Regulation                               | $V_{CC} = 14V \sim 23V$                 |       | 0.1   | 10.0  | mV        |
| $\Delta V_{ref3}$                    | Temperature Stability of $V_{ref1}^{(1)}$     |                                         |       | 20    |       | mV        |
| $I_{b(ea)}$                          | Input Bias Current                            | $V_{inv} = 1V \sim 4V$                  | -0.5  |       | 0.5   | $\mu A$   |
| $I_{source}$                         | Output Source Current                         | $V_{inv} = 2.4V$                        |       | -12   |       | $\mu A$   |
| $I_{sink}$                           | Output Sink Current                           | $V_{inv} = 2.6V$                        |       | 12    |       | $\mu A$   |
| $V_{eao(H)}$                         | Output Upper Clamp Voltage                    |                                         | 4.5   | 5.5   | 6.5   | V         |
| $V_{eao(Z)}$                         | Zero Duty Cycle Output Voltage                |                                         | 0.7   | 1.0   | 1.3   | V         |
| gm                                   | Transconductance <sup>(1)</sup>               |                                         | 90    | 115   | 140   | $\mu mho$ |
| $V_{TH(in)}$                         | Output Voltage Selection Threshold            | $T_A = 25^{\circ}C$                     | 1.24  | 1.30  | 1.36  | V         |
| $V_{TH(reset)}$                      | Output Voltage Reset Threshold <sup>(1)</sup> |                                         | 3.0   | 4.5   | 6.0   | V         |
| <b>Maximum On-Time Section</b>       |                                               |                                         |       |       |       |           |
| $V_{mot}$                            | Maximum On-time Voltage                       | $R_{mot} = 13.7k$                       | 0.95  | 1.00  | 1.05  | V         |
| $t_{ON-max}$                         | Maximum On-time Programming                   | $R_{mot} = 13.7k$ , $T_A = 25^{\circ}C$ | 18.0  | 22.5  | 27.0  | $\mu s$   |
| <b>Current Sense Section</b>         |                                               |                                         |       |       |       |           |
| $V_{CS(limit)}$                      | Current Sense Input Threshold Voltage Limit   |                                         | 0.7   | 0.8   | 0.9   | V         |
| $I_{b(cs)}$                          | Input Bias Current                            | $V_{CS} = 0V \sim 1V$                   | -1.0  | -0.1  | 1.0   | $\mu A$   |
| $t_{d(cs)}$                          | Current Sense Delay to Output <sup>(1)</sup>  |                                         |       | 350   | 500   | ns        |

**Electrical Characteristics** (Continued)

$V_{CC} = 14V$ ,  $T_A = -40^{\circ}C \sim 125^{\circ}C$ , unless otherwise specified.

| Symbol                                 | Parameter                                               | Condition                         | Min. | Typ. | Max. | Unit    |
|----------------------------------------|---------------------------------------------------------|-----------------------------------|------|------|------|---------|
| <b>Zero Current Detection Section</b>  |                                                         |                                   |      |      |      |         |
| $V_{TH(ZCD)}$                          | Input Voltage Threshold <sup>(1)</sup>                  |                                   | 1.35 | 1.50 | 1.65 | V       |
| $HY_{(ZCD)}$                           | Detect Hysteresis <sup>(1)</sup>                        |                                   | 0.05 | 0.10 | 0.15 | V       |
| $V_{clamp(h)}$                         | Input High Clamp Voltage                                | $I_{det} = 3mA$                   | 6.0  | 6.7  | 7.4  | V       |
| $V_{clamp(l)}$                         | Input Low Clamp Voltage                                 | $I_{det} = -3mA$                  | 0    | 0.6  | 1.0  | V       |
| $I_{b(ZCD)}$                           | Input Bias Current                                      | $V_{ZCD} = 1V \sim 5V$            | -1.0 | -0.1 | 1.0  | $\mu A$ |
| $I_{source(zcd)}$                      | Source Current Capability <sup>(1)</sup>                |                                   |      |      | -10  | mA      |
| $I_{sink(zcd)}$                        | Sink Current Capability <sup>(1)</sup>                  |                                   |      |      | 10   | mA      |
| $t_{dead}$                             | Maximum Delay from ZCD to Output Turn-on <sup>(1)</sup> |                                   | 100  |      | 200  | ns      |
| <b>Output Section</b>                  |                                                         |                                   |      |      |      |         |
| $V_{OH}$                               | Output Voltage High                                     | $I_O = -100mA$                    | 9.2  | 11.0 | 12.8 | V       |
| $V_{OL}$                               | Output Voltage Low                                      | $I_O = 100mA$                     |      | 1.0  | 2.5  | V       |
| $t_r$                                  | Rising Time <sup>(1)</sup>                              | $C_L = 1nF$                       |      | 50   | 100  | ns      |
| $t_f$                                  | Falling Time <sup>(1)</sup>                             | $C_L = 1nF$                       |      | 50   | 100  | ns      |
| $V_{O(max)}$                           | Maximum Output Voltage                                  | $V_{CC} = 20V$ , $I_O = 100\mu A$ | 11.5 | 13.0 | 14.5 | V       |
| $V_{O(uvlo)}$                          | Output Voltage with UVLO Activated                      | $V_{CC} = 5V$ , $I_O = 100\mu A$  |      |      | 1    | V       |
| <b>Restart Timer Section</b>           |                                                         |                                   |      |      |      |         |
| $t_{d(rst)}$                           | Restart Timer Delay                                     |                                   | 40   | 160  | 360  | $\mu s$ |
| <b>Over-Voltage Protection Section</b> |                                                         |                                   |      |      |      |         |
| $V_{OVP}$                              | OVP Threshold Voltage                                   | $T_A = 25^{\circ}C$               | 2.60 | 2.66 | 2.72 | V       |
| $HY_{(ovp)}$                           | OVP Hysteresis                                          |                                   | 0.06 | 0.11 | 0.16 | V       |
| <b>Enable Section</b>                  |                                                         |                                   |      |      |      |         |
| $V_{TH(en)}$                           | Enable Threshold Voltage                                |                                   | 0.40 | 0.45 | 0.50 | V       |
| $HY_{(en)}$                            | Enable Hysteresis                                       |                                   | 0.05 | 0.10 | 0.15 | V       |

**Note:**

1. These parameters, although guaranteed by design, are not tested in production.

## Typical Performance Characteristics

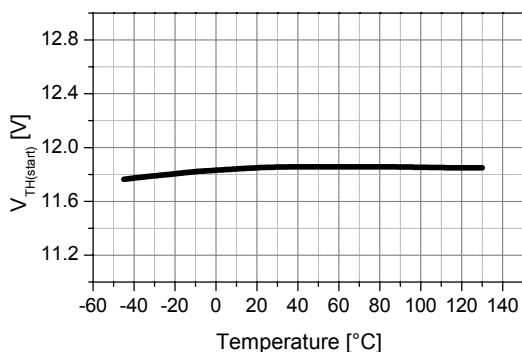


Figure 4. Start Threshold Voltage vs. Temp.

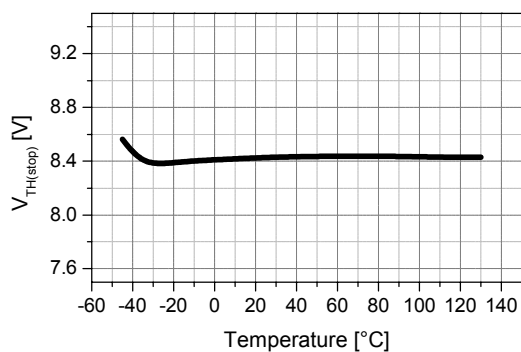


Figure 5. Stop Threshold Voltage vs. Temp.

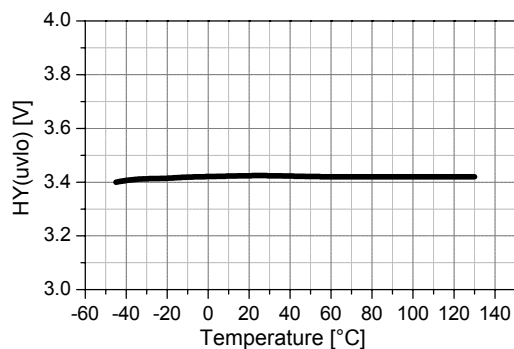


Figure 6. UVLO Hysteresis vs. Temp.

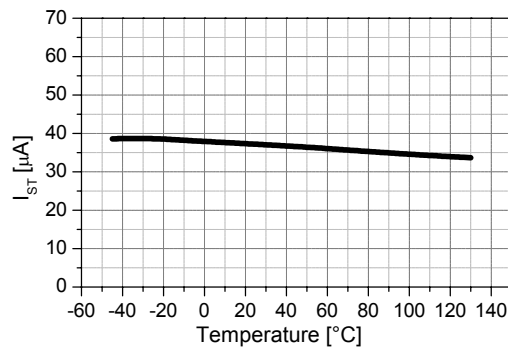


Figure 7. Start-up Supply Current vs. Temp.

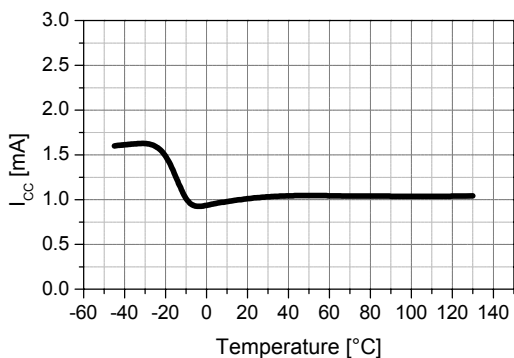


Figure 8. Operating Supply Current vs. Temp.

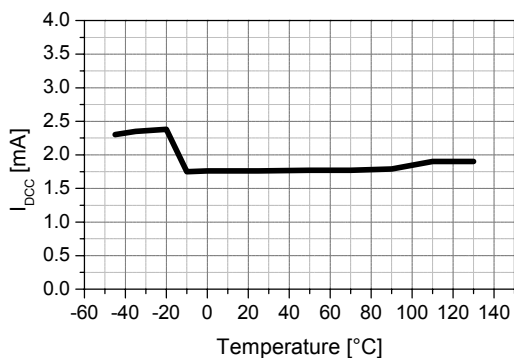


Figure 9. Dynamic Operating Current vs. Temp.

# Typical Performance Characteristics (Continued)

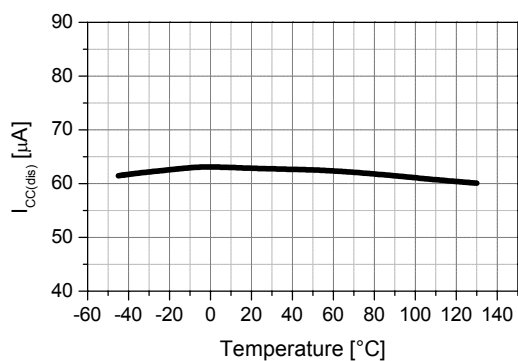


Figure 10.  $I_{CC}$  at Disable vs. Temp.

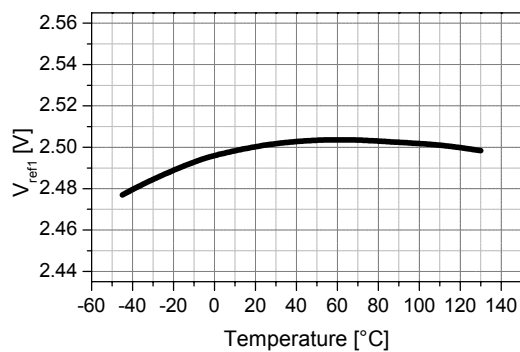


Figure 11.  $V_{ref1}$  vs. Temp.

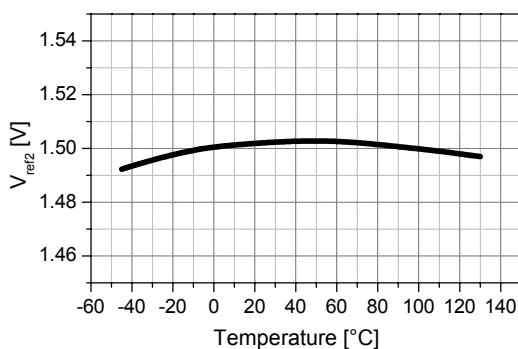


Figure 12.  $V_{ref2}$  vs. Temp.

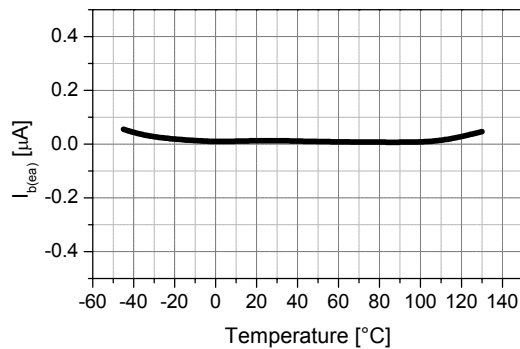


Figure 13. Input Bias Current vs. Temp.

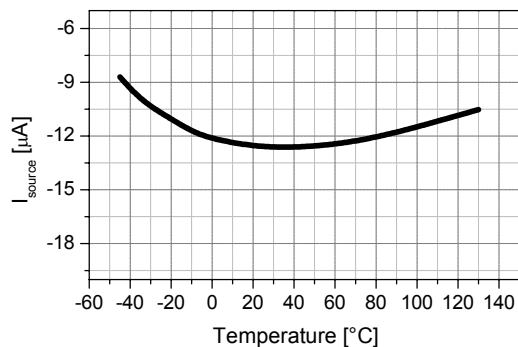


Figure 14. Error Amp. Source Current vs. Temp.

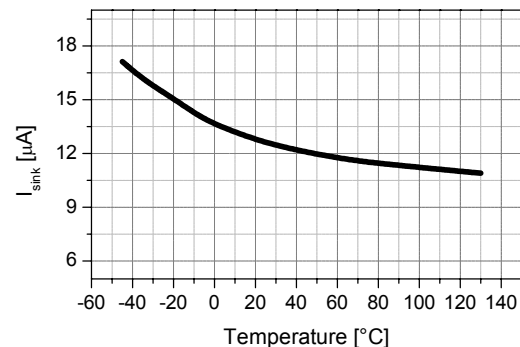


Figure 15. Error Amp. Sink Current vs. Temp.

# Typical Performance Characteristics (Continued)

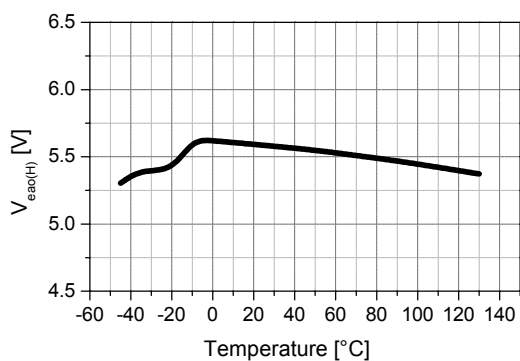


Figure 16. Error Amp. Clamp Voltage vs. Temp.

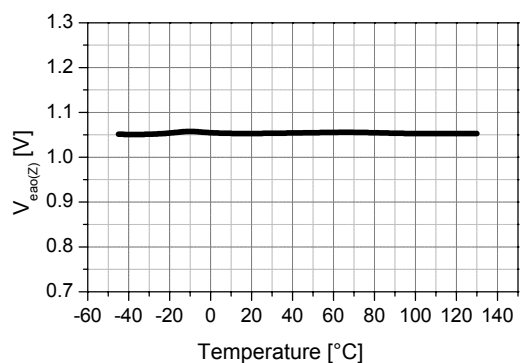


Figure 17. Zero Duty Output Voltage vs. Temp.

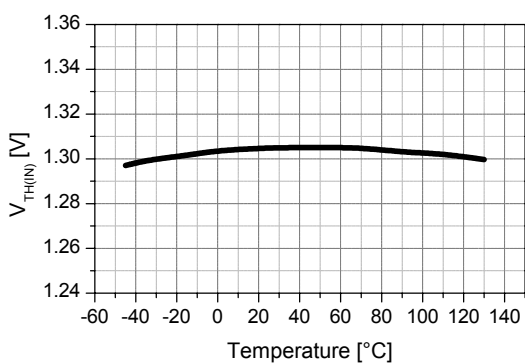


Figure 18. Output Select Threshold vs. Temp.

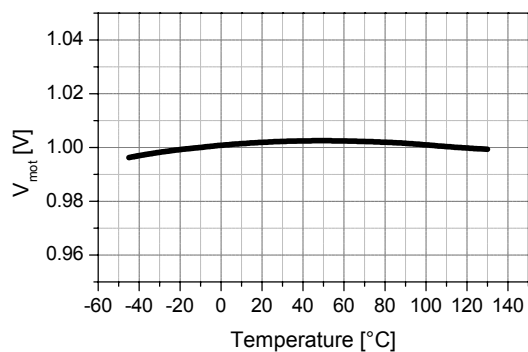


Figure 19. MOT Pin Voltage vs. Temp.

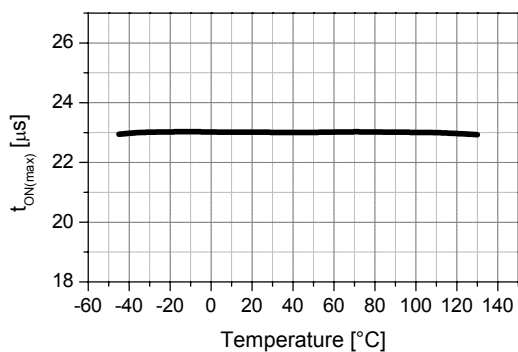


Figure 20. Maximum On-Time vs. Temp.

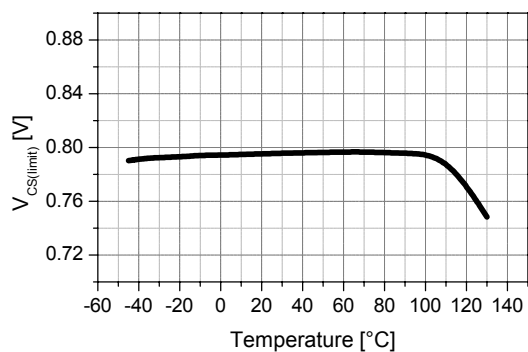


Figure 21. Current Limit vs. Temp.

## Typical Performance Characteristics (Continued)

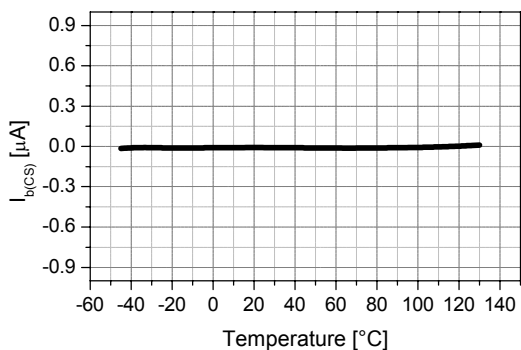


Figure 22. CS Input Bias Current vs. Temp.

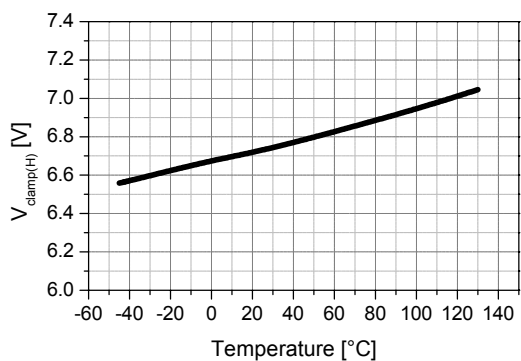


Figure 23. ZCD Input High Clamp vs. Temp.

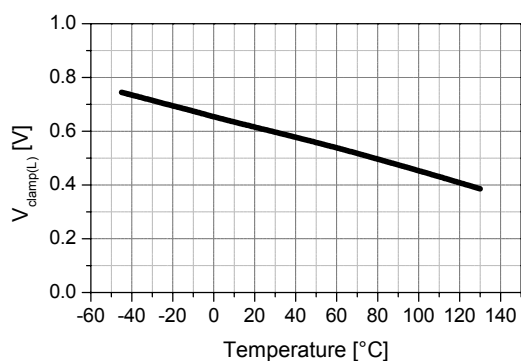


Figure 24. ZCD Input Low Clamp vs. Temp.

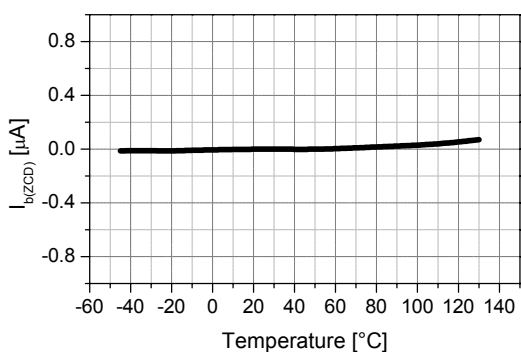


Figure 25. ZCD Input Bias Current vs. Temp.

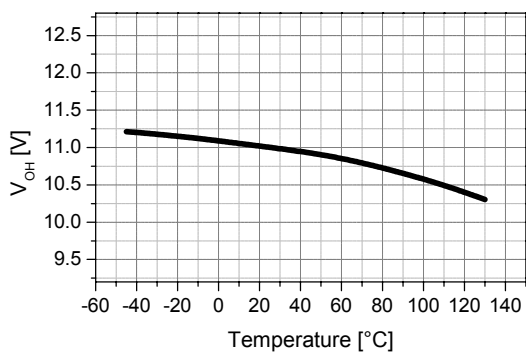


Figure 26. Output Voltage High vs. Temp.

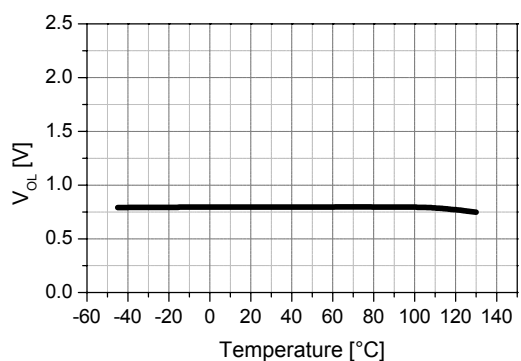


Figure 27. Output Voltage Low vs. Temp.

## Typical Performance Characteristics (Continued)

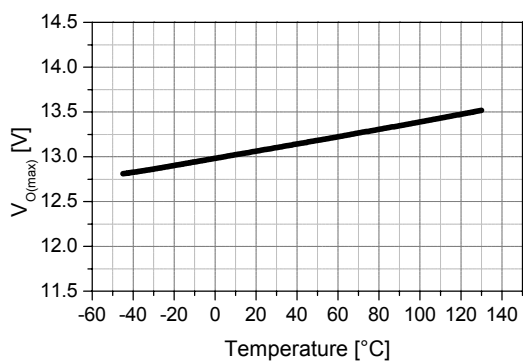


Figure 28. Maximum Output Voltage vs. Temp.

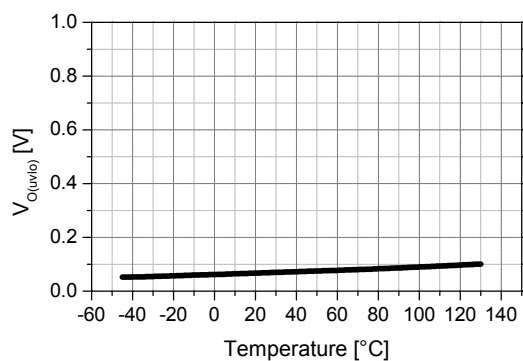


Figure 29. Output Voltage when UVLO vs. Temp.

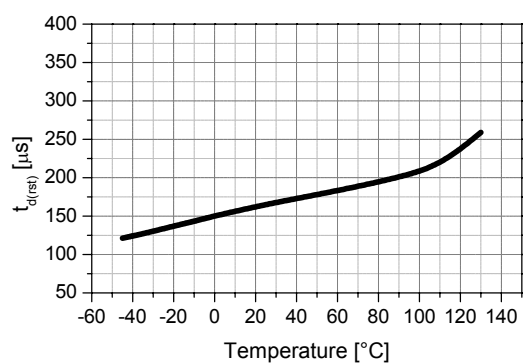


Figure 30. Restart Timer Delay vs. Temp.

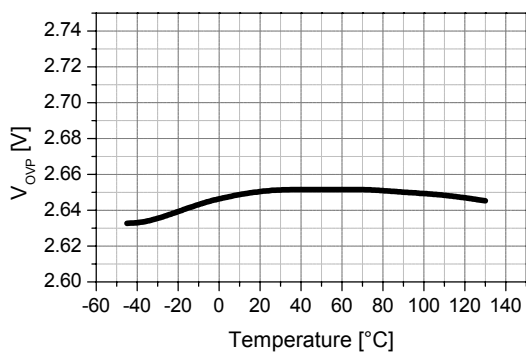


Figure 31. Over-Voltage Protection vs. Temp.

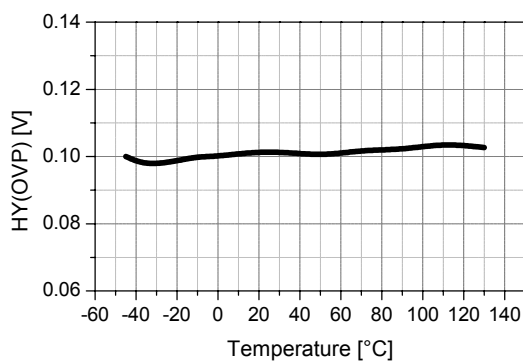


Figure 32. OVP Hysteresis vs. Temp.

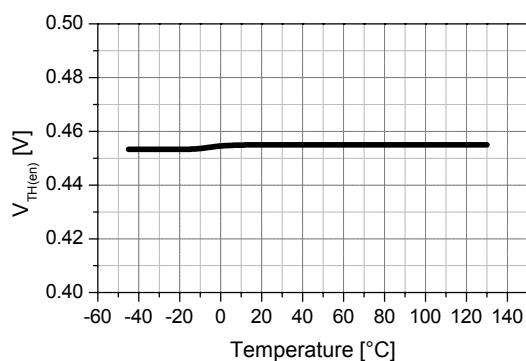
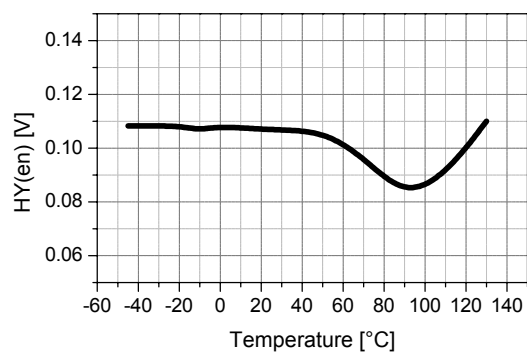


Figure 33. Enable Threshold Voltage vs. Temp.

**Typical Performance Characteristics** (Continued)**Figure 34. Enable Hysteresis vs. Temp.**

## Applications Information

### 1. Error Amplifier Block

The error amplifier block has several functions, such as dual output function, over-voltage protection function, and disable function.

#### 1.1 Dual-Output Function

Unlike conventional CRM PFC controllers, the FAN7528 has the dual-output control function according to the AC line voltage without sensing the rectified AC line voltage. Because the output voltage of the boost converter is proportional to the peak voltage of the input AC line voltage before the boost converter starts switching, the INV pin voltage represents the peak AC line voltage. When the AC line is connected to the boost converter,  $V_{CC}$  voltage starts to increase from zero voltage. If the  $V_{CC}$  voltage reaches 8.5V, the dual-output reference generator compares the INV pin voltage with 1.3V reference and, if the INV pin voltage is lower than 1.3V, the dual-output reference generator sets the reference voltage of the error amplifier to 1.5V. If the INV pin voltage is higher than 1.3V, the reference voltage is set to 2.5V. That means if the output voltage of the boost converter is set to 400V at high line, the output voltage is 240V ( $400V \times 1.5/2.5$ ) at low line. If the output voltage is set to 390V at high line, the output voltage is 234V at low line. Because this block does not need the input voltage sensing network, the power loss and cost related with the sensing network can be saved. The reference voltage of the error amplifier is not reset until  $V_{CC}$  goes below 4.5V.

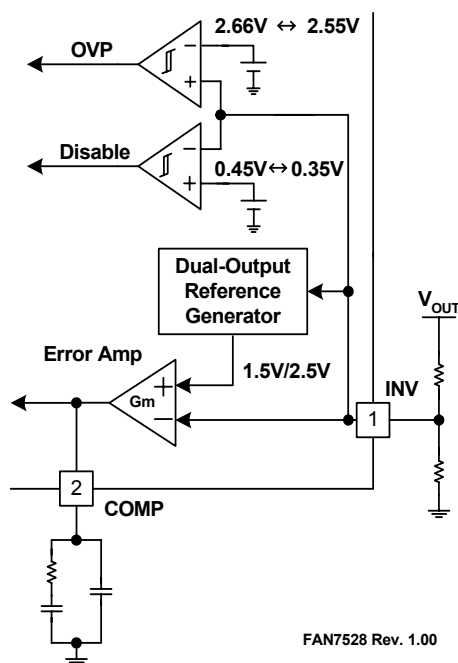


Figure 35. Error Amplifier Block

### 1.2 Over-Voltage Protection Function

The control speed of the PFC converter is very slow; therefore, the over-voltage protection (OVP) of the output voltage is very important. The FAN7528 provides a precise OVP function that shuts down the drive circuit when the INV pin voltage exceeds 2.66V and there is 0.11V hysteresis.

### 1.3 Disable Function

If the INV pin voltage is lower than 0.45V, most of the internal block is disabled, the operating current is reduced to be 65μA, and there is 0.1V hysteresis in the comparator.

### 1.4 Error Amplifier

The error amplifier is a transconductance type amplifier. The output current of the amplifier is proportional to the voltage difference between the inverting input and the non-inverting input of the amplifier. Some resistors and capacitors should be connected to the error amplifier output pin, the COMP pin, for the output voltage loop compensation.

## 2. Zero Current Detection Block

The zero current detector (ZCD) generates the turn-on signal of the MOSFET when the boost inductor current reaches zero using an auxiliary winding coupled with the inductor. If the voltage of the ZCD pin goes higher than 1.5V, the ZCD comparator waits until the voltage goes below 1.4V. If the voltage goes below 1.4V, the zero current detector turns on the MOSFET. The ZCD pin is protected internally by two clamps, 6.7V high clamp and 0.6V low clamp. The 160μs timer generates a MOSFET turn-on signal if the drive output has been low for more than 160μs from the falling edge of the drive output.

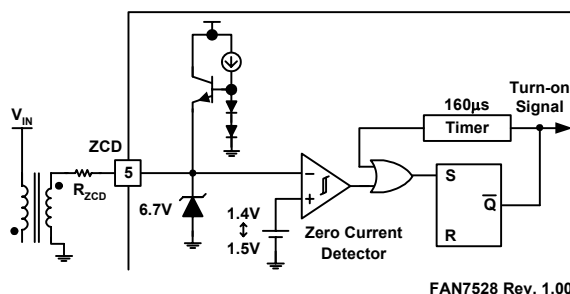


Figure 36. Zero Current Detector Block

### 3. Sawtooth Generator Block

The output of the error amplifier and the output of the sawtooth generator are compared to determine the MOSFET turn-off instance. The slope of the sawtooth is determined by an external resistor connected to the MOT pin. The voltage of the MOT pin is 1V and the slope is proportional to the current flowing out of the MOT pin. The internal ramp signal has 1V offset; therefore, the drive output is shut down if the voltage of the COMP pin is lower than 1V. The MOSFET on-time is maximum when the COMP pin voltage is 5V. According to the slope of the internal ramp, the maximum on-time can be programmed. The necessary maximum on-time depends on the boost inductor, lowest AC line voltage, and maximum output power. The resistor value should be designed properly.

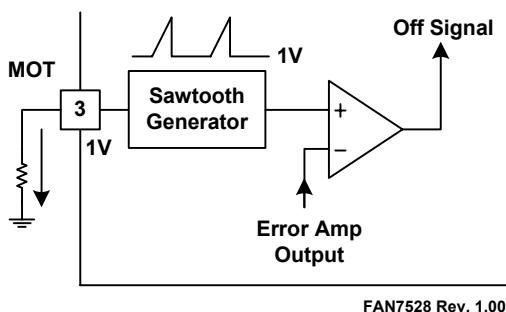


Figure 37. Sawtooth Generator Block

### 4. Over-Current Protection Block

The MOSFET current is sensed using an external sensing resistor for the over-current protection. If the CS pin voltage is higher than 0.8V, the over-current protection comparator generates a protection signal. An internal RC filter is included to filter switching noise.

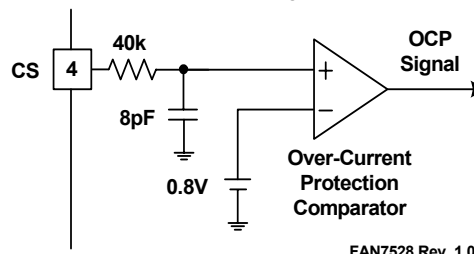


Figure 38. Over-Current Protection Block

### 5. Switch Drive Block

The FAN7528 contains a single totem-pole output stage designed for a direct drive of power MOSFET. The drive output is capable of up to 400mA peak current with a typical rise and fall time of 50ns with 1nF load. The output voltage is clamped to be 13V to protect MOSFET gate even if the  $V_{CC}$  voltage is higher than 13V.

### 6. Under-Voltage Lockout Block

If the  $V_{CC}$  voltage reaches 12V, the IC's internal blocks are enabled and start operation. If the  $V_{CC}$  voltage drops below 8.5V, most of the internal blocks are disabled to reduce the operating current.  $V_{CC}$  voltage should be higher than 8.5V under normal conditions.

## Typical Application Circuit

| Application | Output power | Input voltage                   | Output voltage |
|-------------|--------------|---------------------------------|----------------|
| Adapter     | 100W         | Universal input<br>(90~264 Vac) | 389V/232V      |

### Features

- High efficiency (>90% at 90 Vac input)
- Low THD (total harmonic distortion) (<10% at 264 Vac input)
- Dual-output control

### Key Design Notes

- Diode D4 is used to prevent IC malfunction that can happen if the CS pin voltage is lower than -0.3V.
- Important components for low THD are R2, R5, and C11.

### 1. Schematic

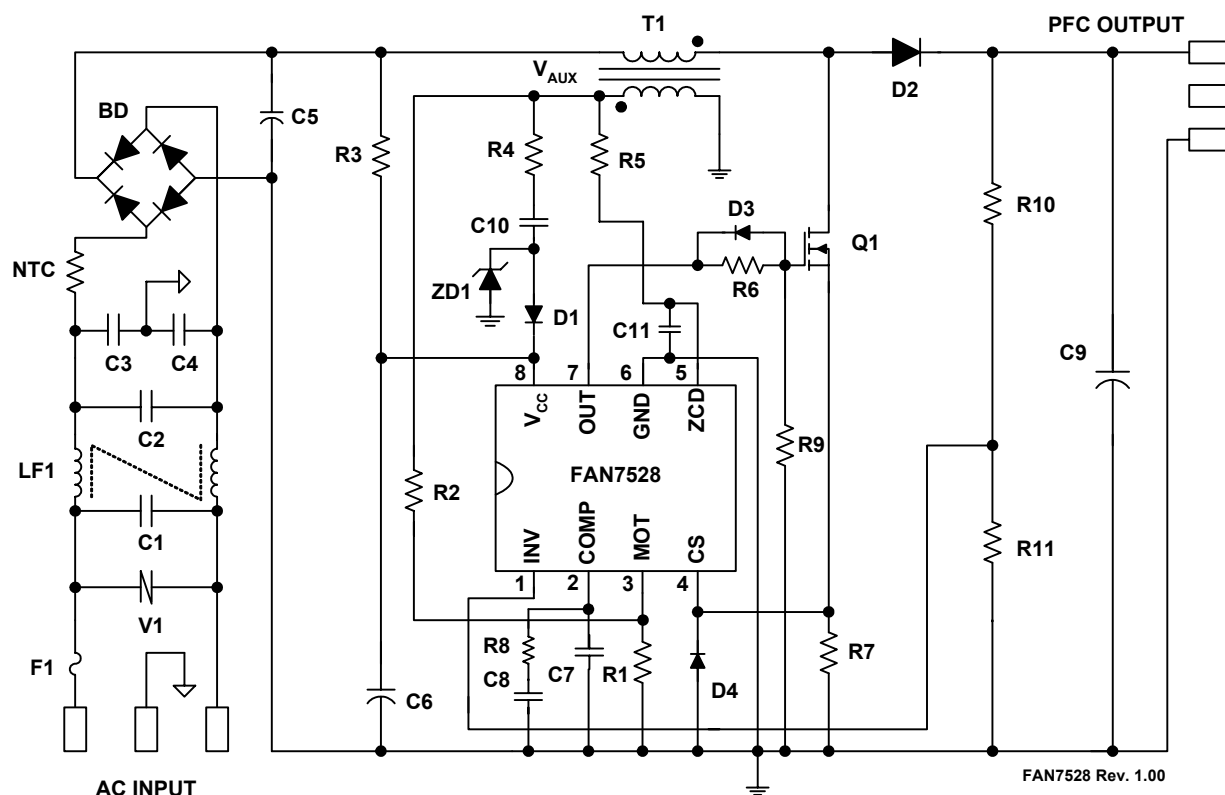
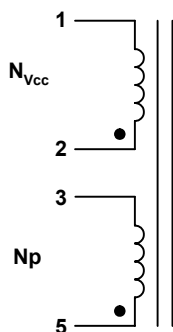


Figure 39. Schematic

## 2. Inductor Schematic Diagram



FAN7528 Rev. 1.00

Figure 40. Inductor Schematic Diagram

## 3. Winding Specification

| No                                                     | Pin (s→f) | Wire                  | Turns | Winding Method   |
|--------------------------------------------------------|-----------|-----------------------|-------|------------------|
| N <sub>p</sub>                                         | 5 → 3     | 0.2 <sup>ϕ</sup> × 10 | 44    | Solenoid Winding |
| Insulation: Polyester Tape t = 0.050mm, 4 Layers       |           |                       |       |                  |
| N <sub>Vcc</sub>                                       | 2 → 1     | 0.2 <sup>ϕ</sup> × 1  | 6     | Solenoid Winding |
| Outer Insulation: Polyester Tape t = 0.050mm, 4 Layers |           |                       |       |                  |
| Air Gap: 0.6mm for each leg                            |           |                       |       |                  |

## 4. Electrical Characteristics

|            | Pin | Specification | Remarks    |
|------------|-----|---------------|------------|
| Inductance | 3–5 | 400μH ± 10%   | 100kHz, 1V |

## 5. Core & Bobbin

- Core: EI 3026
- Bobbin: EI3026
- Ae(mm<sup>2</sup>): 111

## 6. Demo Circuit Part List

| Part             | Value            | Note                   | Part                | Value       | Note       |
|------------------|------------------|------------------------|---------------------|-------------|------------|
| <b>Fuse</b>      |                  |                        | <b>Inductor</b>     |             |            |
| F1               | 3A/250V          |                        | T1                  | 400 $\mu$ H | EI3026     |
| <b>NTC</b>       |                  |                        |                     |             |            |
| NTC              | 10D-9            |                        | <b>MOSFET</b>       |             |            |
| <b>Resistor</b>  |                  |                        | Q1                  | FQPF13N50C  | Fairchild  |
| R1               | 10k $\Omega$     | 1/4W                   |                     |             |            |
| R2               | 370k $\Omega$    | 1/4W                   | <b>Diode</b>        |             |            |
| R3               | 330k $\Omega$    | 1/2W                   | D1                  | 1N4148      | Fairchild  |
| R4               | 150 $\Omega$     | 1/2W                   | D2                  | BYV26C      | 600V, 1A   |
| R5               | 20k $\Omega$     | 1/4W                   | D3                  | 1N5819      | Fairchild  |
| R6               | 10 $\Omega$      | 1/4W                   | D4                  | 1N5819      | Fairchild  |
| R7               | 0.22 $\Omega$    | 1/2W                   | ZD1                 | 1N4746      | 18V        |
| R8               | 10k $\Omega$     | 1/4W                   |                     |             |            |
| R9               | 10k $\Omega$     | 1/4W                   | <b>Bridge Diode</b> |             |            |
| R10              | 2M $\Omega$      | 1/4W                   | BD                  | KBL06       | 600V/4A    |
| R11              | 12.9k $\Omega$   | 1/4W                   |                     |             |            |
| <b>Capacitor</b> |                  |                        | <b>Line Filter</b>  |             |            |
| C1               | 150nF/275VAC     | Box Capacitor          | LF1                 | 40mH        | Wire 0.4mm |
| C2               | 330nF/275VAC     | Box Capacitor          |                     |             |            |
| C3               | 2.2nF/3kV        | Ceramic Capacitor      | <b>IC</b>           |             |            |
| C4               | 2.2nF/3kV        | Ceramic Capacitor      | IC1                 | FAN7528     | Fairchild  |
| C5               | 150nF/630V       | Film Capacitor         |                     |             |            |
| C6               | 47 $\mu$ F/25V   | Electrolytic Capacitor | <b>TNR</b>          |             |            |
| C7               | 47nF/50V         | Ceramic Capacitor      | V1                  | 471         | 470V       |
| C8               | 220nF            | MLCC                   |                     |             |            |
| C9               | 100 $\mu$ F/450V | Electrolytic Capacitor |                     |             |            |
| C10              | 12nF/100V        | Film Capacitor         |                     |             |            |
| C11              | 47pF/50V         | Ceramic Capacitor      |                     |             |            |

## 7. Layout

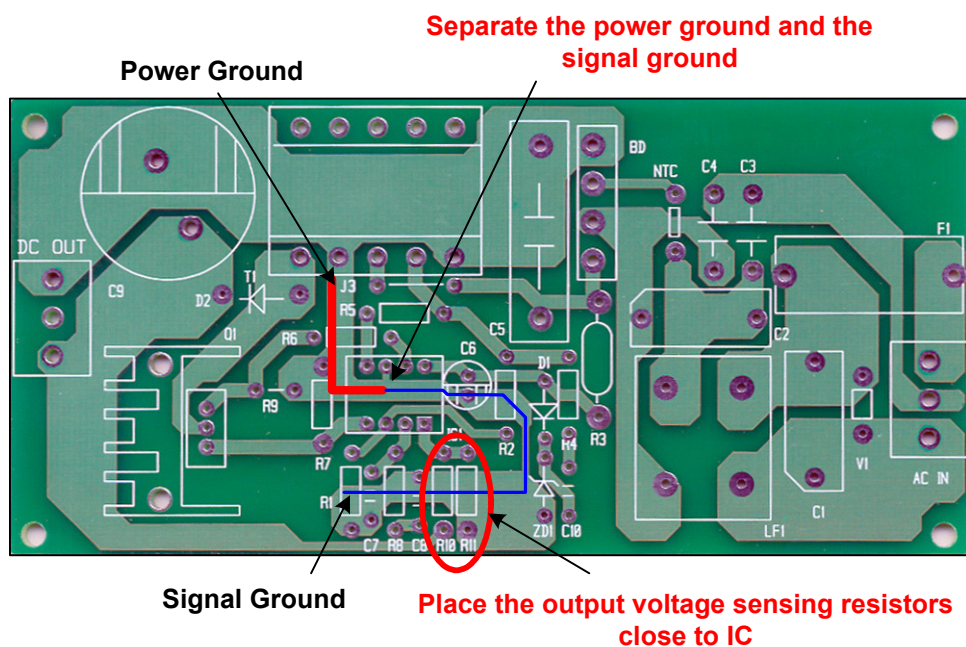


Figure 41. PCB Layout Considerations for FAN7528

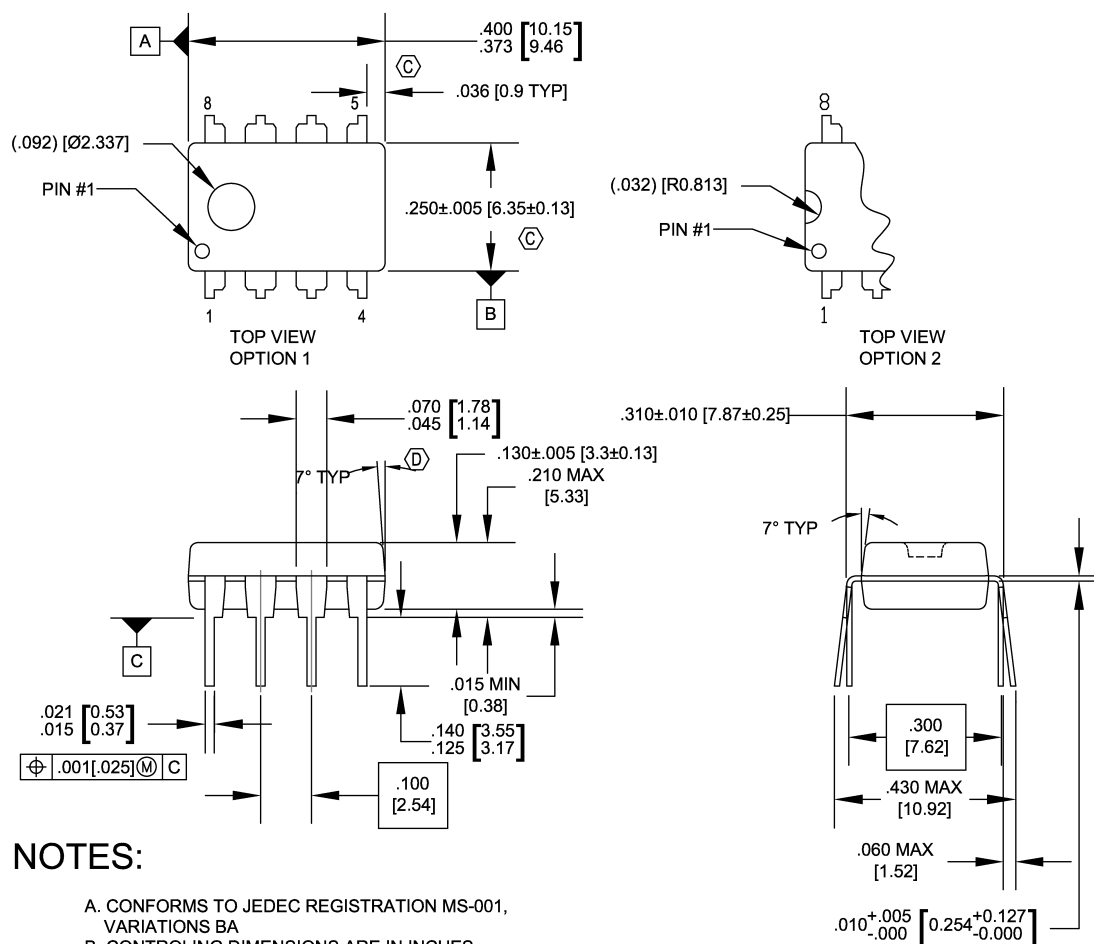
## 8. Performance Data

|      |     | 90 Vac | 110 Vac | 220 Vac | 264 Vac |
|------|-----|--------|---------|---------|---------|
| 100W | PF  | 0.999  | 0.998   | 0.991   | 0.983   |
|      | THD | 3.5%   | 3.6%    | 6.1%    | 7.3%    |
| 50W  | PF  | 0.997  | 0.996   | 0.971   | 0.947   |
|      | THD | 5.1%   | 5.5%    | 11.1%   | 13.0%   |

## Mechanical Dimensions

### 8-DIP

Dimensions are in millimeters unless otherwise noted.



### NOTES:

- CONFORMS TO JEDEC REGISTRATION MS-001, VARIATIONS BA
- CONTROLLING DIMENSIONS ARE IN INCHES  
REFERENCE DIMENSIONS ARE IN MILLIMETERS
- DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCHES OR 0.25MM.
- DOES NOT INCLUDE DAMBAR PROTRUSIONS.  
DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 INCHES OR 0.25MM.
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

N08EREVG

Figure 42. 8-Lead Dual In-Line Package (DIP)

# Mechanical Dimensions

## 8-SOP

Dimensions are in millimeters unless otherwise noted.

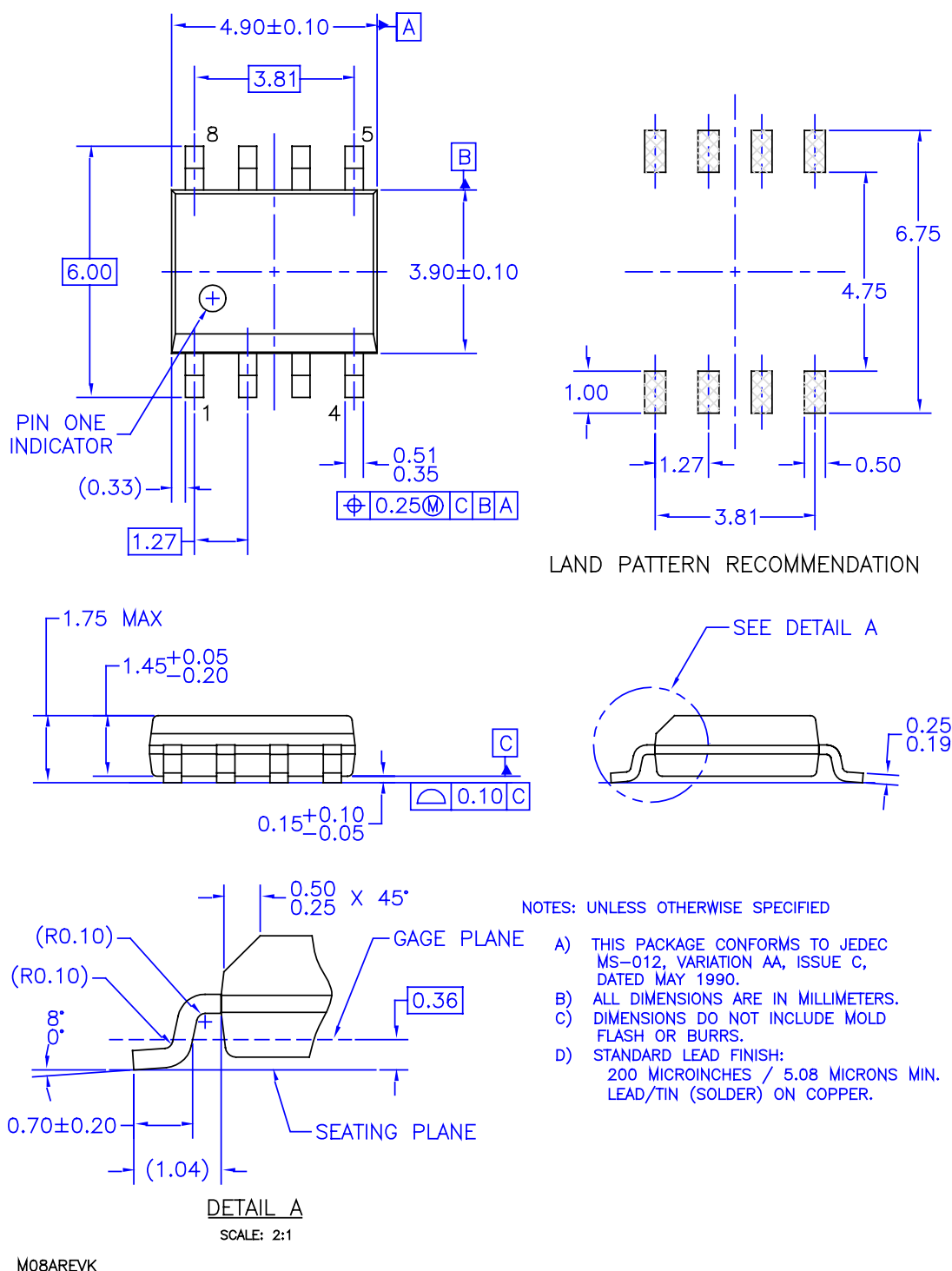


Figure 43. 8-Lead Small Outline Package (SOP)

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