

INTERNATIONAL RECTIFIER



HEXFET® TRANSISTORS

**COMBINATION
N AND P CHANNEL
(2 EACH)
POWER MOSFETs**

14 LEAD DUAL-IN-LINE QUAD
(CERAMIC SIDE BRAZED PACKAGE)

**IRFG6110****2N7336****JANTX2N7336****JANTXV2N7336****[REF: MIL-S-19500/598]**

**100 Volt, 0.7 Ohm (N-Channel) and
-100 Volt, 1.40 Ohm (P-Channel)**

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dv/dt capability.

Ideal for ac applications, the P and N-Channel dice are physical complements such that their similar switching characteristics and their opposite polarity offers circuit simplification as well as all the other well established advantages of MOSFETs.

They are well suited for both military and commercial applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

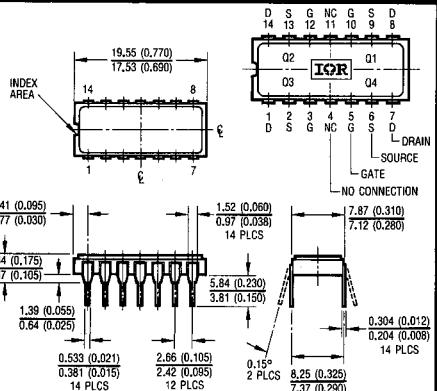
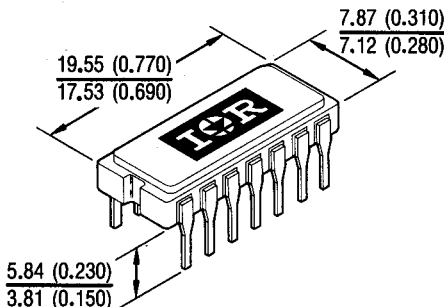
Product Summary

Part Number	BV _{DSS}	R _{DS(on)}		I _D	
		N	P	N	P
IRFG6110	±100V	0.70Ω	1.4Ω	1.0A	-0.75A

Features:

- Avalanche Energy Rating
- Dynamic dv/dt Rating
- Hermetically Sealed
- For Automatic Insertion
- Lightweight
- Simple Drive Requirements
- Ease of Paralleling
- 2 N-Channel/2 P-Channel Co-Packaged HEXFETs

CASE STYLE AND DIMENSIONS



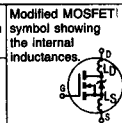
Conforms to JEDEC MO-036AB
Dimensions in Millimeters and (Inches)

Absolute Maximum Ratings For Each Chip ① ⑤

Parameter		N-Channel	P-Channel	Units
I_D @ $V_{GS} = \pm 10V, T_C = 25^\circ C$	Continuous Drain Current	1.0	-0.75	A
I_D @ $V_{GS} = \pm 10V, T_C = 100^\circ C$	Continuous Drain Current	0.6	-0.5	
I_{DM}	Pulsed Drain Current	4.0	-3.0	
P_D @ $T_C = 25^\circ C$	Max. Power Dissipation	1.4	1.4	W
	Linear Derating Value	0.011	0.011	W/K ⑤
V_{GS}	Gate-to-Source Voltage	± 20	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	75	75	mJ
dv/dt	Peak Diode Recovery ③	5.5	-5.5	V/ns
T_J	Operating Junction Temperature	-55 to 150		$^\circ C$
T_{STG}	Storage Temperature Range			
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		
	Weight	1.3 (typical)		g

Electrical Characteristics For Each N-Channel Chip @ $T_J = 25^\circ C$ (Unless Otherwise Specified)

Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS} Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V$, $I_D = 1.0$ mA
$\Delta BV_{DSS}/\Delta T_J$ Temperature Coefficient of Breakdown Voltage	—	0.13	—	V/ $^\circ C$	Reference to $25^\circ C$, $I_D = 1.0$ mA
$R_{DS(on)}$ Static Drain-to-Source On-State Resistance	—	—	0.70	Ω	$V_{GS} = 10V$, $I_D = 0.6A$
	—	—	0.80		$V_{GS} = 10V$, $I_D = 1.0A$ ④
$V_{GS(th)}$ Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$
g_{fs} Forward Transconductance	0.86	—	—	S (n)	$V_{DS} \geq 15V$, $I_{DS} = 0.60A$ ④
I_{DSS} Zero Gate Voltage Drain Current	—	—	25	μA	$V_{DS} = 0.8 \times \text{Max. Rating}$, $V_{GS} = 0V$
	—	—	250		$V_{DS} = 0.8 \times \text{Max. Rating}$, $V_{GS} = 0V$, $T_J = 125^\circ C$
I_{GSS} Gate-to-Source Leakage Forward	—	—	100	nA	$V_{GS} = 20V$
I_{GSS} Gate-to-Source Leakage Reverse	—	—	-100	nA	$V_{GS} = -20V$
Q_g Total Gate Charge	—	—	15	nC	$V_{GS} = 10V$, $I_D = 1.0A$
Q_{gs} Gate-to-Source Charge	—	—	7.5		$V_{DS} = 0.5 \times \text{Max. Rating}$
Q_{gd} Gate-to-Drain ("Miller") Charge	—	—	7.5		See Fig. 6 and 14
$t_{d(on)}$ Turn-On Delay Time	—	—	20	ns	$V_{DD} = 50V$, $I_D = 1.0A$, $R_G = 240$
t_r Rise Time	—	—	25		See Fig. 11
$t_{d(off)}$ Turn-Off Delay Time	—	—	40		
t_f Fall Time	—	—	40		
L_D Internal Drain Inductance	—	4.0	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S Internal Source Inductance	—	6.0	—		Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss} Input Capacitance	—	180	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$
C_{oss} Output Capacitance	—	82	—		$f = 1.0$ MHz
C_{res} Reverse Transfer Capacitance	—	15	—		See Fig. 5



Source-Drain Diode Ratings and Characteristics for Each N-Channel Chip

Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S Continuous Source Current (Body Diode)	—	—	1.0	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier. 
I_{SM} Pulsed Source Current (Body Diode) ①	—	—	4.0		
V_{SD} Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}$, $I_S = 1.0\text{A}$, $V_{GS} = 0\text{V}$ ④
t_{rr} Reverse Recovery Time	—	—	200	ns	$T_J = 25^\circ\text{C}$, $I_F = 1.0\text{A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$
Q_{RR} Reverse Recovery Charge	—	—	0.83	μC	$V_{DD} \leq 50\text{V}$
t_{on} Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① Repetitive Rating: Pulse width limited by maximum junction temperature (see figure 9) Refer to current HEXFET reliability report

② @ $V_{DD} = 25\text{V}$. Starting $T_J = 25^\circ\text{C}$
 $L \geq 112\text{ mH}$, $R_G = 25\Omega$
Peak $I_L = 1.0\text{A}$

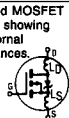
③ $I_{SD} \leq 1.0\text{A}$, $di/dt \leq 75\text{ A}/\mu\text{s}$
 $V_{DD} \leq BV_{DSS}$, $T_J \leq 150^\circ\text{C}$
Suggested $R_G = 24\Omega$

④ Pulse width $\leq 300\text{ }\mu\text{s}$; Duty Cycle $\leq 2\%$

⑤ $K/W = ^\circ\text{C}/\text{W}$
 $W/K = \text{W}/^\circ\text{C}$

Electrical Characteristics For Each P-Channel Chip @ $T_J = 25^\circ\text{C}$ (Unless Otherwise Specified)

Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS} Drain-to-Source Breakdown Voltage	-100	—	—	V	$V_{GS} = 0V, I_D = -1.0\text{ mA}$
$\Delta BV_{DSS}/\Delta T_J$ Temperature Coefficient of Breakdown Voltage	—	-0.098	—	V/°C	Reference to 25°C , $I_D = -1.0\text{ mA}$
$R_{DS(on)}$ Static Drain-to-Source On-State Resistance	—	—	1.4	Ω	$V_{GS} = -10V, I_D = -0.50A$ ①
	—	—	1.73		$V_{GS} = -10V, I_D = -0.75A$
$V_{GS(th)}$ Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$
g_{fs} Forward Transconductance	0.67	—	—	S (Ω)	$V_{DS} \geq -15V, I_{DS} = -0.50A$ ②
I_{DSS} Zero Gate Voltage Drain Current	—	—	-25	μA	$V_{DS} = 0.8 \times \text{Max. Rating}, V_{GS} = 0V$
	—	—	-250		$V_{DS} = 0.8 \times \text{Max. Rating}$ $V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS} Gate-to-Source Leakage Forward	—	—	-100	nA	$V_{GS} = -20V$
I_{GSS} Gate-to-Source Leakage Reverse	—	—	100		$V_{GS} = 20V$
Q_g Total Gate Charge	—	—	15	nC	$V_{GS} = -10V, I_D = -0.75A$
Q_{gs} Gate-to-Source Charge	—	—	7.0		$V_{DS} = 0.5 \times \text{Max. Rating}$
Q_{gd} Gate-to-Drain ("Miller") Charge	—	—	8.0		See Fig. 20 and 28 ④
$t_{d(on)}$ Turn-On Delay Time	—	—	30	ns	$V_{DD} = -50V, I_D = -0.75A, R_G = 24\Omega$
t_r Rise Time	—	—	60		See Fig. 25
$t_{d(off)}$ Turn-Off Delay Time	—	—	40		
t_f Fall Time	—	—	40		
L_D Internal Drain Inductance	—	4.0	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S Internal Source Inductance	—	6.0	—		Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss} Input Capacitance	—	200	—	pF	$V_{GS} = 0V, V_{DS} \leq -25V$
C_{oss} Output Capacitance	—	85	—		$f = 1.0\text{ MHz}$
C_{rss} Reverse Transfer Capacitance	—	30	—		See Fig. 19



Source-Drain Diode Ratings and Characteristics for Each P-Channel Chip

Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S Continuous Source Current (Body Diode)	—	—	-0.75	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier.
I_{SM} Pulsed Source Current (Body Diode) ①	—	—	-3.0		
V_{SD} Diode Forward Voltage	—	—	-5.5	V	$T_J = 25^\circ\text{C}, I_S = -0.75A, V_{GS} = 0V$ ④
t_{rr} Reverse Recovery Time	—	—	200	ns	$T_J = 25^\circ\text{C}, I_F = -0.75A, di/dt \leq -100\text{ A}/\mu\text{s}$
Q_{RR} Reverse Recovery Charge	—	—	9.0	μC	$V_{DD} \leq -50V$
t_{on} Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$				

① Repetitive Rating: Pulse width limited by maximum junction temperature (see figure 23)
Refer to current HEXFET reliability report

③ $I_{SD} \leq -0.75A, di/dt \leq -75\text{ A}/\mu\text{s}$
 $V_{DD} \leq BV_{DSS}, T_J \leq 150^\circ\text{C}$
Suggested $R_G = 24\Omega$

⑤ $K/W = ^\circ\text{C}/W$
 $W/K = W/^\circ\text{C}$

② $V_{DD} = -25V$. Starting $T_J = 25^\circ\text{C}$
 $L \geq 200\text{ mH}, R_G = 24\Omega$
Peak $I_L = -0.75A$

④ Pulse width $\leq 300\text{ }\mu\text{s}$; Duty Cycle $\leq 2\%$

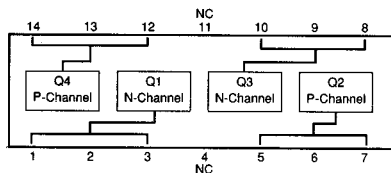
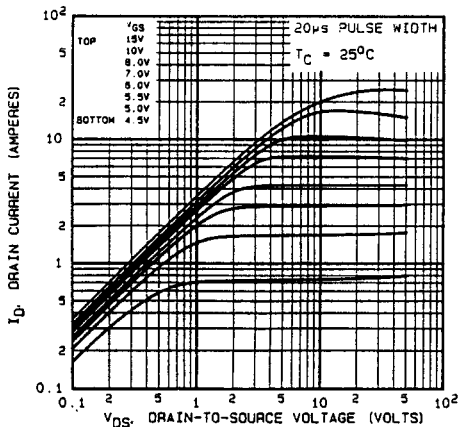
Power Ratings

Power Ratings Test	Single FET	All Four FETs With Equal Power	Units
P_D @ $T_A = 25^\circ\text{C}$ Max. Power Dissipation	1.4	2.5	W
L_{DF} Linear Derating Factor	0.011	0.020	W/K
R_{thJC} Thermal Resistance Junction-to-Case	17	—	K/W
R_{thJA} Thermal Resistance Junction-to-Ambient	90	50	K/W
K_1, K_2 Thermal Coupling Factors	45	40	%

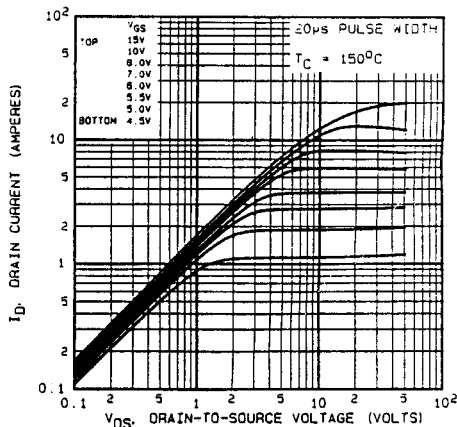
The temperature rise of each device within the package is the result of the power dissipated by the device itself and the power dissipated by the other devices. The power dissipated by the adjacent devices does not have the same effect as the power dissipated within the junction itself. The temperature rise for any particular unit (e.g. (1)) within the package can be calculated with the following expression:

$$(1) \Delta T_1 = 90 (P_1 + K_{12} P_2)$$

where the K_{ij} are the thermal coupling coefficients shown in the Power Ratings Table.


**N-Channel
Q1, Q3**


**Fig. 1 — Typical Output Characteristics,
 $T_C = 25^\circ\text{C}$**



**Fig. 2 — Typical Output Characteristics,
 $T_C = 150^\circ\text{C}$**

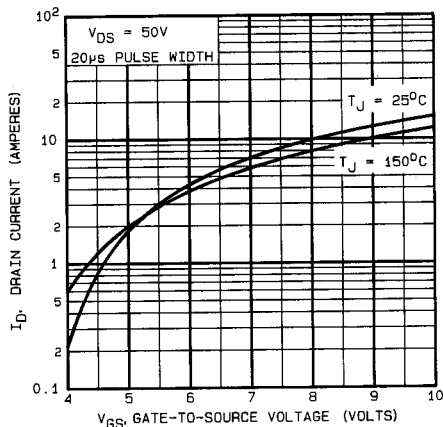


Fig. 3 — Typical Transfer Characteristics

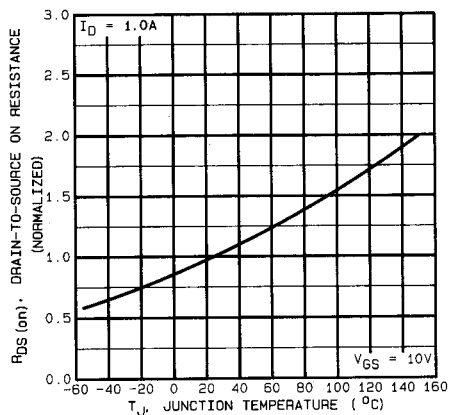


Fig. 4 — Normalized On-Resistance Vs. Temperature

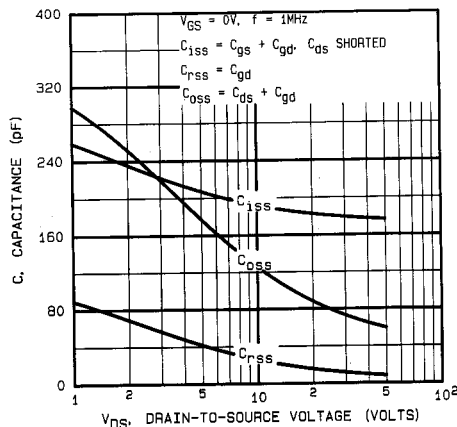


Fig. 5 — Typical Capacitance Vs. Drain-to-Source Voltage

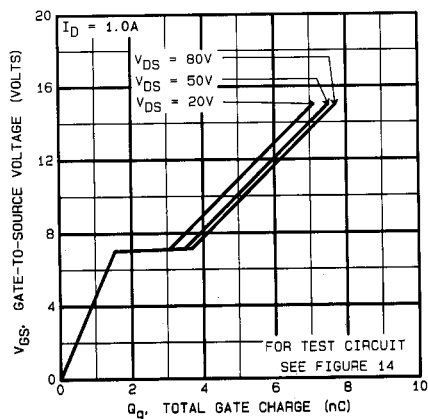


Fig. 6 — Typical Gate Charge Vs. Gate-to-Source Voltage

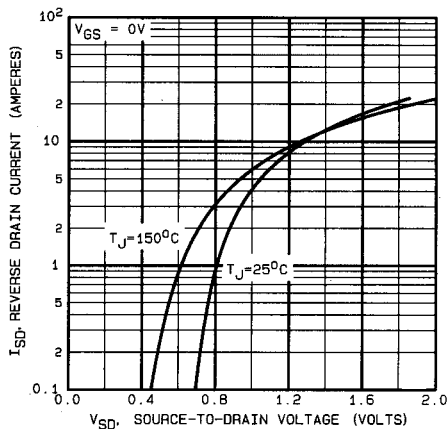


Fig. 7 — Typical Source-Drain Diode Forward Voltage

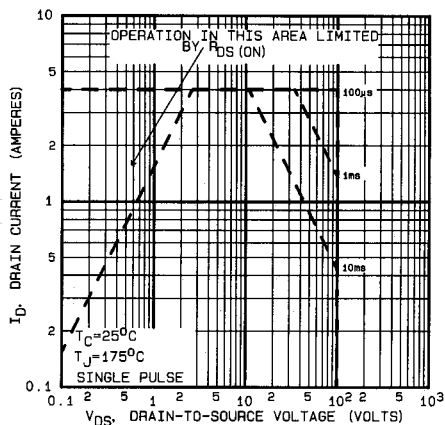


Fig. 8 — Maximum Safe Operating Area

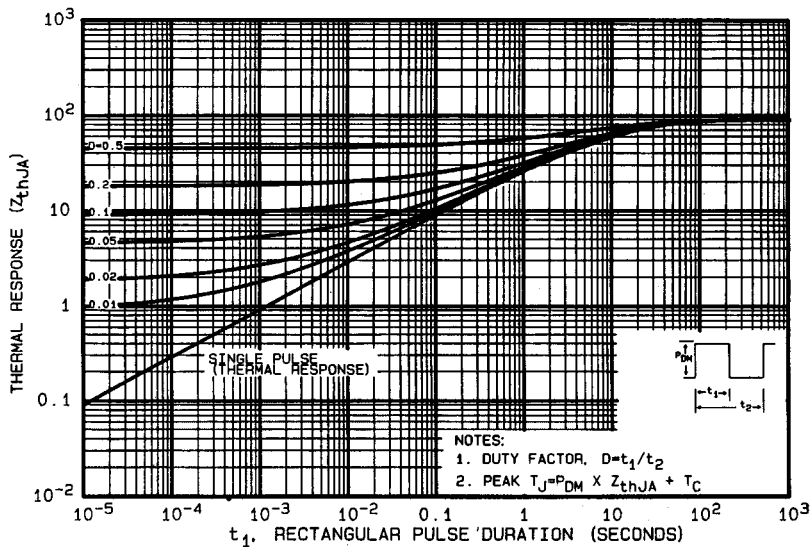


Fig. 9 — Maximum Effective Transient Thermal Impedance, Junction-to-Ambient Vs. Pulse Duration

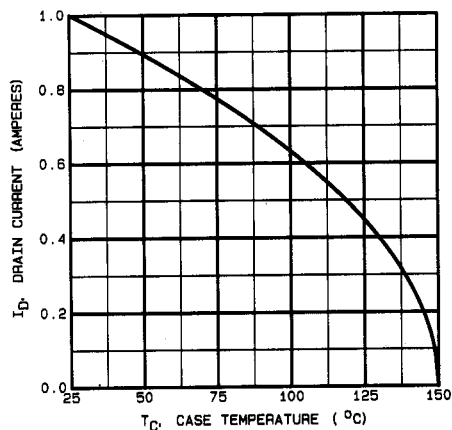


Fig. 10 — Maximum Drain Current Vs. Case Temperature

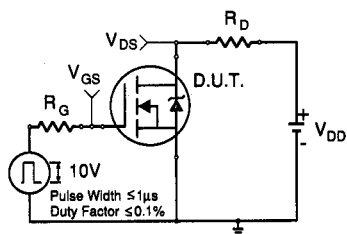


Fig. 11a — Switching Time Test Circuit

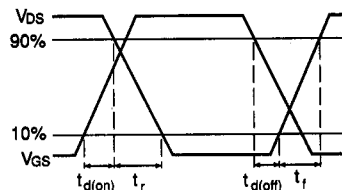


Fig. 11b — Switching Time Waveforms

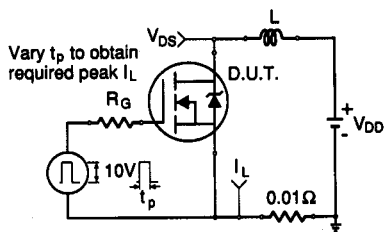


Fig. 12a — Unclamped Inductive Test Circuit

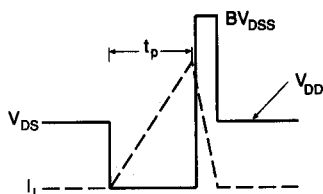


Fig. 12b — Unclamped Inductive Waveforms

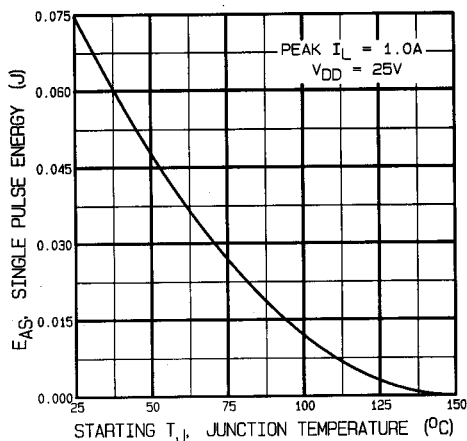


Fig. 12c — Maximum Avalanche Energy Vs. Starting Junction Temperature

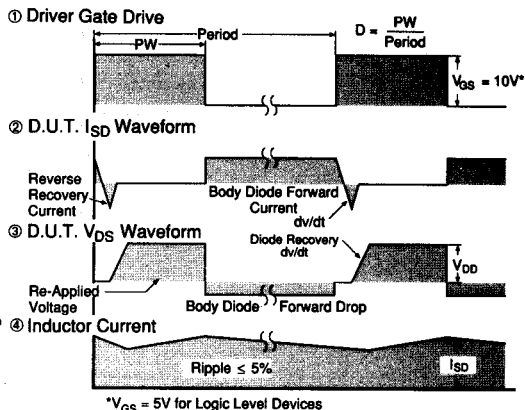
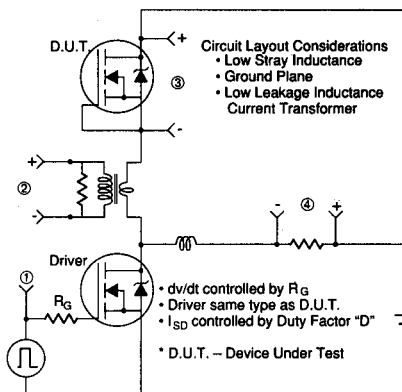


Fig. 13—Peak Diode Recovery dv/dt Test Circuit

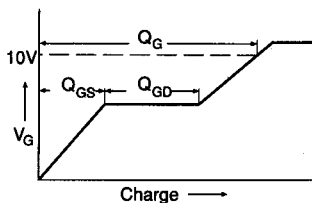


Fig. 14a—Basic Gate Charge Waveform

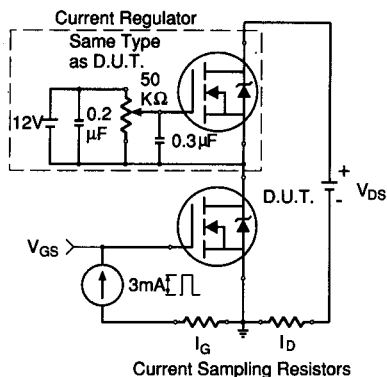


Fig. 14b—Gate Charge Test Circuit

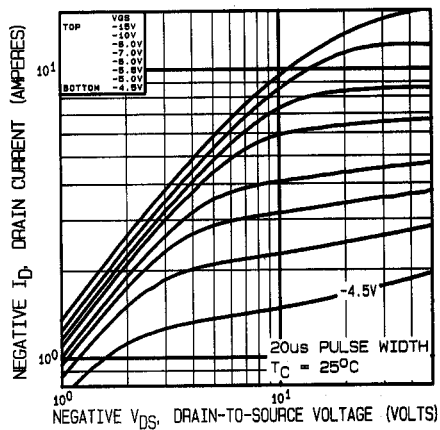
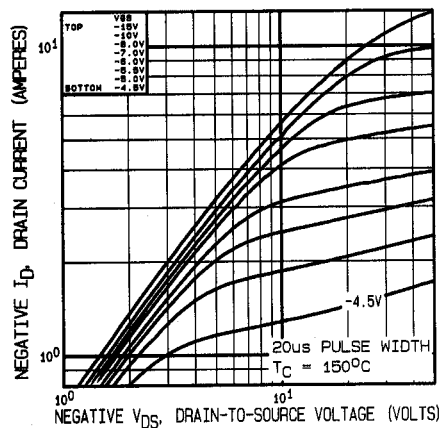
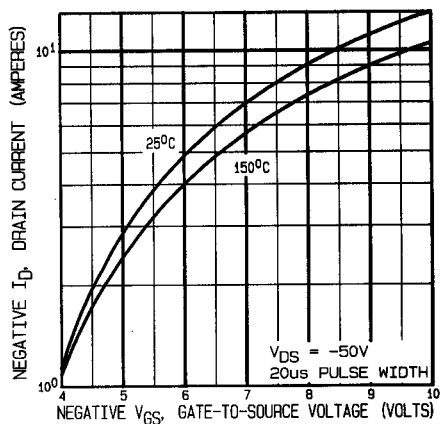
Fig. 15 — Typical Output Characteristics,
 $T_C = 25^\circ\text{C}$ Fig. 16 — Typical Output Characteristics,
 $T_C = 150^\circ\text{C}$ 

Fig. 17 — Typical Transfer Characteristics

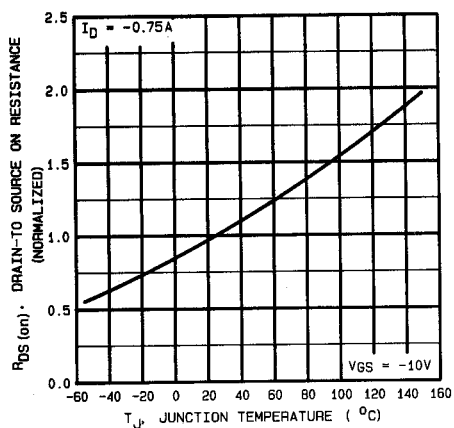


Fig. 18 — Normalized On-Resistance Vs. Temperature

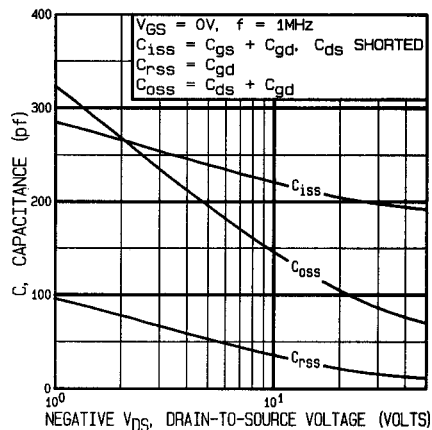


Fig. 19 — Typical Capacitance Vs. Drain-to-Source Voltage

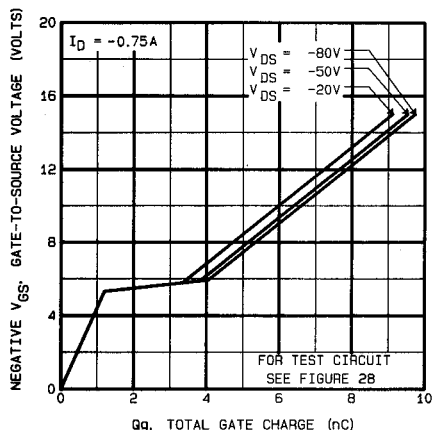


Fig. 20 — Typical Gate Charge Vs. Gate-to-Source Voltage

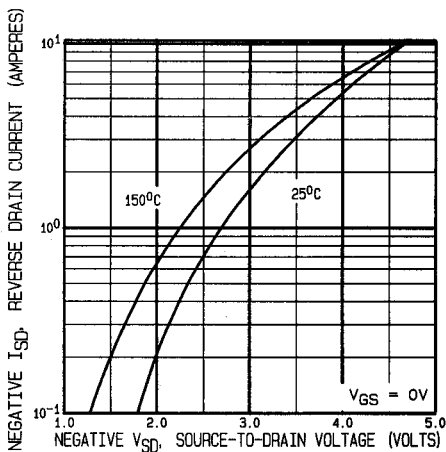


Fig. 21 — Typical Source-Drain Diode Forward Voltage

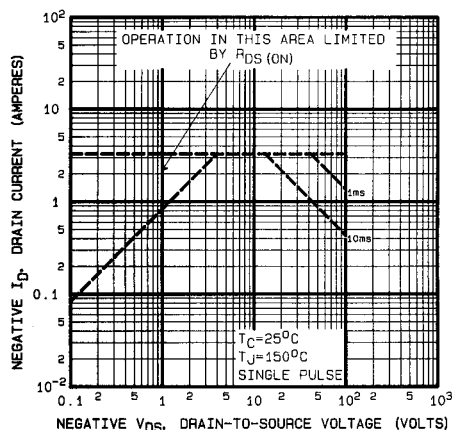


Fig. 22 — Maximum Safe Operating Area

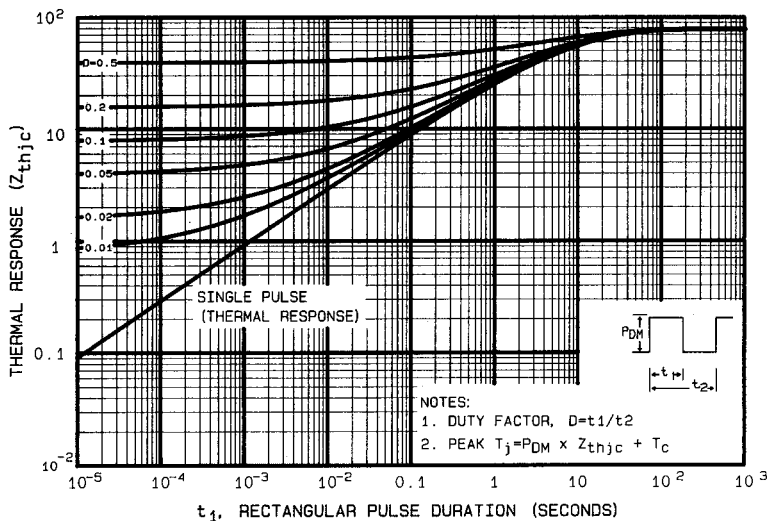


Fig. 23 — Maximum Effective Transient Thermal Impedance, Junction-to-Ambient Vs. Pulse Duration

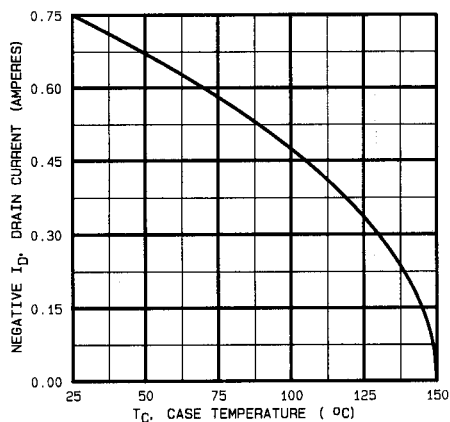


Fig. 24 — Maximum Drain Current Vs. Case Temperature

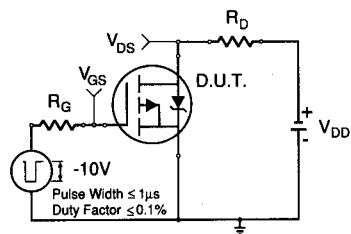


Fig. 25a — Switching Time Test Circuit

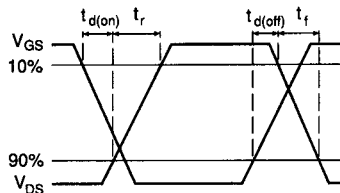


Fig. 25b — Switching Time Waveforms

P-Channel Q2, Q4

IRFG6110, JANTXV, JANTX-, 2N7336 Devices

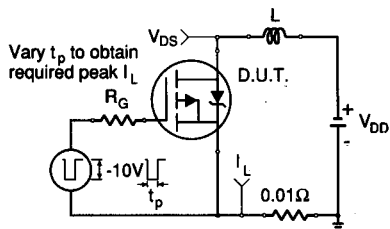


Fig. 26a — Unclamped Inductive Test Circuit

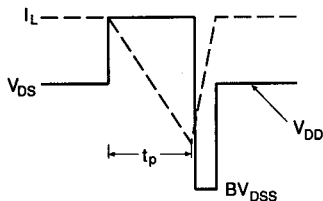


Fig. 26b — Unclamped inductive Waveforms

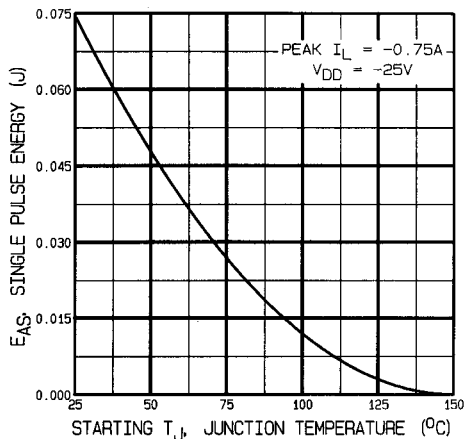


Fig. 26c — Maximum Avalanche Energy Vs. Starting Junction Temperature

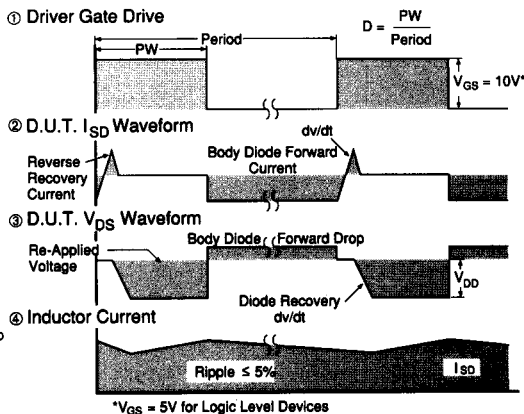
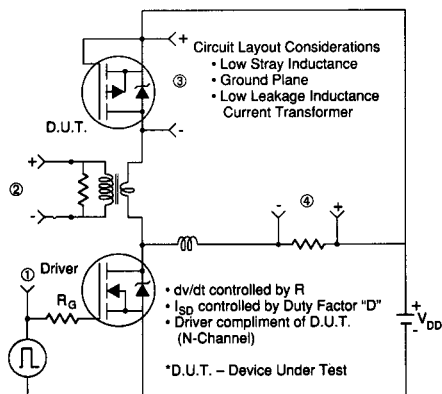


Fig. 27 — Peak Diode Recovery dv/dt Test Circuit

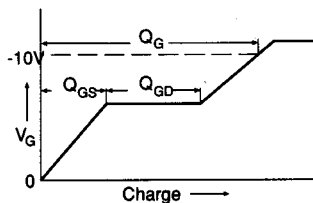


Fig. 28a — Basic Gate Charge Waveform

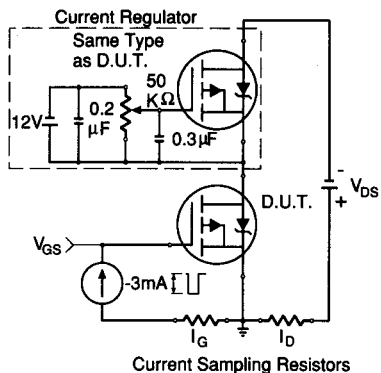


Fig. 28b — Gate Charge Test Circuit