Mar.22,2002 Ver.2
Under Development

SPDT SWITCH GaAs MMIC

■ GENERAL DESCRIPTION

NJG1600KB2 is a GaAs SPDT switch IC that features small-sized package and low insertion loss , and ideally suited for T/R switch of digital cordless telephone or other digital wireless systems.

This switch is operated in the wide frequency range from 100MHz to 2.5GHz at low operating voltage from +2.5V. The ultra small & ultra thin FLP6-B2 package is adopted.

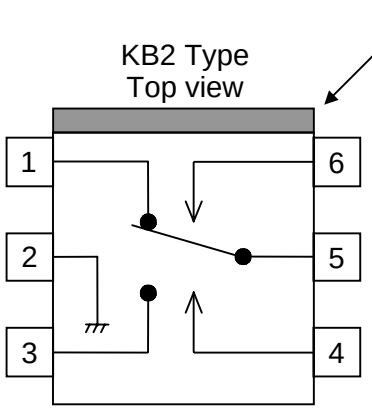
■ PACKAGE OUTLINE

NJG1600KB2

■ FEATURES

●Low control voltage	+2.7V typ.
●Low insertion loss	0.3dB typ. @f=1.0GHz 0.35dB typ. @f=2.0GHz 0.4dB typ. @f=2.5GHz
●High isolation	25dB typ. @f=1.0GHz 18dB typ. @f=2.0GHz 17dB typ. @f=2.5GHz
●Pin at 1dB compression point	27dBm typ. @f=2.5GHz
●Low control current	15uA typ.
●Ultra small & ultra thin package	FLP6-B2 (Package size: 2.1x2.0x0.75mm)

■ PIN CONFIGURATION



Pin connection

1.P1
2.GND
3.P2
4.VCTL2
5.PC
6.VCTL1

■ TRUTH TABLE

"H"=$V_{CTL\ (H)}$, "L"=$V_{CTL\ (L)}$

V_{CTL1}	H	L
V_{CTL2}	L	H
PC - P1	OFF	ON
PC - P2	ON	OFF

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITIONS	CONDITIONS	UNITS
RF Input Power	P_{IN}	V_{DD}=2.7V, V_{CTL}=0V/2.7V	27	dBm
Supply Voltage	V_{DD}	VDD terminal	7.5	V
Control Voltage	V_{CTL}	VCTL terminal	7.5	V
Operating Temp.	T_{opr}		-40~+85	°C
Storage Temp.	T_{stg}		-55~+150	°C

■ ELECTRICAL CHARACTERISTICS

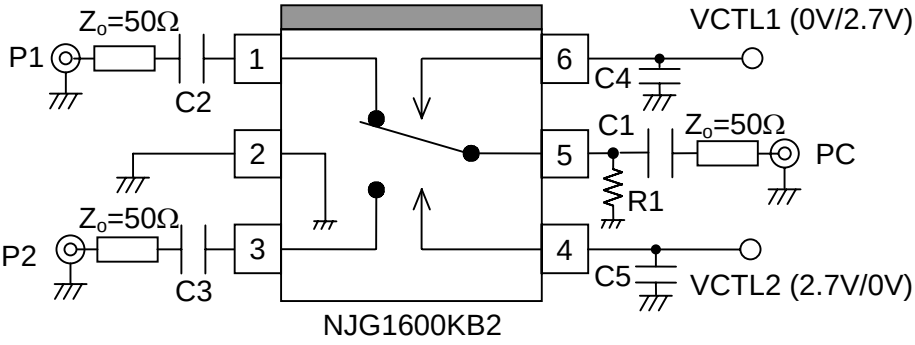
(General conditions: $V_{CTL\ (L)}$=0V, $V_{CTL\ (H)}$=2.7V, Z_S=Z_I=50Ω, T_a=25°C)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Current	I_{DD}	f=2.5GHz, P_{IN}=22dBm	-	120	-	uA
Control Voltage (LOW)	$V_{CTL\ (L)}$		0	-	0.8	V
Control Voltage (HIGH)	$V_{CTL\ (H)}$		2.0	2.7	V_{DD}	V
Control Current	I_{CTL}	f=2.5GHz, P_{IN}=22dBm	-	15	30	uA
Insertion Loss 1	LOSS1	f=1.0GHz, P_{IN}=22dBm	-	0.3	0.4	dB
Insertion Loss 2	LOSS2	f=2.0GHz, P_{IN}=22dBm	-	0.35	0.45	dB
Insertion Loss 3	LOSS3	f=2.5GHz, P_{IN}=22dBm	-	0.4	0.5	
Isolation 1	ISL1	f=1.0GHz, P_{IN}=22dBm	22	25	-	dB
Isolation 2	ISL2	f=2.0GHz, P_{IN}=22dBm	15	18	-	dB
Isolation 3	ISL2	f=2.5GHz, P_{IN}=22dBm	14	17	-	
Pin at 1dB Compression Point	P_{-1dB}	f=2.5GHz	24	27	-	dBm
VSWR	VSWR	f=0.1~2.5GHz, ON state	-	1.4	1.6	
Switching time	T_{SW}	f=0.1~2.5GHz	-	100	-	ns

■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
1	P1	RF port. This port is connected with PC port by controlling 4th pin ($V_{CTL(H)}$) to 2.5~6.5V and 6th pin($V_{CTL(L)}$) to -0.2~+0.2V. An external capacitor is required to block the DC bias voltage of internal circuit. (50~100MHz:0.01uF, 0.1~0.5GHz: 1000pF, 0.5~2.5GHz: 56pF)
2	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
3	P2	RF port. This port is connected with PC port by controlling 6th pin ($V_{CTL\ (H)}$) to 2.5~6.5V and 4th pin($V_{CTL(L)}$) to -0.2~+0.2V. An external capacitor is required to block the DC bias voltage of internal circuit. (50~100MHz:0.01uF, 0.1~0.5GHz: 1000pF, 0.5~2.5GHz: 56pF)
4	VCTL2	Control port 2. The voltage of this port controls PC to P1 state. The 'ON' and 'OFF' state is toggled by controlling voltage of this terminal such as high-state (2.5~6.5V) or low-state (-0.2~+0.2V). The voltage of 6th pin have to be set to opposite state. The bypass capacitor has to be chosen to reduce switching time delay from 10pF~1000pF range.
5	PC	Common RF port. In order to block the DC bias voltage of internal circuit, an external capacitor is required. (50~100MHz:0.01uF, 0.1~0.5GHz: 1000pF, 0.5~2.5GHz: 56pF)
6	VCTL1	Control port 1. The voltage of this port controls PC to P2 state. The 'ON' and 'OFF' state is toggled by controlling voltage of this terminal such as high-state (2.5~6.5V) or low-state (-0.2~+0.2V). The voltage of 4th pin have to be set to opposite state. The bypass capacitor has to be chosen to reduce switching time delay from 10pF~1000pF range.

■APPLICATION CIRCUIT

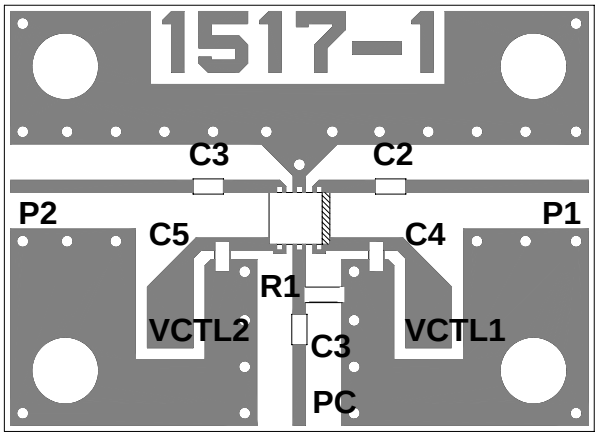


Parts List

Parts ID	Constant	Notes
C1~C3	56pF	GRM36 MURATA
C4, C5	10pF	GRM36 MURATA
R1	560KΩ	1608 Size

■RECOMMENDED PCB DESIGN

(TOP VIEW)



PCB SIZE=19.4x14.0mm
PCB: FR-4, t=0.2mm
CAPACITOR: size 1005
STRIPLINE WIDTH=0.4mm

PRECAUTIONS

[1] The DC blocking capacitors have to be placed at RF terminal of P1, P2 and PC.
[2] To reduce stlipline influence on RF characteristics, please locate bypass capacitors (C4, C5) close to each terminals.
[3] To avoid degradation of isolation or high power characteristics, please layout ground pattern right under this IC.

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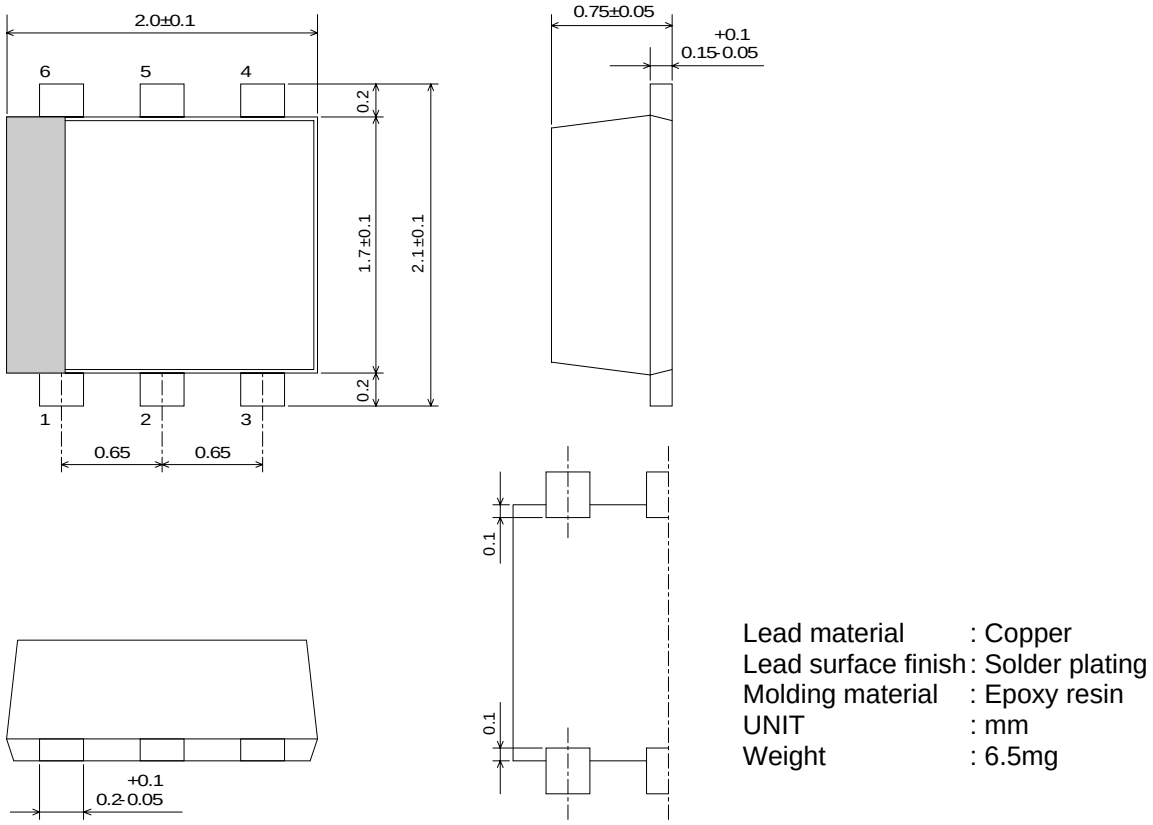
■PACKAGE OUTLINE (FLP6-B2)



Lead material : Copper
Lead surface finish : Solder plating
Molding material : Epoxy resin
UNIT : mm
Weight : 6.5mg

Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.