



1. General description

The 74HC40103 is an 8-bit synchronous down counter. It has control inputs for enabling or disabling the clock (CP), for clearing the counter to its maximum count and for presetting the counter either synchronously or asynchronously. In normal operation, the counter is decremented by one count on each positive-going transition of the clock (CP). Counting is inhibited when the terminal enable input (\overline{TE}) is HIGH. The terminal count output (\overline{TC}) goes LOW when the count reaches zero if \overline{TE} is LOW, and remains LOW for one full clock period. When the synchronous preset enable input (\overline{PE}) is LOW, data at the jam input (P0 to P7) is clocked into the counter on the next positive-going clock transition regardless of the state of \overline{TE} . When the asynchronous preset enable input (\overline{PL}) is LOW, data at the jam input (P0 to P7) is asynchronously forced into the counter regardless of the state of \overline{PE} , \overline{TE} , or CP. The jam inputs (P0 to P7) represent a single 8-bit binary word. When the master reset input (\overline{MR}) is LOW, the counter is asynchronously cleared to its maximum count (decimal 255) regardless of the state of any other input. If all control inputs except \overline{TE} are HIGH at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 256 clock pulses long. Device may be cascaded using the \overline{TE} input and the \overline{TC} output, in either a synchronous or ripple mode. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Cascadable
- Synchronous or asynchronous preset
- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low-power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standard no. 7A
- CMOS input levels
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +80 °C and from -40 °C to +125 °C

3. Applications

- Divide-by-n counters
- Programmable timers
- Interrupt timers
- Cycle/program counters.

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC40103D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC40103PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

5. Functional diagram

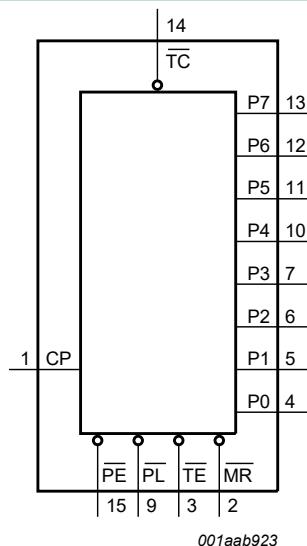


Fig. 1. Functional diagram

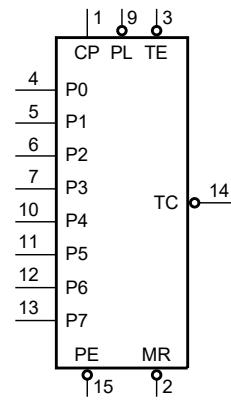


Fig. 2. Logic symbol

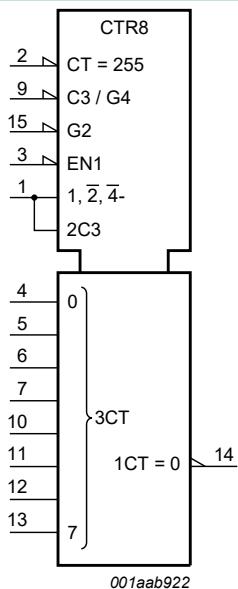


Fig. 3. IEC logic symbol

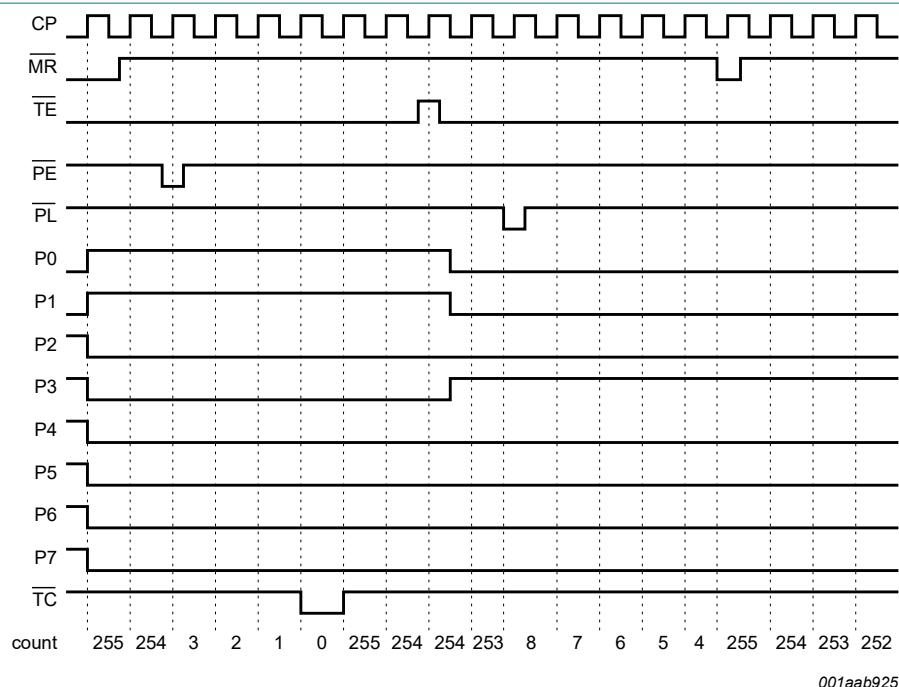
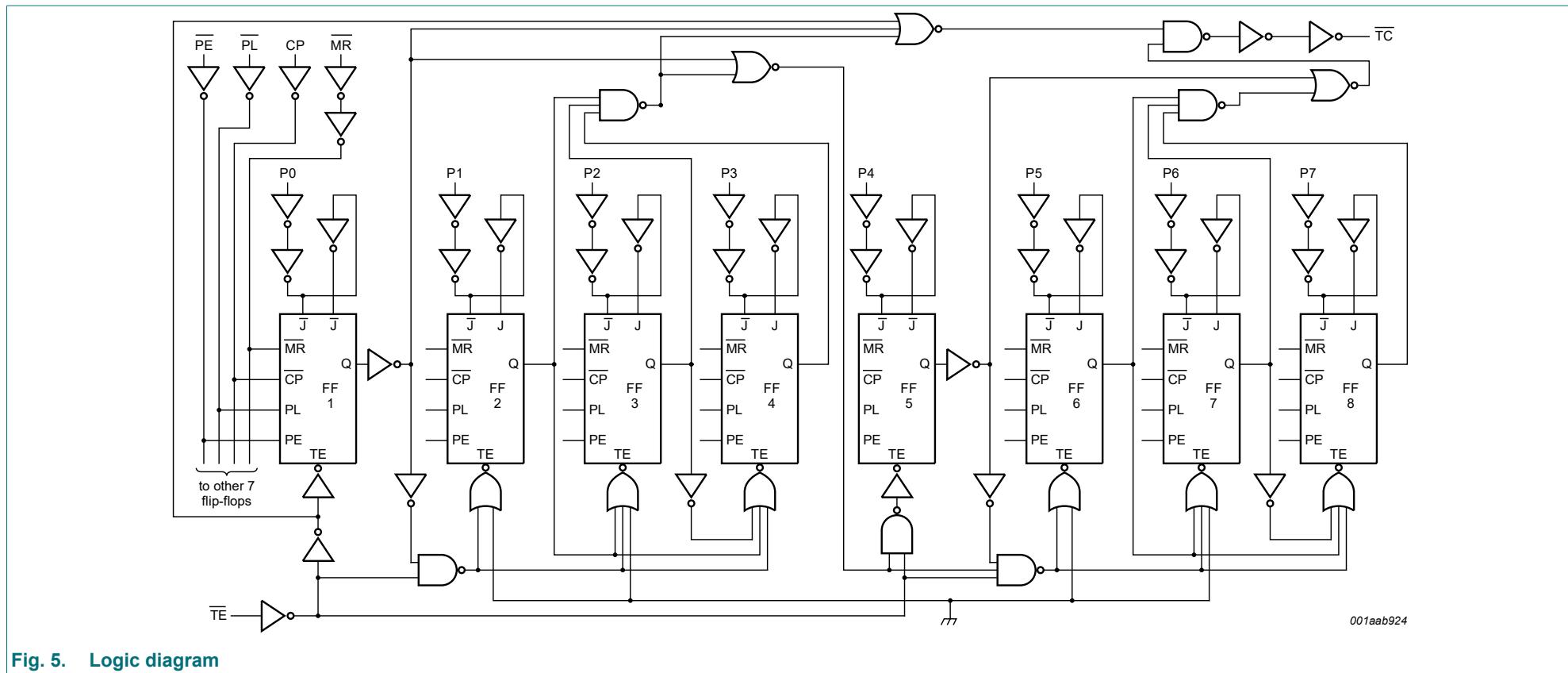
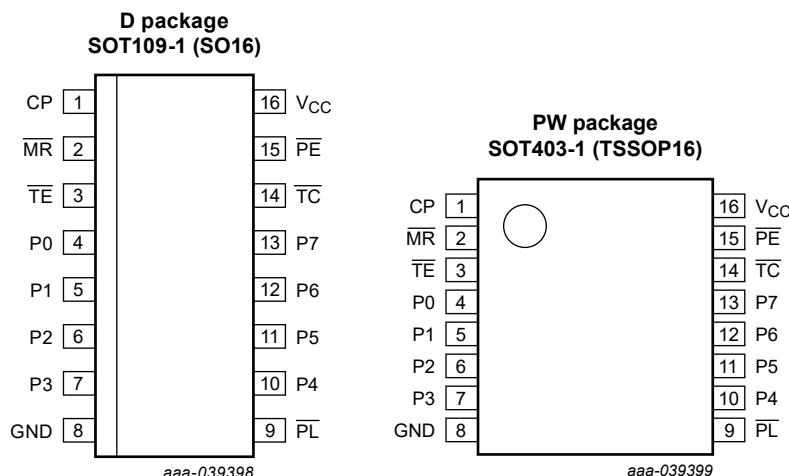


Fig. 4. Timing diagram



6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
CP	1	clock input (LOW-to-HIGH, edge-triggered)
MR	2	asynchronous master reset input (active LOW)
TE	3	terminal enable input (active LOW)
P0	4	jam input 0
P1	5	jam input 1
P2	6	jam input 2
P3	7	jam input 3
GND	8	ground (0 V)
PL	9	asynchronous preset enable input (active LOW)
P4	10	jam input 4
P5	11	jam input 5
P6	12	jam input 6
P7	13	jam input 7
TC	14	terminal count output (active LOW)
PE	15	synchronous preset enable input (active LOW)
V _{CC}	16	positive supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Control inputs				Preset mode	Action [1]
MR	PL	PE	TE		
L	X	X	X	asynchronous	clear to maximum count
H	L	X	X	asynchronous	preset asynchronously
	H	L	X	synchronous	preset on next LOW-to-HIGH clock transition
		H	L	synchronous	count down
		H		synchronous	inhibit counter

[1] Clock connected to CP.

Synchronous operation: changes occur on the LOW-to-HIGH CP transition.

Jam inputs: MSD = P7, LSD = P0.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	[1]	-	±20 mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	[1]	-	±20 mA
I _O	output current	V _O = -0.5 V to V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	+50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation		[2]	-	500 mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.

For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		2.0	5.0	6.0	V
V _I	input voltage		0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	V
Δt/ΔV	input transition rise and fall rates	V _{CC} = 2.0 V	-	-	625	ns
		V _{CC} = 4.5 V	-	1.67	139	ns
		V _{CC} = 6.0 V	-	-	83	ns
T _{amb}	ambient temperature		-40	-	+125	°C

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25^\circ\text{C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 2.0\text{ V}$	1.9	2.0	-	V
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	4.4	4.5	-	V
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 6.0\text{ V}$	5.9	6.0	-	V
		$I_O = -4\text{ mA}; V_{CC} = 4.5\text{ V}$	3.98	4.32	-	V
		$I_O = -5.2\text{ mA}; V_{CC} = 6.0\text{ V}$	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 2.0\text{ V}$	-	0	0.1	V
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	-	0	0.1	V
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 6.0\text{ V}$	-	0	0.1	V
		$I_O = 4\text{ mA}; V_{CC} = 4.5\text{ V}$	-	0.15	0.26	V
		$I_O = 5.2\text{ mA}; V_{CC} = 6.0\text{ V}$	-	0.16	0.26	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0\text{ V}$	-	-	± 0.1	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$; $V_{CC} = 6.0\text{ V}$	-	-	8.0	μA
C_I	input capacitance		-	3.5	-	pF
$T_{amb} = -40^\circ\text{C}$ to $+85^\circ\text{C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	-	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	-	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 2.0\text{ V}$	1.9	-	-	V
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	4.4	-	-	V
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 6.0\text{ V}$	5.9	-	-	V
		$I_O = -4\text{ mA}; V_{CC} = 4.5\text{ V}$	3.84	-	-	V
		$I_O = -5.2\text{ mA}; V_{CC} = 6.0\text{ V}$	5.34	-	-	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μ A; V _{CC} = 2.0 V	-	-	0.1	V
		I _O = 20 μ A; V _{CC} = 4.5 V	-	-	0.1	V
		I _O = 20 μ A; V _{CC} = 6.0 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	-	0.33	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	-	0.33	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	\pm 1.0	μ A
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	80	μ A
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	V
		V _{CC} = 4.5 V	3.15	-	-	V
		V _{CC} = 6.0 V	4.2	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	V
		V _{CC} = 4.5 V	-	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μ A; V _{CC} = 2.0 V	1.9	-	-	V
		I _O = -20 μ A; V _{CC} = 4.5 V	4.4	-	-	V
		I _O = -20 μ A; V _{CC} = 6.0 V	5.9	-	-	V
		I _O = -4 mA; V _{CC} = 4.5 V	3.7	-	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.2	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μ A; V _{CC} = 2.0 V	-	-	0.1	V
		I _O = 20 μ A; V _{CC} = 4.5 V	-	-	0.1	V
		I _O = 20 μ A; V _{CC} = 6.0 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	\pm 1.0	μ A
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	160	μ A

11. Dynamic characteristics

Table 7. Dynamic characteristics

$GND = 0 \text{ V}$; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$; for test circuit see [Fig. 12](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$						
t_{pd}	propagation delay	CP to $\overline{\text{TC}}$; see Fig. 6 [1]				
		$V_{\text{CC}} = 2.0 \text{ V}$	-	96	300	ns
		$V_{\text{CC}} = 4.5 \text{ V}$	-	35	60	ns
		$V_{\text{CC}} = 6.0 \text{ V}$	-	28	51	ns
		$V_{\text{CC}} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	30	-	ns
		$\overline{\text{TE}}$ to $\overline{\text{TC}}$; see Fig. 7				
		$V_{\text{CC}} = 2.0 \text{ V}$	-	50	175	ns
		$V_{\text{CC}} = 4.5 \text{ V}$	-	18	35	ns
		$V_{\text{CC}} = 6.0 \text{ V}$	-	14	30	ns
		PL to $\overline{\text{TC}}$; see Fig. 8				
		$V_{\text{CC}} = 2.0 \text{ V}$	-	102	315	ns
		$V_{\text{CC}} = 4.5 \text{ V}$	-	37	63	ns
		$V_{\text{CC}} = 6.0 \text{ V}$	-	30	53	ns
		$\overline{\text{MR}}$ to $\overline{\text{TC}}$; see Fig. 8				
		$V_{\text{CC}} = 2.0 \text{ V}$	-	83	275	ns
		$V_{\text{CC}} = 4.5 \text{ V}$	-	30	55	ns
		$V_{\text{CC}} = 6.0 \text{ V}$	-	24	47	ns
t_{PHL}	HIGH to LOW propagation delay	see Fig. 7 [2]				
		$V_{\text{CC}} = 2.0 \text{ V}$	-	19	75	ns
		$V_{\text{CC}} = 4.5 \text{ V}$	-	7	15	ns
		$V_{\text{CC}} = 6.0 \text{ V}$	-	6	13	ns
		t_{t}				
t_{W}	pulse width	CP HIGH or LOW; see Fig. 6				
		$V_{\text{CC}} = 2.0 \text{ V}$	165	22	-	ns
		$V_{\text{CC}} = 4.5 \text{ V}$	33	8	-	ns
		$V_{\text{CC}} = 6.0 \text{ V}$	28	6	-	ns
		$\overline{\text{MR}}$ LOW; see Fig. 8				
		$V_{\text{CC}} = 2.0 \text{ V}$	125	39	-	ns
		$V_{\text{CC}} = 4.5 \text{ V}$	25	14	-	ns
		$V_{\text{CC}} = 6.0 \text{ V}$	21	11	-	ns
		PL LOW; see Fig. 8				
		$V_{\text{CC}} = 2.0 \text{ V}$	125	33	-	ns
		$V_{\text{CC}} = 4.5 \text{ V}$	25	12	-	ns
		$V_{\text{CC}} = 6.0 \text{ V}$	21	10	-	ns
		t_{rec}				
		$\overline{\text{MR}}$ to CP, PL to CP; see Fig. 9				
		$V_{\text{CC}} = 2.0 \text{ V}$	50	14	-	ns
		$V_{\text{CC}} = 4.5 \text{ V}$	10	5	-	ns
		$V_{\text{CC}} = 6.0 \text{ V}$	9	4	-	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
t_{su}	set-up time	$\bar{P}E$ to CP; see Fig. 10					
		$V_{CC} = 2.0 \text{ V}$	75	22	-	ns	
		$V_{CC} = 4.5 \text{ V}$	15	8	-	ns	
		$V_{CC} = 6.0 \text{ V}$	13	6	-	ns	
		$\bar{T}E$ to CP; see Fig. 11					
		$V_{CC} = 2.0 \text{ V}$	150	44	-	ns	
		$V_{CC} = 4.5 \text{ V}$	30	16	-	ns	
		$V_{CC} = 6.0 \text{ V}$	26	13	-	ns	
		Pn to CP; see Fig. 10					
		$V_{CC} = 2.0 \text{ V}$	75	22	-	ns	
		$V_{CC} = 4.5 \text{ V}$	15	8	-	ns	
		$V_{CC} = 6.0 \text{ V}$	13	6	-	ns	
		$\bar{P}E$ to CP; see Fig. 10					
		$V_{CC} = 2.0 \text{ V}$	0	-14	-	ns	
		$V_{CC} = 4.5 \text{ V}$	0	-5	-	ns	
t_h	hold time	$V_{CC} = 6.0 \text{ V}$	0	-4	-	ns	
		$\bar{T}E$ to CP; see Fig. 11					
		$V_{CC} = 2.0 \text{ V}$	0	-30	-	ns	
		$V_{CC} = 4.5 \text{ V}$	0	-11	-	ns	
		$V_{CC} = 6.0 \text{ V}$	0	-9	-	ns	
		Pn to CP; see Fig. 10					
		$V_{CC} = 2.0 \text{ V}$	0	-17	-	ns	
		$V_{CC} = 4.5 \text{ V}$	0	-6	-	ns	
		$V_{CC} = 6.0 \text{ V}$	0	-5	-	ns	
		see Fig. 6					
		$V_{CC} = 2.0 \text{ V}$	3.0	10	-	MHz	
		$V_{CC} = 4.5 \text{ V}$	15	29	-	MHz	
		$V_{CC} = 6.0 \text{ V}$	18	35	-	MHz	
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	32	-	MHz	
C_{PD}	power dissipation capacitance	$V_I = \text{GND}$ to V_{CC}	[3]	-	24	-	pF
$T_{amb} = -40 \text{ }^{\circ}\text{C}$ to $+85 \text{ }^{\circ}\text{C}$							
t_{pd}	propagation delay	CP to $\bar{T}C$; see Fig. 6	[1]				
		$V_{CC} = 2.0 \text{ V}$	-	-	375	ns	
		$V_{CC} = 4.5 \text{ V}$	-	-	75	ns	
		$V_{CC} = 6.0 \text{ V}$	-	-	64	ns	
		$\bar{T}E$ to $\bar{T}C$; see Fig. 7					
		$V_{CC} = 2.0 \text{ V}$	-	-	220	ns	
		$V_{CC} = 4.5 \text{ V}$	-	-	44	ns	
		$V_{CC} = 6.0 \text{ V}$	-	-	37	ns	
		$\bar{P}L$ to $\bar{T}C$; see Fig. 8					
		$V_{CC} = 2.0 \text{ V}$	-	-	395	ns	
		$V_{CC} = 4.5 \text{ V}$	-	-	79	ns	
		$V_{CC} = 6.0 \text{ V}$	-	-	40	ns	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	\overline{MR} to \overline{TC} ; see Fig. 8				
		$V_{CC} = 2.0 \text{ V}$	-	-	345	ns
		$V_{CC} = 4.5 \text{ V}$	-	-	69	ns
		$V_{CC} = 6.0 \text{ V}$	-	-	59	ns
t_t	transition time	see Fig. 7 [2]				
		$V_{CC} = 2.0 \text{ V}$	-	-	95	ns
		$V_{CC} = 4.5 \text{ V}$	-	-	19	ns
		$V_{CC} = 6.0 \text{ V}$	-	-	16	ns
t_w	pulse width	CP HIGH or LOW; see Fig. 6				
		$V_{CC} = 2.0 \text{ V}$	205	-	-	ns
		$V_{CC} = 4.5 \text{ V}$	41	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	35	-	-	ns
		\overline{MR} LOW; see Fig. 8				
		$V_{CC} = 2.0 \text{ V}$	155	-	-	ns
		$V_{CC} = 4.5 \text{ V}$	31	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	26	-	-	ns
		\overline{PL} LOW; see Fig. 8				
		$V_{CC} = 2.0 \text{ V}$	155	-	-	ns
		$V_{CC} = 4.5 \text{ V}$	31	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	26	-	-	ns
		\overline{MR} to CP, \overline{PL} to CP; see Fig. 9				
		$V_{CC} = 2.0 \text{ V}$	65	-	-	ns
		$V_{CC} = 4.5 \text{ V}$	13	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	11	-	-	ns
t_{su}	set-up time	\overline{PE} to CP; see Fig. 10				
		$V_{CC} = 2.0 \text{ V}$	95	-	-	ns
		$V_{CC} = 4.5 \text{ V}$	19	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	16	-	-	ns
		\overline{TE} to CP; see Fig. 11				
		$V_{CC} = 2.0 \text{ V}$	190	-	-	ns
		$V_{CC} = 4.5 \text{ V}$	38	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	33	-	-	ns
		P_n to CP; see Fig. 10				
		$V_{CC} = 2.0 \text{ V}$	95	-	-	ns
		$V_{CC} = 4.5 \text{ V}$	19	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	16	-	-	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_h	hold time	\overline{PE} to CP; see Fig. 10				
		$V_{CC} = 2.0 \text{ V}$	0	-	-	ns
		$V_{CC} = 4.5 \text{ V}$	0	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	0	-	-	ns
		\overline{TE} to CP; see Fig. 11				
		$V_{CC} = 2.0 \text{ V}$	0	-	-	ns
		$V_{CC} = 4.5 \text{ V}$	0	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	0	-	-	ns
		\overline{Pn} to CP; see Fig. 10				
		$V_{CC} = 2.0 \text{ V}$	0	-	-	ns
		$V_{CC} = 4.5 \text{ V}$	0	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	0	-	-	ns
f_{max}	maximum frequency	see Fig. 6				
		$V_{CC} = 2.0 \text{ V}$	2.4	-	-	MHz
		$V_{CC} = 4.5 \text{ V}$	12	-	-	MHz
		$V_{CC} = 6.0 \text{ V}$	14	-	-	MHz
$T_{amb} = -40 \text{ }^{\circ}\text{C} \text{ to } +125 \text{ }^{\circ}\text{C}$						
t_{pd}	propagation delay	CP to \overline{TC} ; see Fig. 6	[1]			
		$V_{CC} = 2.0 \text{ V}$	-	-	450	ns
		$V_{CC} = 4.5 \text{ V}$	-	-	90	ns
		$V_{CC} = 6.0 \text{ V}$	-	-	77	ns
		\overline{TE} to \overline{TC} ; see Fig. 7				
		$V_{CC} = 2.0 \text{ V}$	-	-	265	ns
		$V_{CC} = 4.5 \text{ V}$	-	-	53	ns
		$V_{CC} = 6.0 \text{ V}$	-	-	45	ns
		\overline{PL} to \overline{TC} ; see Fig. 8				
		$V_{CC} = 2.0 \text{ V}$	-	-	475	ns
		$V_{CC} = 4.5 \text{ V}$	-	-	95	ns
		$V_{CC} = 6.0 \text{ V}$	-	-	81	ns
t_{PHL}	HIGH to LOW propagation delay	\overline{MR} to \overline{TC} ; see Fig. 8				
		$V_{CC} = 2.0 \text{ V}$	-	-	415	ns
		$V_{CC} = 4.5 \text{ V}$	-	-	83	ns
		$V_{CC} = 6.0 \text{ V}$	-	-	71	ns
t_t	transition time	see Fig. 7	[2]			
		$V_{CC} = 2.0 \text{ V}$	-	-	110	ns
		$V_{CC} = 4.5 \text{ V}$	-	-	22	ns
		$V_{CC} = 6.0 \text{ V}$	-	-	19	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_W	pulse width	CP HIGH or LOW; see Fig. 6				
		$V_{CC} = 2.0 \text{ V}$	250	-	-	ns
		$V_{CC} = 4.5 \text{ V}$	50	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	43	-	-	ns
		\bar{MR} LOW; see Fig. 8				
		$V_{CC} = 2.0 \text{ V}$	190	-	-	ns
		$V_{CC} = 4.5 \text{ V}$	38	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	32	-	-	ns
		\bar{PL} LOW; see Fig. 8				
		$V_{CC} = 2.0 \text{ V}$	190	-	-	ns
		$V_{CC} = 4.5 \text{ V}$	38	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	32	-	-	ns
t_{rec}	recovery time	\bar{MR} to CP, \bar{PL} to CP; see Fig. 9				
		$V_{CC} = 2.0 \text{ V}$	75	-	-	ns
		$V_{CC} = 4.5 \text{ V}$	15	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	13	-	-	ns
t_{su}	set-up time	\bar{PE} to CP; see Fig. 10				
		$V_{CC} = 2.0 \text{ V}$	110	-	-	ns
		$V_{CC} = 4.5 \text{ V}$	22	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	19	-	-	ns
		\bar{TE} to CP; see Fig. 11				
		$V_{CC} = 2.0 \text{ V}$	225	-	-	ns
		$V_{CC} = 4.5 \text{ V}$	45	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	38	-	-	ns
		Pn to CP; see Fig. 10				
		$V_{CC} = 2.0 \text{ V}$	110	-	-	ns
		$V_{CC} = 4.5 \text{ V}$	22	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	19	-	-	ns
t_h	hold time	\bar{PE} to CP; see Fig. 10				
		$V_{CC} = 2.0 \text{ V}$	0	-	-	ns
		$V_{CC} = 4.5 \text{ V}$	0	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	0	-	-	ns
		\bar{TE} to CP; see Fig. 11				
		$V_{CC} = 2.0 \text{ V}$	0	-	-	ns
		$V_{CC} = 4.5 \text{ V}$	0	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	0	-	-	ns
		Pn to CP; see Fig. 10				
		$V_{CC} = 2.0 \text{ V}$	0	-	-	ns
		$V_{CC} = 4.5 \text{ V}$	0	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	0	-	-	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{\max}	maximum frequency	see Fig. 6				
		$V_{CC} = 2.0 \text{ V}$	2.0	-	-	MHz
		$V_{CC} = 4.5 \text{ V}$	10	-	-	MHz
		$V_{CC} = 6.0 \text{ V}$	12	-	-	MHz

- [1] t_{pd} is the same as t_{PHL} , t_{PLH} .
 [2] t_i is the same as t_{THL} , t_{TLH} .
 [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11.1. Waveforms and test circuit

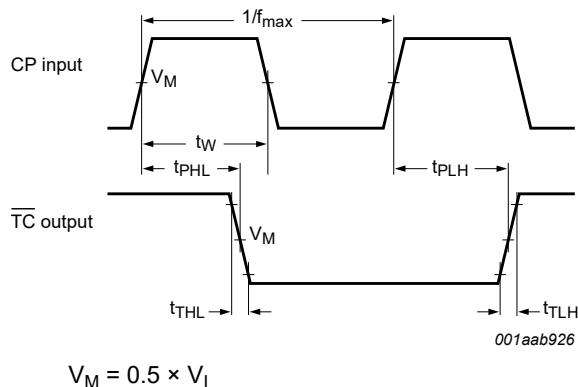


Fig. 6. Clock input (CP) to \overline{TC} propagation delays, clock pulse width, output transition times and the maximum clock pulse frequency

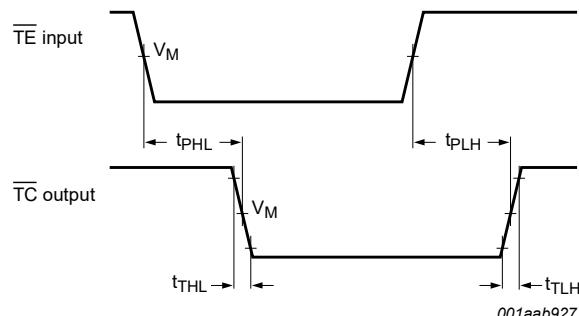


Fig. 7. TE to \overline{TC} propagation delays

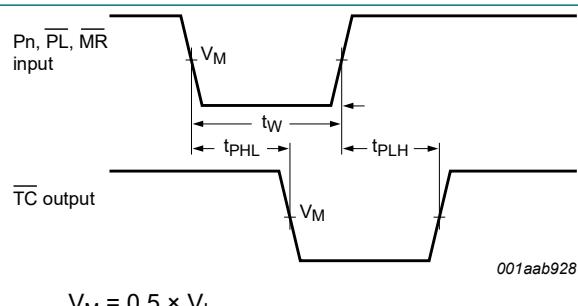


Fig. 8. PL, MR, Pn to \overline{TC} propagation delays

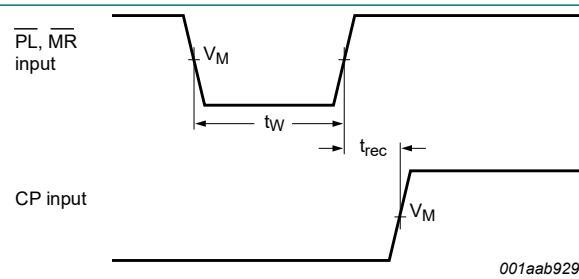
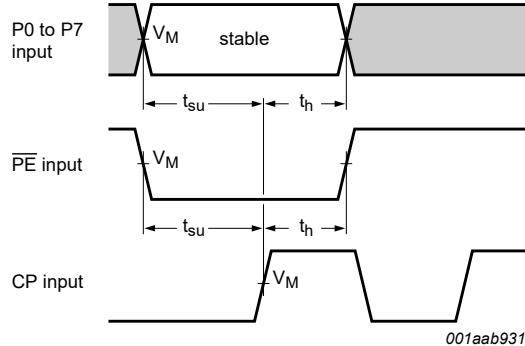


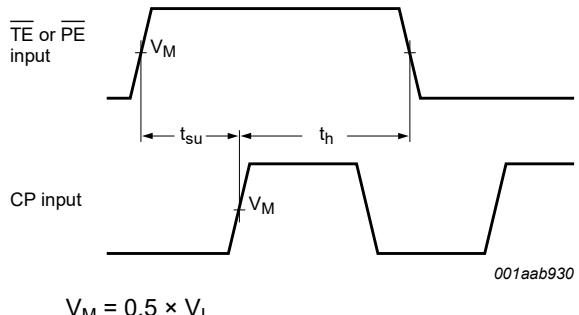
Fig. 9. Removal time for MR and PL



The shaded areas indicate when the input is permitted to change for predictable output performance.

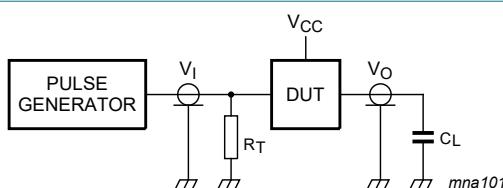
$$V_M = 0.5 \times V_I$$

Fig. 10. Hold and set-up times for P_n , \overline{PE} to CP



$$V_M = 0.5 \times V_I$$

Fig. 11. Hold and set-up times for \overline{MR} or \overline{PE} to CP



Test data is given in [Table 8](#).

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance.

Fig. 12. Test circuit for measuring switching times

Table 8. Test data

Supply	Input		Load
V_{CC}	V_I	t_r, t_f	C_L
2.0 V	V_{CC}	6 ns	50 pF
4.5 V	V_{CC}	6 ns	50 pF
6.0 V	V_{CC}	6 ns	50 pF
5.0 V	V_{CC}	6 ns	15 pF

12. Application information

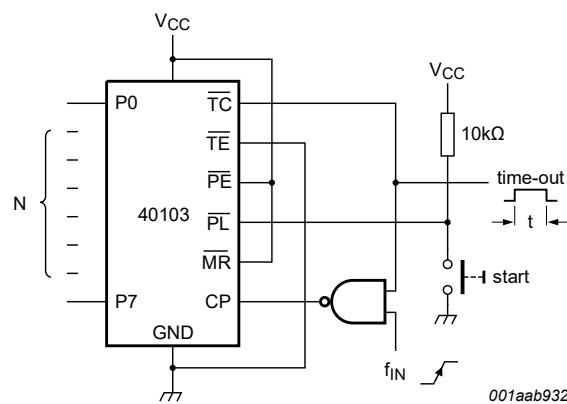


Fig. 13. Programmable timer

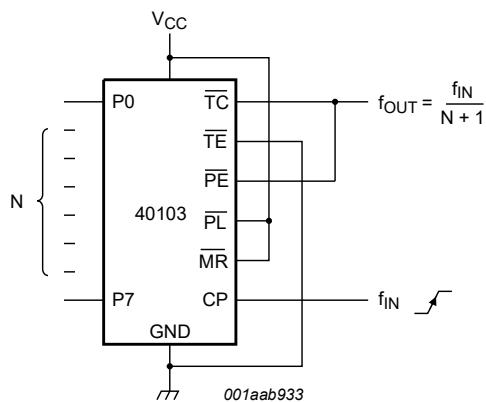


Fig. 14. Divide-by-N counter

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

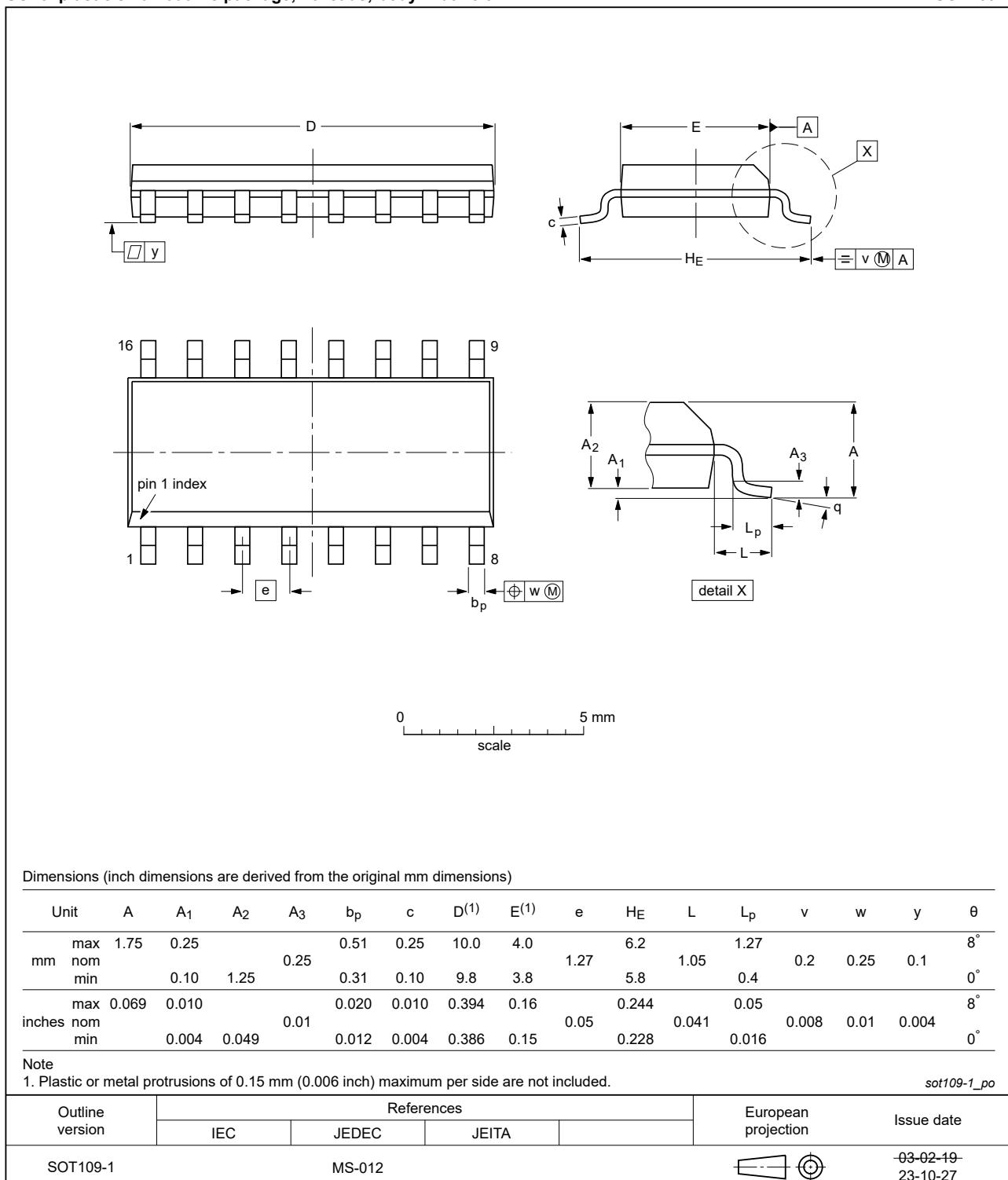


Fig. 15. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

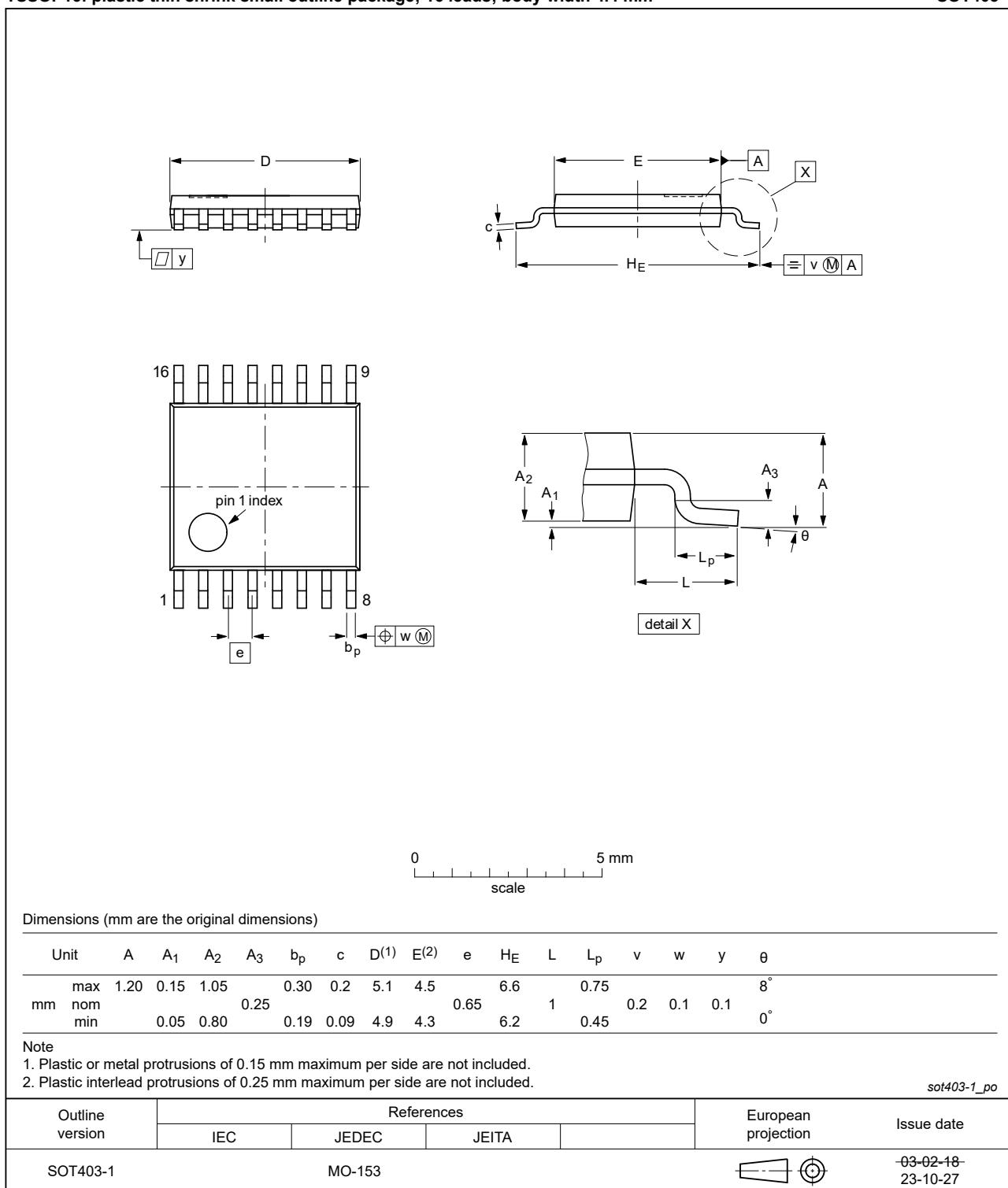


Fig. 16. Package outline SOT403-1 (TSSOP16)

14. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC40103 v.6	20240326	Product data sheet	-	74HC40103 v.5
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 2: ESD specification updated according to the latest JEDEC standard. Table 4: Derating values for P_{tot} total power dissipation updated. Fig. 15, Fig. 16: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153 			
74HC40103 v.5	20160421	Product data sheet	-	74HC40103 v.4
Modifications:	<ul style="list-style-type: none"> Type number 74HC40103DB (SOT338-1) removed. 			
74HC40103 v.4	20160127	Product data sheet	-	74HC40103 v.3
Modifications:	<ul style="list-style-type: none"> Type number 74HC40103N (SOT38-4) removed. 			
74HC40103 v.3	20041112	Product data sheet	-	74HC_HCT40103_CNV v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors. Removed type number 74HCT40103. Inserted family specification. 			
74HC_HCT40103_CNV v.2	19970918	Product specification	-	74HC_HCT40103 v.1
74HC_HCT40103 v.1	19901201	Product specification	-	-

16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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