

Quad, High-Speed HDMI/DVI 2:1 Digital Video Switch

General Description

The MAX4886 high-speed analog switch is ideal for HDMI/DVI switching applications, permitting 2:1 or 1:2 switching. The MAX4886 contains four differential pairs of 1:2 or 2:1 switches for RGB and clocking signals. The MAX4886 connects either one monitor to one of two digital video signals, or one HDMI/DVI source to one of two loads (sink).

The MAX4886 set of differential switches is based on an nFET architecture with internal charge pump for gate overdrive. This advanced architecture results in an extremely low capacitance and on-resistance needed for the excellent return loss requirements for digital switching. An efficient internal charge-pump design offers very low quiescent current for power-sensitive notebook designs.

The MAX4886 features 8Ω (typ) on-resistance and 2.5pF on-capacitance switches for routing RGB and CLK video signals. The MAX4886 is a high-frequency companion device to the MAX4929. These two devices combined perform the full 2:1 HDMI/DVI switching function.

The MAX4886 is available in a space-saving, 42-pin, 3.5mm x 9.0mm TQFN package and operates over the extended -40°C to +85°C temperature range.

Applications

HDTV Monitors/Receivers
Video Projectors
Notebook Computers
Digital HDTV Switch Boxes/Tuners
Multimedia Audio/Video Switchers
Servers/Routers with DVI Interfaces
Digital Video Recorders
LVDS Switching
1000 Base-BX, Switching

Pin Configuration appears at end of data sheet.

Features

- ◆ Single +3.0V to +3.6V Power Supply
- ◆ Low On-Resistance (R_{ON}): 8Ω (typ)
- ◆ Low On-Capacitance (C_{ON}): 2.5pF (typ)
- ◆ Low Skew: 20ps (typ)
- ◆ 700μA Low Supply Current
- ◆ 2.6GHz (typ) Ultra-High Bandwidth
- ◆ 0.6dB (typ) Ultra-Low Insertion Loss
- ◆ High-Frequency Companion Device to MAX4929
- ◆ Use MAX4886 and MAX4929 to Form a Complete HDMI/DVI 2:1 Switch
- ◆ 42-Pin, 3.5mm x 9.0mm, Space-Saving TQFN

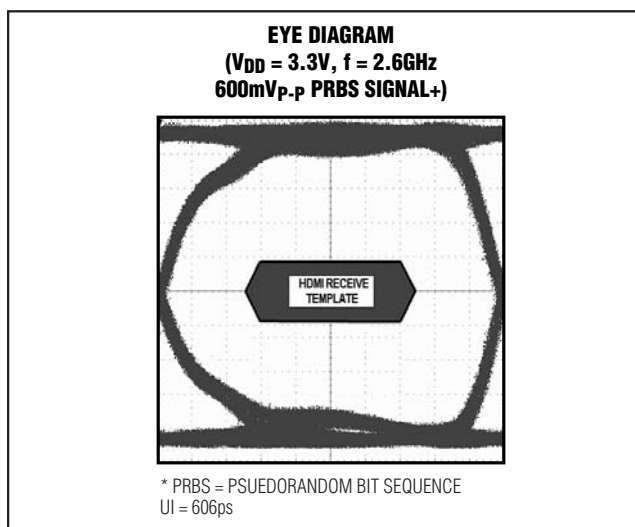
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX4886ETO+	-40°C to +85°C	42 TQFN-EP*	T42359OM-1

+ Denotes a lead-free package.

*EP = Exposed paddle.

Eye Diagram



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ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)

V _{DD}	-0.3V to +4V
SEL (Note 1)	-0.3V to (V _{DD} + 0.3V)
COM ₋ , NC ₋ , NO ₋	-0.3V to (V _{DD} + 0.3V)
Continuous Current Through Any Switch	±120mA
Peak Current Through Any Switches (Pulsed at 1ms, 10% duty cycle)	±240mA

Continuous Power Dissipation (T_A = +70°C)

42-Pin Thin QFN-EP (derate 35.7mW/°C above +70°C)	2857.1mW
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

Note 1: Signal exceeding V_{DD} or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +3.0V to +3.6V, T_A = T_{MIN} to T_{MAX}. Typical values are at V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V _{DD}		3.0		3.6	V
Quiescent Supply Current	I _{DD}	+3V ≤ V _{DD} ≤ +3.6V; SEL = 0V or V _{DD}		600	1100	μA
ANALOG SWITCH						
On-Resistance (Note 3)	R _{ON}	V _{DD} = +3V, 0V ≤ V _{COM₋} ≤ V _{DD} , I _{COM₋} = -40mA	T _A = +25°C		8	11
			T _A = T _{MIN} to T _{MAX}			15
		V _{DD} = +3V, I _{COM₋} = -40mA, 0 ≤ V _{COM₋} ≤ 1.5V	T _A = +25°C		8	11
			T _A = T _{MIN} to T _{MAX}			15
On-Resistance Matching (Notes 3, 4)	ΔR _{ON}	V _{DD} = +3V, 1.5V ≤ V _{COM₋} ≤ V _{DD} , I _{COM₋} = -40mA	T _A = +25°C		0.28	0.40
			T _A = T _{MIN} to T _{MAX}			0.8
		V _{DD} = +3V, 0 ≤ V _{COM₋} ≤ 1.5V, I _{COM₋} = -40mA	T _A = +25°C		0.28	0.40
			T _A = T _{MIN} to T _{MAX}			0.8
On-Resistance Flatness (Note 3)	R _{FLAT(ON)}	V _{DD} = +3V, I _{COM₋} = -40mA, 1.5V < V _{COM₋} < V _{DD}	T _A = +25°C		0.02	0.60
			T _A = T _{MIN} to T _{MAX}			1
		V _{DD} = +3V, I _{COM₋} = -40mA, 0 ≤ V _{COM₋} ≤ 1.5V	T _A = +25°C		0.02	0.60
			T _A = T _{MIN} to T _{MAX}			1
Leakage Current	I _L	V _{DD} = +3.6V, V _{COM₋} = +0.3V, +3.3V, V _{NC₋} or V _{NO₋} = +3.3V, 0.3V	-1		+1	μA
SWITCH DYNAMIC						
Off-Capacitance	C _{OFF}	f = 1MHz, V _{COM₋} = V _{NC₋} or V _{NO₋}		1.5		pF

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +3.0V$ to $+3.6V$, $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $V_{DD} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
On-Capacitance	CON	$f = 1MHz$, $V_{COM_} = V_{NC_}$ or $V_{NO_}$		2.5		pF
Propagation Delay	t_{PD1} , t_{PD2}	$R_S = R_L = 50\Omega$ (Figure 2)		100		ps
Output Skew Between Ports	t_{SKEW1}	Skew between any two ports, $R_S = R_L = 50\Omega$ (Figure 3)		20		ps
Skew Between Same Ports	t_{SKEW2}	$R_S = R_L = 50\Omega$, skew between any two ports (Figure 3)		20		ps
SWITCH AC PERFORMANCE						
On-Channel -3dB Bandwidth	BW	$R_S = R_L = 50\Omega$ (Figure 4)		2.6		GHz
Insertion Loss	I_{LOS}	$R_S = R_L = 50\Omega$, $f = 50MHz$ (Figure 4)		0.6		dB
Off-Isolation	V_{ISO}	$R_S = R_L = 50\Omega$, single-ended, $f = 50MHz$ (Figure 4)		-58		dB
Crosstalk	V_{CT1}	Crosstalk between any two switches, $R_S = R_L = 50\Omega$, $f = 50MHz$ (Figure 4)		-49		dB
LOGIC INPUTS (SEL)						
Input-Low Voltage	V_{IL}	$V_{DD} = +3.0V$			0.8	V
Input-High Voltage	V_{IH}	$V_{DD} = +3.6V$	2.0			V
Input-Voltage Hysteresis	V_{HYST}			100		mV
Input Leakage Current	I_{LEAK}	$V_{DD} = +3.6V$, $V_{COM_}$ or $V_{NC_}$ or $V_{NO_} = 0V$	-1		+1	μA

Note 2: Maximum and minimum limits over temperature are guaranteed by design and characterization. Device is production tested at $T_A = +25^\circ C$.

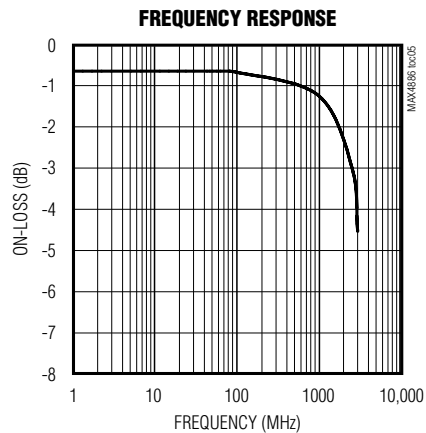
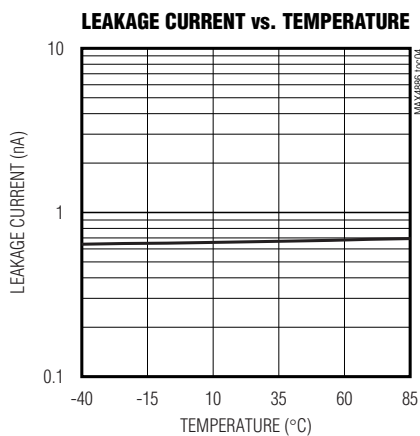
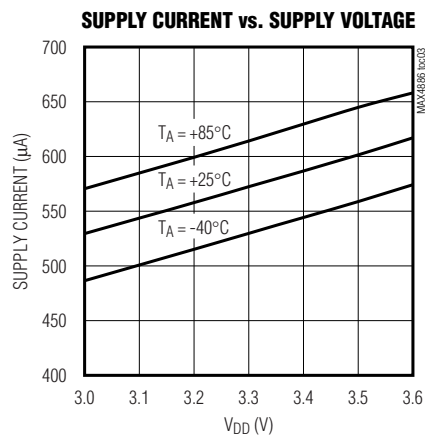
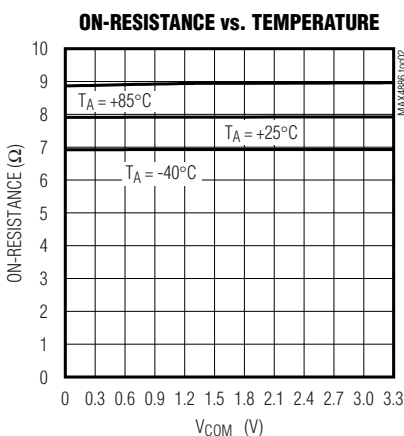
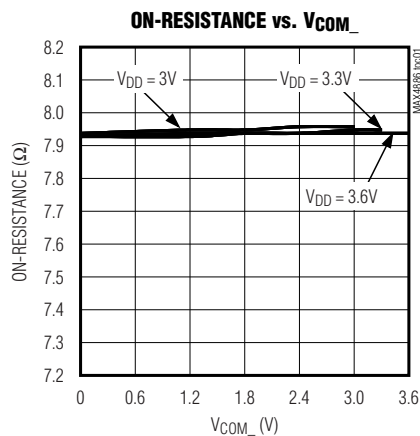
Note 3: Negative current is going into $COM_$ and out of $NO_$ or $NC_$.

Note 4: Guaranteed by design.

Quad, High-Speed HDMI/DVI 2:1 Digital Video Switch

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)



Quad, High-Speed HDMI/DVI 2:1 Digital Video Switch

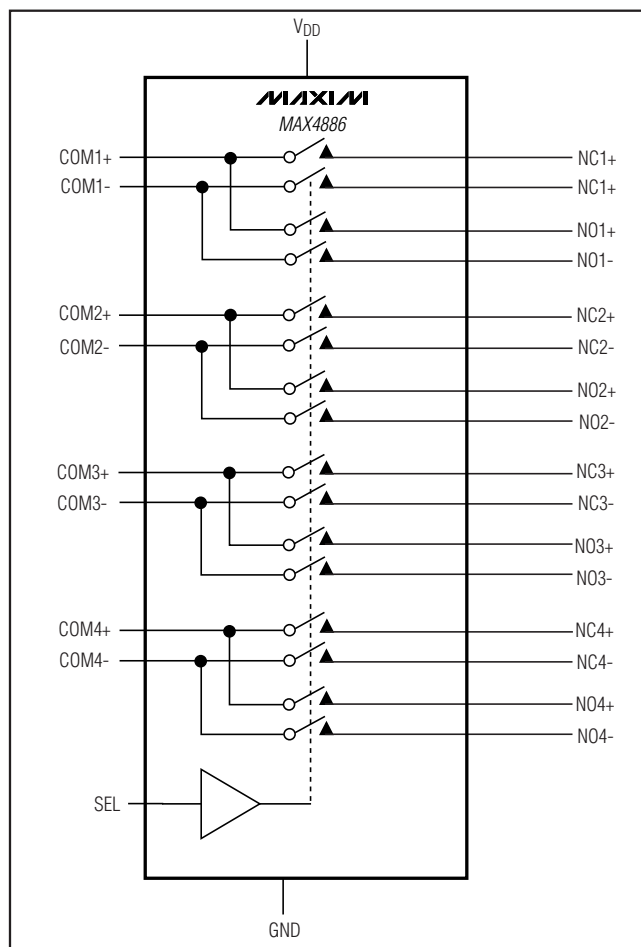
Pin Description

PIN	NAME	FUNCTION
1, 4, 10, 14, 17, 19, 21, 39, 41	GND	Ground
5, 8, 13, 18, 20, 30, 40, 42	V _{DD}	Power-Supply Voltage Input. Bypass V _{DD} to GND with a 0.1μF or larger ceramic capacitor.
2	COM1+	Data Signal Inputs/Outputs
3	COM1-	Data Signal Inputs/Outputs
6	COM2+	Data Signal Inputs/Outputs
7	COM2-	Data Signal Inputs/Outputs
9	SEL	Select Input. Logic input for switch connection (see Table 1).
11	COM3+	Data Signal Inputs/Outputs
12	COM3-	Data Signal Inputs/Outputs
15	COM4+	Data Signal Inputs/Outputs
16	COM4-	Data Signal Inputs/Outputs
22	NO4-	Differential Pair. Data Signal Inputs/Outputs.
23	NO4+	Differential Pair. Data Signal Inputs/Outputs.
24	NO3-	Differential Pair. Data Signal Inputs/Outputs.
25	NO3+	Differential Pair. Data Signal Inputs/Outputs.
26	NC4-	Differential Pair. Data Signal Inputs/Outputs.
27	NC4+	Differential Pair. Data Signal Inputs/Outputs.
28	NC3-	Differential Pair. Data Signal Inputs/Outputs.
29	NC3+	Differential Pair. Data Signal Inputs/Outputs.
31	NO2-	Differential Pair. Data Signal Inputs/Outputs.
32	NO2+	Differential Pair. Data Signal Inputs/Outputs.
33	NO1-	Differential Pair. Data Signal Inputs/Outputs.
34	NO1+	Differential Pair. Data Signal Inputs/Outputs.
35	NC2-	Differential Pair. Data Signal Inputs/Outputs.
36	NC2+	Differential Pair. Data Signal Inputs/Outputs.
37	NC1-	Differential Pair. Data Signal Inputs/Outputs.
38	NC1+	Differential Pair. Data Signal Inputs/Outputs.
EP	EP	Exposed Paddle. Connect EP to GND.

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Functional Diagram



Detailed Description

The MAX4886 high-speed analog switch is ideal for HDMI/DVI switching applications, permitting 2:1 or 1:2 switching. The MAX4886 contains four differential pairs for HDMI or DVI switching. The MAX4886 connects either one monitor to one of two digital video signals or one HDMI/DVI output to one of two connectors or loads.

The MAX4886 differential switches are based on an nFET architecture with an internal charge pump for gate overdrive. This advanced architecture results in an extremely low capacitance and on-resistance needed for an excellent returns loss.

The MAX4886 features an 8Ω (typ) on-resistance and 2.5pF on-capacitance switches for routing RGB and CLK video signals.

Table 1. Switch Truth Table

SEL	FUNCTION
0	COM_ to NC_
1	COM_ to NO_

The MAX4886 switches are identical, and any of the switches can be used to route RGB and CLK video signals.

The device will also be useful in other high-speed switching applications such as LVDS and LVPECL.

Analog-Signal Levels

Signal inputs over the full voltage range (0V to V_{DD}) are passed through the switch with minimal change in on-resistance (see the *Typical Operating Characteristics* section). The switches are bidirectional. Therefore, COM_, NC_, and NO_ can be either inputs or outputs.

Logic Inputs (SEL)

The MAX4886 has a logic input that controls the switch on/off function. Use SEL to switch COM_ to NO_ or COM_ to NC_. Table 1 and the *Functional Diagram* illustrate the MAX4886 Truth Table.

Applications Information

Power-Supply Bypassing and Sequencing

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence V_{DD} on first, followed by the switch inputs and the logic inputs. Bypass at least one V_{DD} input to ground with a 0.1 μ F capacitor as close to the device as possible. Use the smallest physical size possible for optimal performance.

It is also recommended to bypass more than one V_{DD} input. A good strategy is to bypass one V_{DD} input with a 0.1 μ F capacitor and at least a second V_{DD} input with a 1nF to 10nF capacitor. (Use 0603 or smaller physical size ceramic capacitor).

PC Board (PCB) Layout

High-speed switches such as the MAX4886 require proper PCB layout for optimum performance. Ensure that impedance-controlled PCB traces for high-speed signals are matched in length, and as short as possible. Connect the MAX4886 exposed paddle to a solid ground plane.

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Timing Circuits/Timing Diagrams

MAX4886

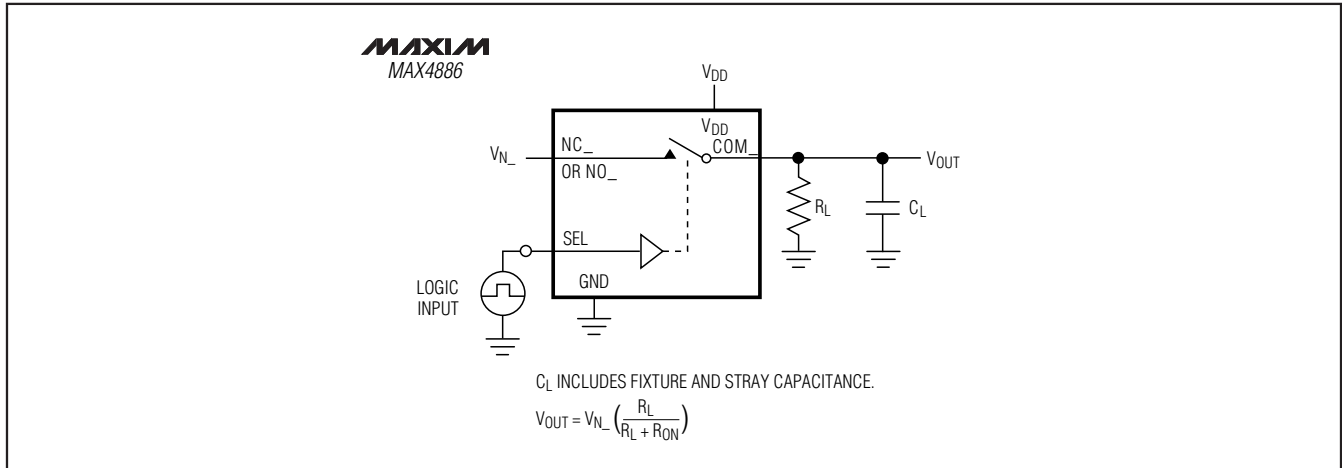


Figure 1. Switching Time

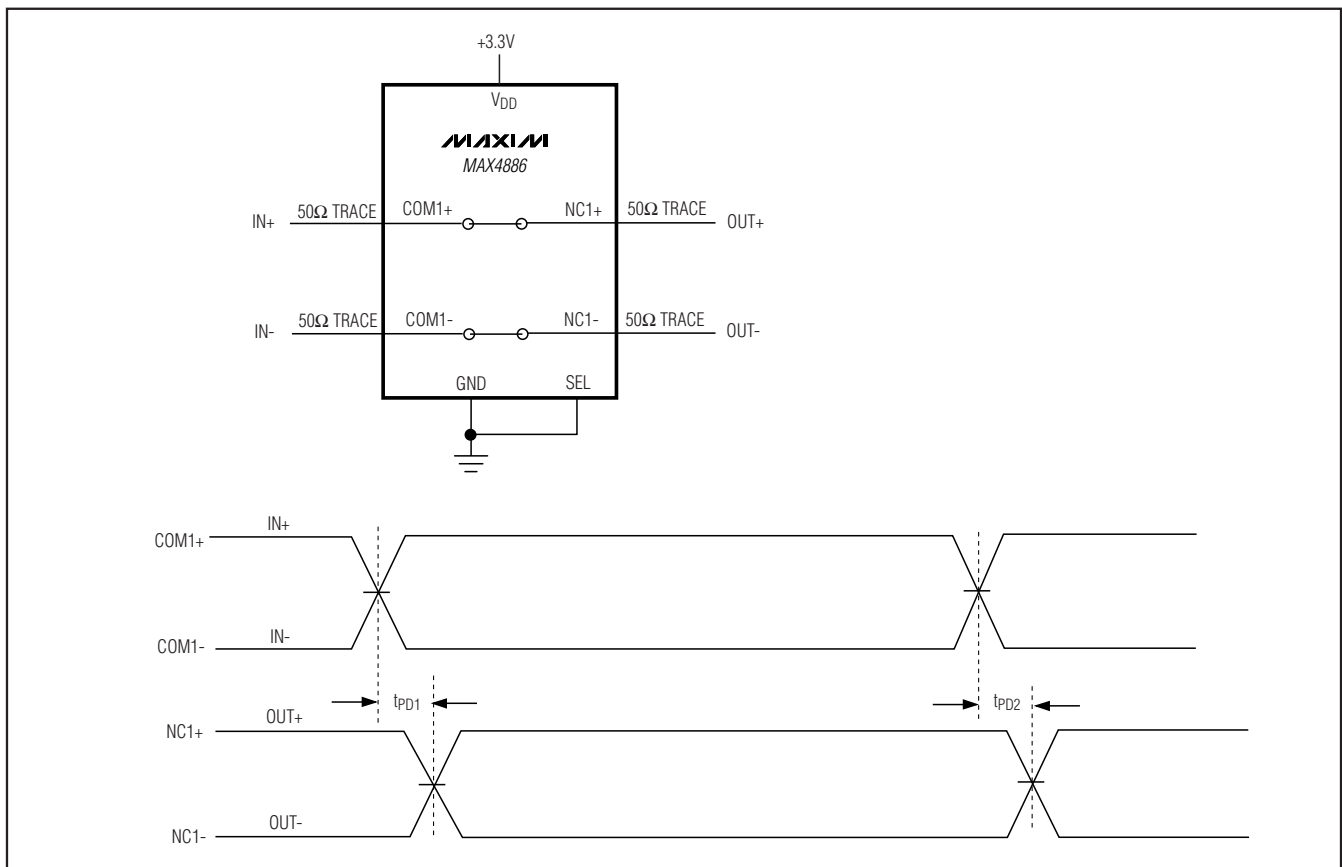


Figure 2. Propagation Delay

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Timing Circuits/Timing Diagrams (continued)

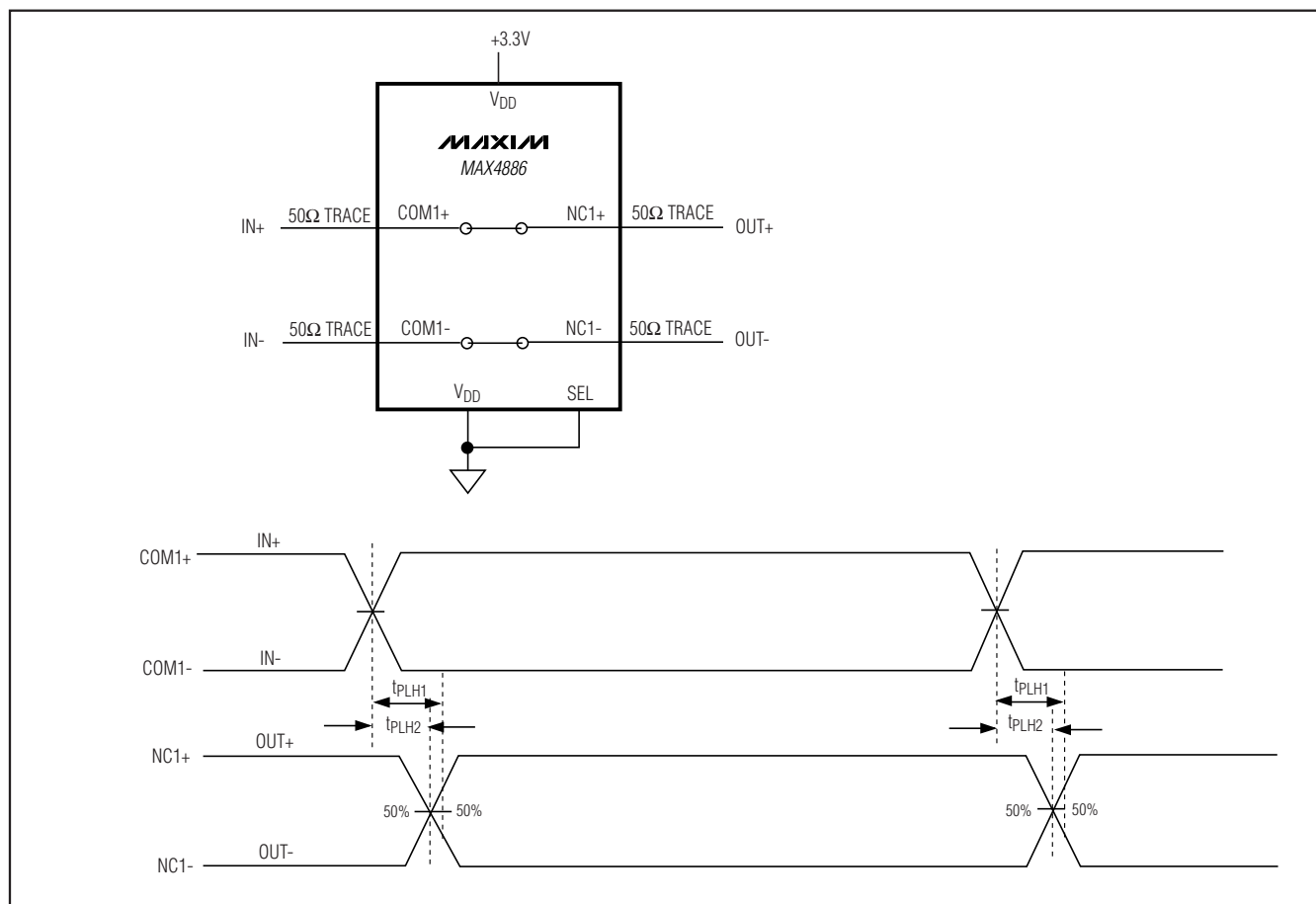


Figure 3. Skew Measurements

Additional Applications Information

In a typical application (see Figure 5), the MAX4886 and MAX4929 are used to route the TMDS signals and low-frequency signals between two HDMI inputs.

In another application (see Figure 6), the MAX4886 is used in a notebook to route high-frequency DVI port on the computer or to the connector on the docking station. The MAX4886 routes four differential signals (RGB and CLK) either to the DVI connector or to the docking station port. The switch is inherently bilateral and may be used as a 2:1 or 1:2 mux without penalties.

Chip Information

PROCESS: BiCMOS

Connect exposed paddle to GND.

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MAX4886

Timing Circuits/Timing Diagrams (continued)

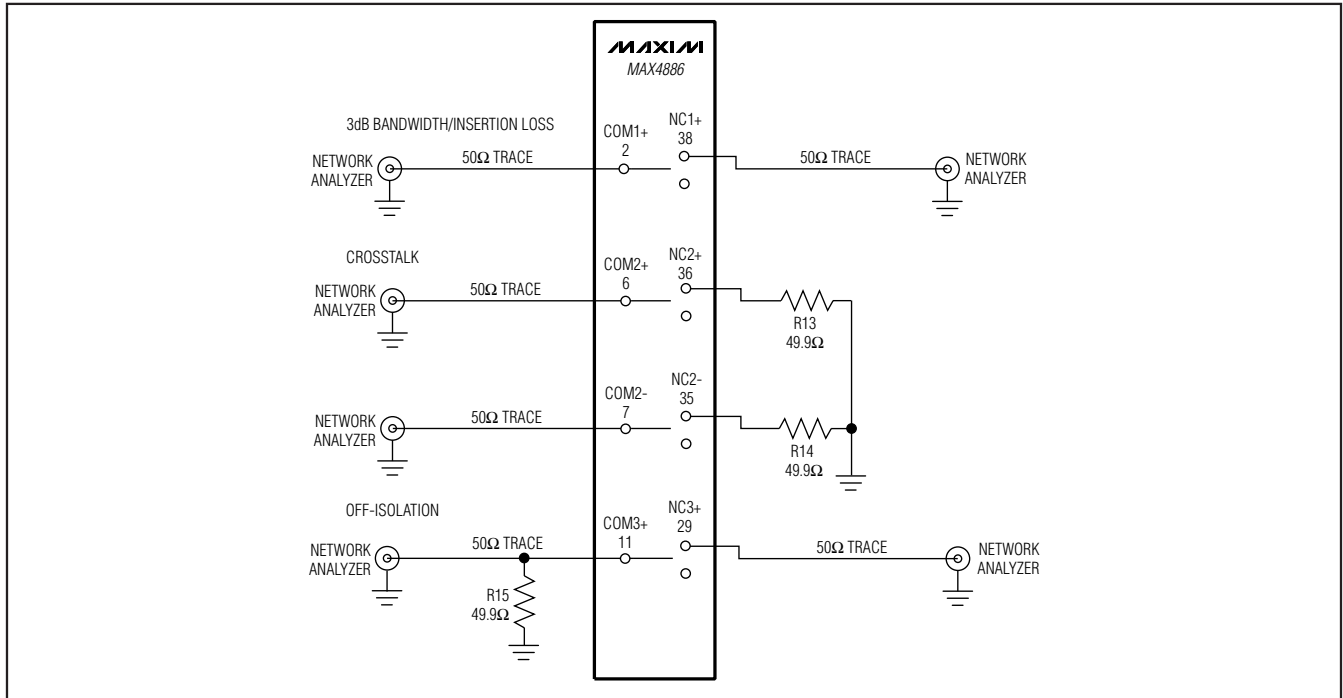


Figure 4. On-Loss, Off-Isolation, and Crosstalk

Typical Application Diagrams

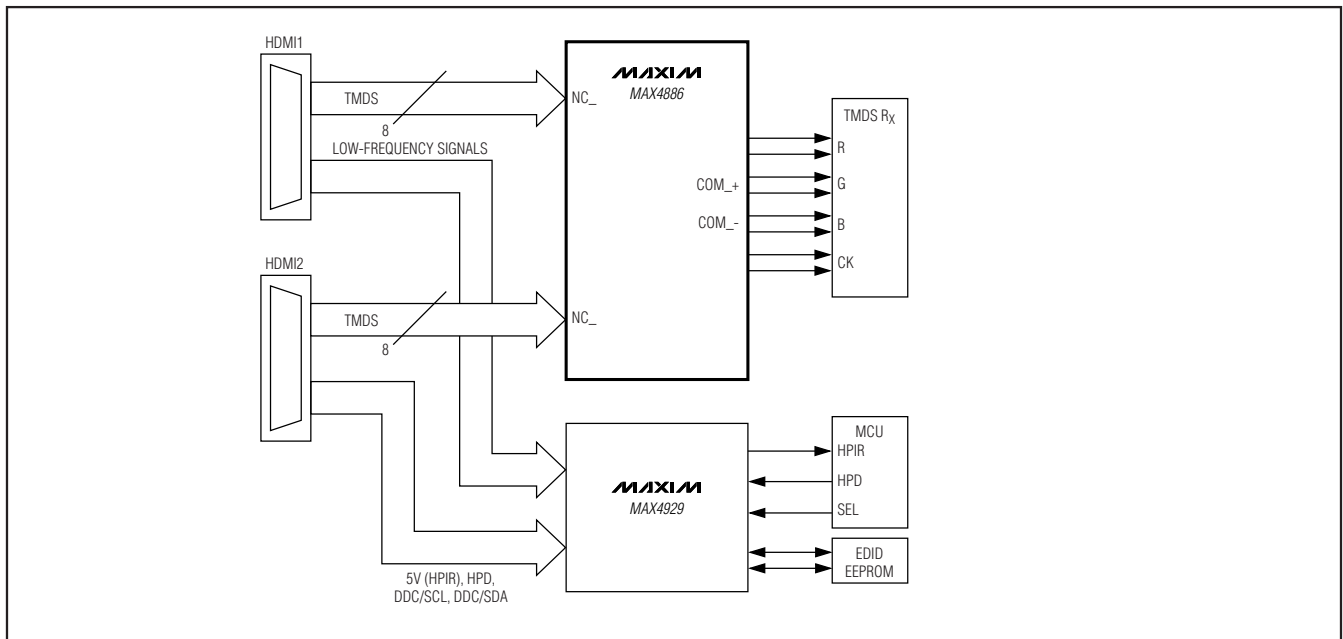


Figure 5. TV/Monitor Application

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Typical Application Diagrams (continued)

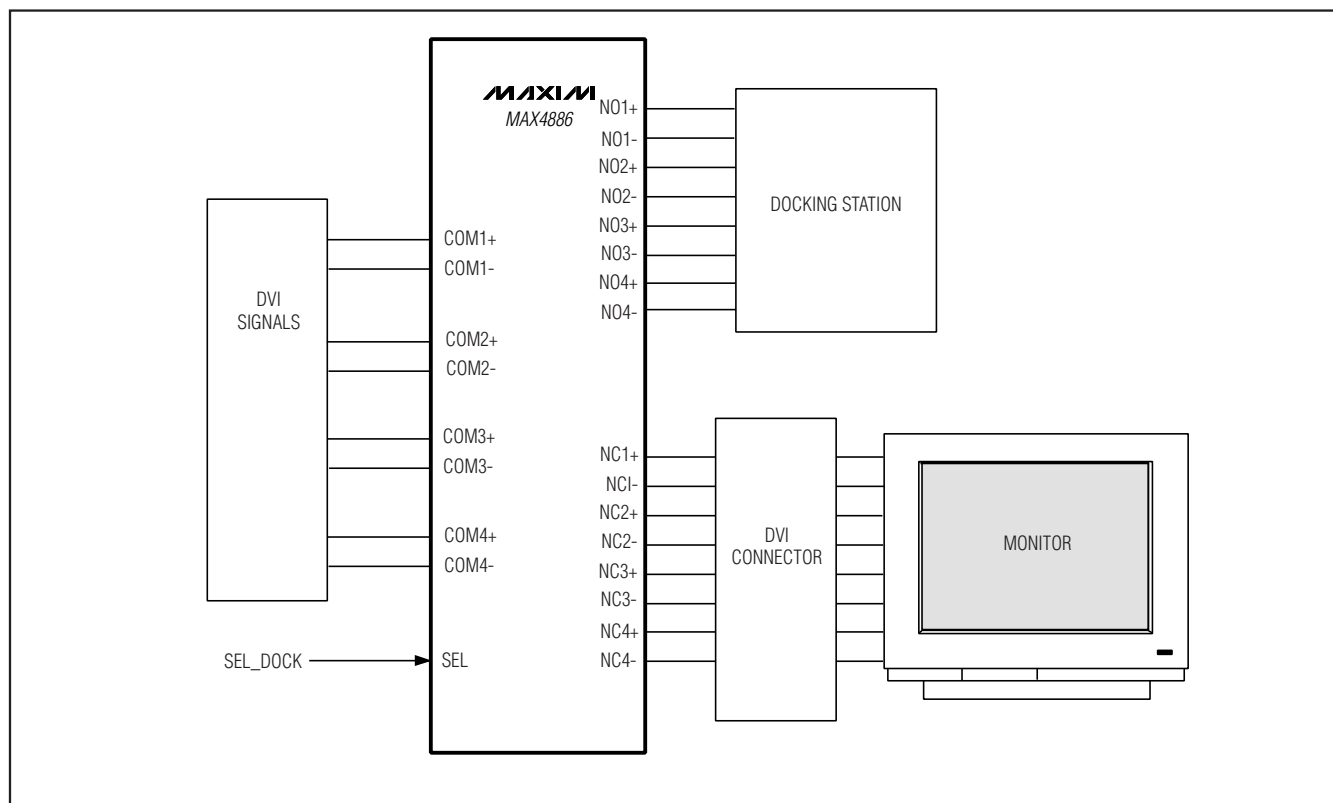
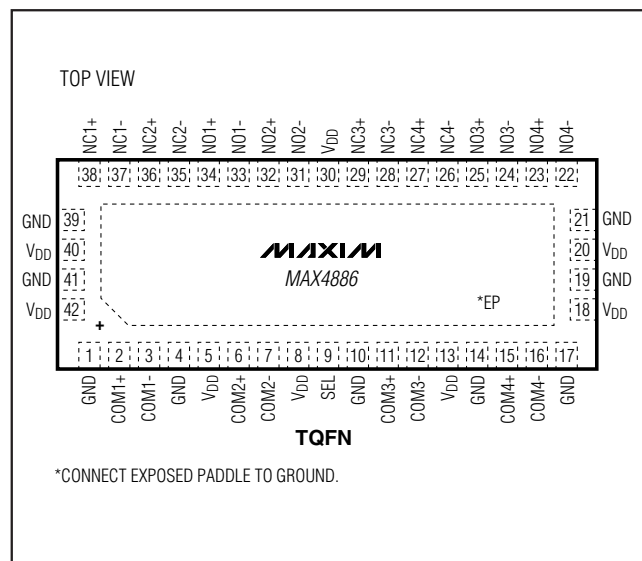


Figure 6. Notebook Application

Pin Configuration



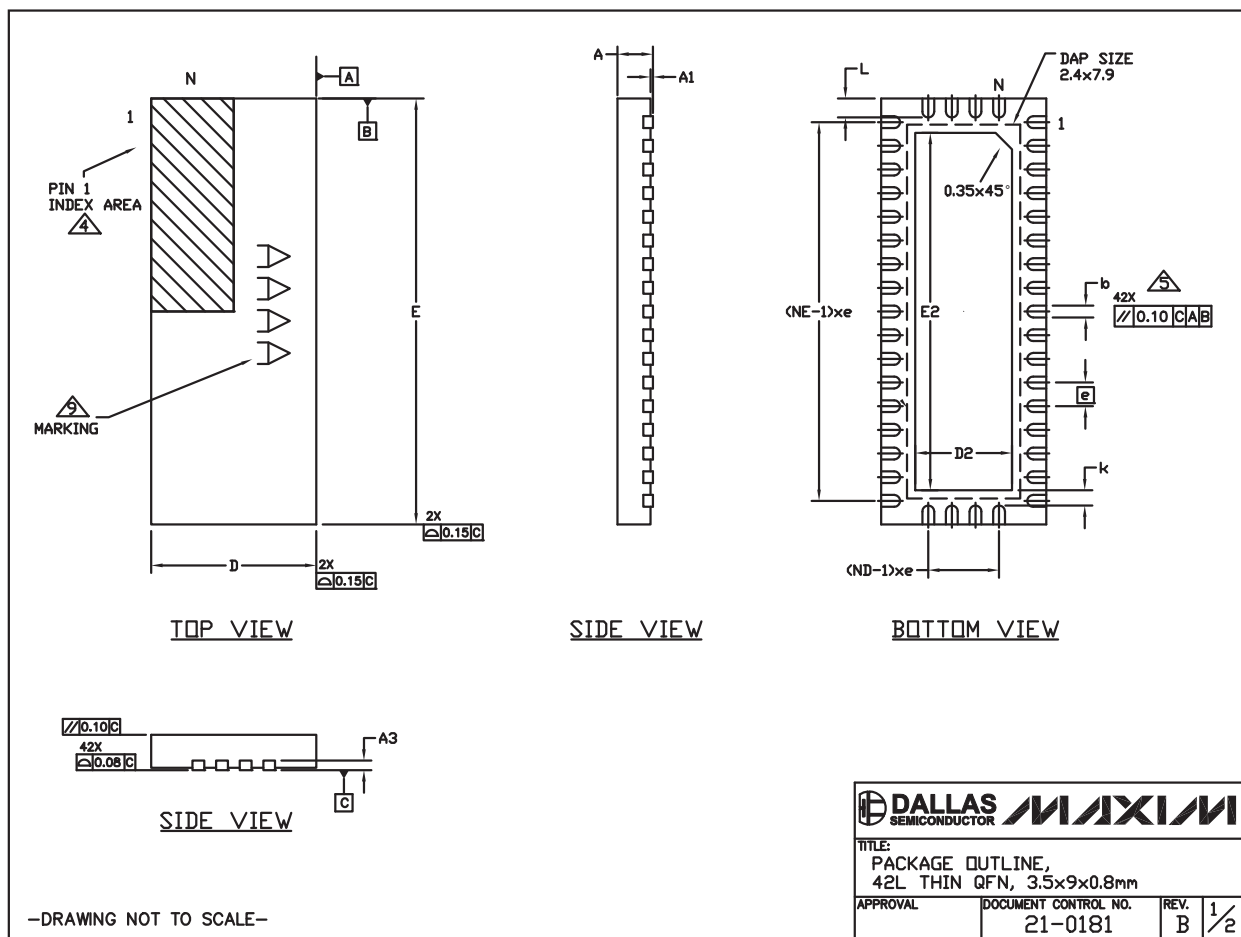
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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX4886

42L THIN QFNPS



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Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

COMMON DIMENSIONS				
REF.	MIN.	NOM.	MAX.	NOTE
A	0.70	0.75	0.80	
A1	0	—	0.05	
A3	0.20 REF.			
b	0.20	0.25	0.30	
D	3.40	3.50	3.60	
E	8.90	9.00	9.10	
e	0.50 BSC.			
k	0.25	—	—	
L	0.35	0.40	0.45	ALL PINS
N	42			
ND	4			
NE	17			

PKG. CODE	EXPOSED PAD VARIATIONS					
	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T423590-1	1.95	2.05	2.15	7.45	7.55	7.65
T423590M-1	1.95	2.05	2.15	7.45	7.55	7.65

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
8. WARPAGE SHALL NOT EXCEED 0.10mm.
9. MARKING IS FOR PACKAGE ORIENTATION PURPOSE ONLY.
10. LEAD CENTERLINES TO BE AT DEFINED BY DIMENSION e ± 0.05 .

—DRAWING NOT TO SCALE—

			
TITLE: PACKAGE OUTLINE, 42L THIN QFN, 3.5x9x0.8mm			
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