MX29GA512F H/L

DATASHEET

Contents

SINGLE VOLTAGE 3V ONLY FLASH MEMORY

FEATURES

GENERAL FEATURES

- Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
  - VCC=VI/O=2.7V~3.6V
- Byte/Word mode switchable
  - 33,554,432 x 16 / 67,108,864 x 8
- 64KW uniform sector architecture
  - 512 equal sectors
- 8-word page read buffer
- 32-word write buffer
- Latch-up protected to 100mA from -1V to 1.5xVcc
- Low Vcc write inhibit : Vcc ≤ VLKO
- Compatible with JEDEC standard
  - Pinout and software compatible to single power supply Flash
- Deep power down mode

PERFORMANCE

- High Performance
  - 100ns (Vcc=3.0~3.6V)
  - 110ns (Vcc=2.7~3.6V)
  - Page access time: 25ns
  - Fast program time: 11us/word
  - Fast erase time: 0.6s/sector
- Low Power Consumption
  - Low active read current: 20mA (typical) at 5MHz
  - Low standby current: 60uA (typical)
- Minimum 100,000 erase/program cycle
- 20 years data retention

SOFTWARE FEATURES

- Program/Erase Suspend & Program/Erase Resume
  - Suspends sector erase operation to read data from or program data to another sector which is not being erased
  - Suspends sector program operation to read data from another sector which is not being program
- Status Reply
  - Data# Polling & Toggle bits provide detection of program and erase operation completion
- Support Common Flash Interface (CFI)

HARDWARE FEATURES

- Ready/Busy# (RY/BY#) Output
  - Provides a hardware method of detecting program and erase operation completion
- Hardware Reset (RESET#) Input
  - Provides a hardware method to reset the internal state machine to read mode
- WP#/ACC input pin
  - Hardware write protect pin/Provides accelerated program capability

SECURITY

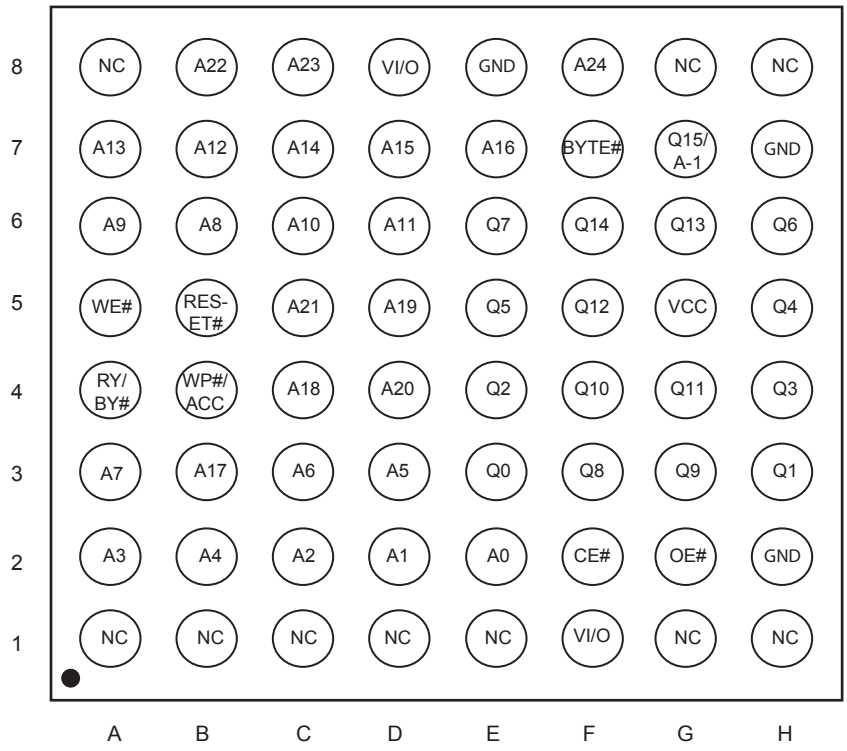
- Extra 128-word sector for security
  - Features factory locked and identifiable, and customer lockable
- Advanced sector protection/unprotection function (Solid and Password Protect)
  - Provides sector protect/unprotect function to disable or enable program or erase operation in the sector

PACKAGE

- 64-Ball FBGA (11mm x 13mm)
- **All devices are RoHS Compliant**

PIN CONFIGURATION

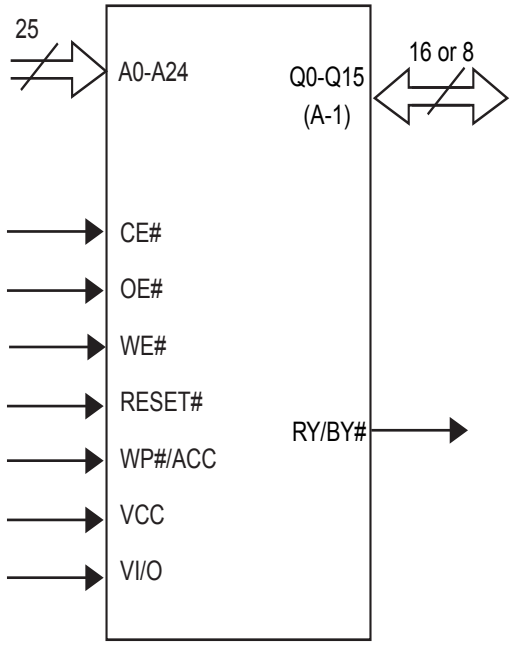
64 FBGA



PIN DESCRIPTION

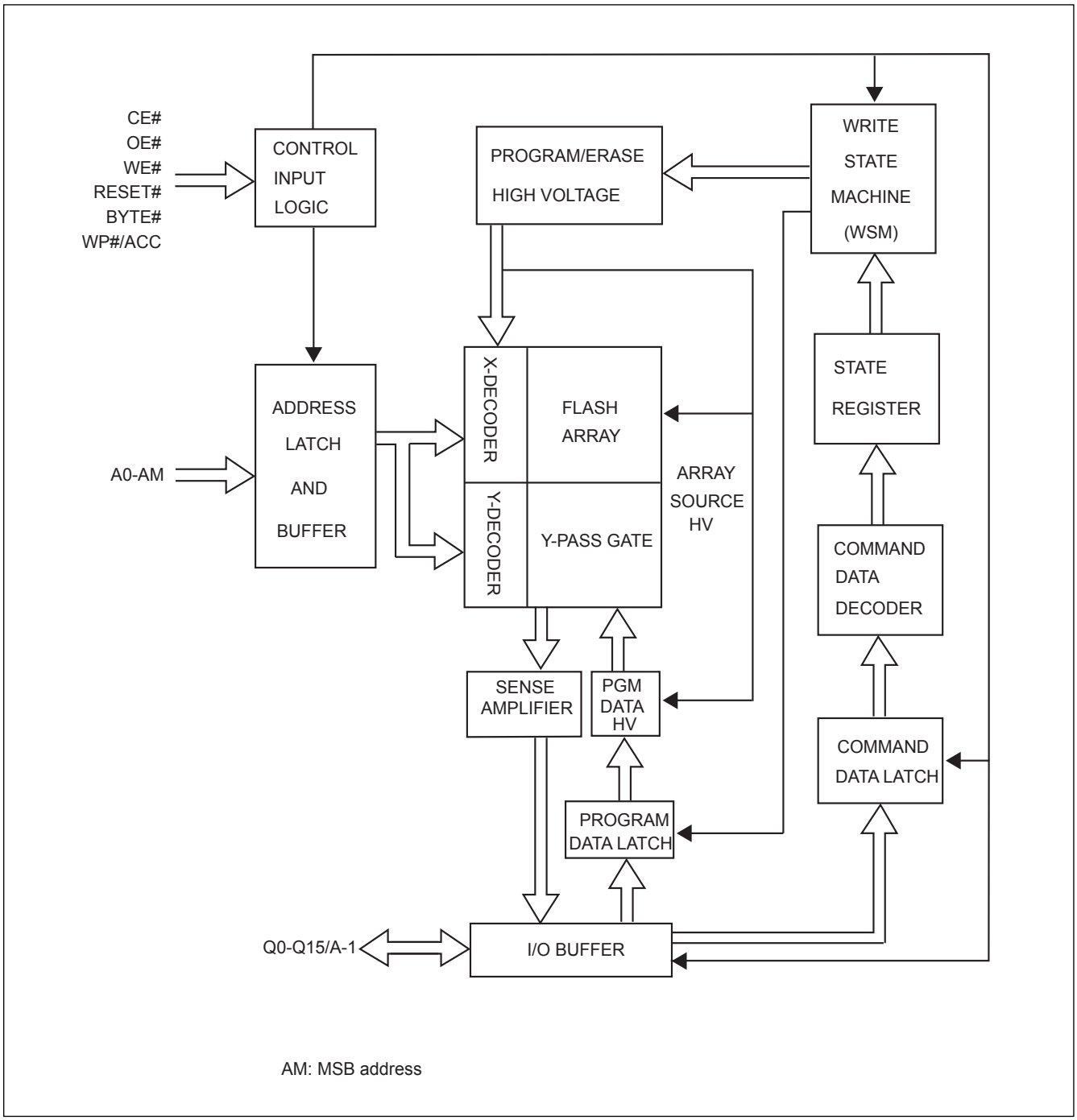
SYMBOL	PIN NAME
A0~A24	Address Input/LSB address
Q0~Q14	Data Inputs/Outputs
Q15/A-1	Q15(Word Mode)/LSB address
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
RESET#	Hardware Reset Pin, Active Low
WP#/ACC	Hardware Write Protect/Programming Acceleration input
RY/BY#	Ready/Busy Output
VCC	+3.0V single power supply
GND	Device Ground
NC	Pin Not Connected Internally

LOGIC SYMBOL



Note:
1. WP#/ACC has internal pull up.
2. VI/O voltage must be tied with VCC.

BLOCK DIAGRAM



BLOCK DIAGRAM DESCRIPTION

The block diagram on Page 7 illustrates a simplified architecture of MX29GA512F H/L. Each block in the block diagram represents one or more circuit modules in the real chip used to access, erase, program, and read the memory array.

The "CONTROL INPUT LOGIC" block receives input pins CE#, OE#, WE#, RESET#, and WP#/ACC. It creates internal timing control signals according to the input pins and outputs to the "ADDRESS LATCH AND BUFFER" to latch the external address pins A0-AM(MSB of address). The internal addresses are output from this block to the main array and decoders composed of "X-DECODER", "Y-DECODER", "Y-PASS GATE", AND "FLASH ARRAY". The X-DECODER decodes the word-lines of the flash array, while the Y-DECODER decodes the bit-lines of the flash array. The bit lines are electrically connected to the "SENSE AMPLIFIER" and "PGM DATA HV" selectively through the Y-PASS GATES. SENSE AMPLIFIERS are used to read out the contents of the flash memory, while the "PGM DATA HV" block is used to selectively deliver high power to bit-lines during programming. The "I/O BUFFER" controls the input and output on the Q0-Q15/A-1 pads. During read operation, the I/O BUFFER receives data from SENSE AMPLIFIERS and drives the output pads accordingly. In the last cycle of program command, the I/O BUFFER transmits the data on Q0-Q15/A-1 to "PROGRAM DATA LATCH", which controls the high power drivers in "PGM DATA HV" to selectively program the bits in a word or byte according to the user input pattern.

The "PROGRAM/ERASE HIGH VOLTAGE" block comprises the circuits to generate and deliver the necessary high voltage to the X-DECODER, FLASH ARRAY, and "PGM DATA HV" blocks. The logic control module comprises of the "WRITE STATE MACHINE, WSM", "STATE REGISTER", "COMMAND DATA DECODER", and "COMMAND DATA LATCH". When the user issues a command by toggling WE#, the command on Q0-Q15/A-1 is latched in the COMMAND DATA LATCH and is decoded by the COMMAND DATA DECODER. The STATE REGISTER receives the command and records the current state of the device. The WSM implements the internal algorithms for program or erase according to the current command state by controlling each block in the block diagram.

ARRAY ARCHITECTURE

The main flash memory array can be organized as Byte mode (x8) or Word mode (x16). The details of the address ranges and the corresponding sector addresses are shown in Table 1.

BLOCK STRUCTURE

Table 1. MX29GA512F H/L SECTOR ARCHITECTURE

Sector Size		Sector	Sector Address A24-A16	Address Range (x16)
Kbytes	Kwords			
128	64	SA0	000000000	0000000h-000FFFFh
128	64	SA1	000000001	0010000h-001FFFFh
128	64	SA2	000000010	0020000h-002FFFFh
:	:	:	:	:
:	:	:	:	:
128	64	SA511	111111111	1FF0000h-1FFFFFFh

BUS OPERATION

Table 2-1. BUS OPERATION

Mode Select	RESET#	CE#	WE#	OE#	Address (Note4)	Data I/O Q15~Q0	WP#/ ACC
Device Reset	L	X	X	X	X	HighZ	L/H
Standby Mode	Vcc ± 0.3V	Vcc ± 0.3V	X	X	X	HighZ	H
Output Disable	H	L	H	H	X	HighZ	L/H
Read Mode	H	L	H	L	AIN	DOUT	L/H
Write	H	L	L	H	AIN	DIN	Note1,2
Accelerate Program	H	L	L	H	AIN	DIN	Vhv

Notes:
1. The first or last sector was protected if WP#/ACC=Vil.
2. When WP#/ACC = Vih, the protection conditions of the outmost sector depends on previous protection conditions. Refer to the advaned protect feature.
3. Q0~Q15 are input (DIN) or output (DOUT) pins according to the requests of command sequence, sector protection, or data polling algorithm.

Table 2-2. BUS OPERATION

Item	Control Input			AM to A12	A11 to A10	A9	A8 to A7	A6	A5 to A4	A3 to A2	A1	A0	Q7 ~ Q0	Q15 ~ Q8
	CE#	WE#	OE#											
Sector Lock Status Verification	L	H	L	SA	X	V_{hv}	X	L	X	L	H	L	01h or 00h (Note 1)	X
Read Silicon ID Manufacturer Code	L	H	L	X	X	V_{hv}	X	L	X	L	L	L	C2H	X
Read Silicon ID -- MX29GA512F H/L														
Cycle 1	L	H	L	X	X	V_{hv}	X	L	X	L	L	H	7EH	22H(Word)
Cycle 2	L	H	L	X	X	V_{hv}	X	L	X	H	H	L	39H	22H(Word)
Cycle 3	L	H	L	X	X	V_{hv}	X	L	X	H	H	H	01H	22H(Word)

Notes:
1. Sector unprotected code:00h. Sector protected code:01h.
2. Factory locked code: WP# protects high address sector: 99h.
   WP# protects low address sector: 89h
   Factory unlocked code: WP# protects high address sector: 19h.
   WP# protects low address sector: 09h
3. AM: MSB of address.

FUNCTIONAL OPERATION DESCRIPTION

READ OPERATION

To perform a read operation, the system addresses the desired memory array or status register location by providing its address on the address pins and simultaneously enabling the chip by driving CE# & OE# LOW, and WE# HIGH. After the Tce and Toe timing requirements have been met, the system can read the contents of the addressed location by reading the Data (I/O) pins. If either the CE# or OE# is held HIGH, the outputs will remain tri-stated and no data will appear on the output pins.

PAGE READ

This device is able to provide high performance page read. Page size is 8 words. The higher address Amax ~ A3 select the certain page, while A2~A0 for word mode select the particular word in a page. The page access time is Taa or Tce, following by Tpa for the rest of the page read time. When CE# toggles, access time is Taa or Tce. Page mode can be turned on by keeping "page-read address" constant and changing the "intra-read page" addresses.

WRITE OPERATION

To perform a write operation, the system provides the desired address on the address pins, enables the chip by asserting CE# LOW, and disables the Data (I/O) pins by holding OE# HIGH. The system then places data to be written on the Data (I/O) pins and pulses WE# LOW. The device captures the address information on the falling edge of WE# and the data on the rising edge of WE#. To see an example, please refer to the timing diagram in Figure 1. The system is not allowed to write invalid commands (commands not defined in this datasheet) to the device. Writing an invalid command may put the device in an undefined state.

DEVICE RESET

Driving the RESET# pin LOW for a period of Trp or more will return the device to Read mode. If the device is in the middle of a program or erase operation, the reset operation will take at most a period of Tready1 before the device returns to Read mode. Until the device does returns to Read mode, the RY/BY# pin will remain Low (Busy Status).

When the RESET# pin is held at GND±0.3V, the device only consumes standby (Isbr) current. However, the device draws larger current if the RESET# pin is held at a voltage greater than GND+0.3V and less than or equal to Vil.

It is recommended to tie the system reset signal to the RESET# pin of the flash memory. This allows the device to be reset with the system and puts it in a state where the system can immediately begin reading boot code from it.

STANDBY MODE

The device enters Standby mode whenever the RESET# and CE# pins are both held High except in the embedded mode. While in this mode, WE# and OE# will be ignored, all Data Output pins will be in a high impedance state, and the device will draw minimal (Isb) current.

FUNCTIONAL OPERATION DESCRIPTION (cont'd)

OUTPUT DISABLE

While in active mode (RESET# HIGH and CE# LOW), the OE# pin controls the state of the output pins. If OE# is held HIGH, all Data (I/O) pins will remain tri-stated. If held LOW, the Word Data (I/O) pins will drive data.

HARDWARE WRITE PROTECT

By driving the WP#/ACC pin LOW. The highest or lowest was protected from all erase/program operations. If WP#/ACC is held HIGH (Vih to VCC), these sectors revert to their previously protected/unprotected status.

ACCELERATED PROGRAMMING OPERATION

By applying high voltage (Vhv) to the WP#/ACC pin, the device will enter the Accelerated Programming mode. This mode permits the system to skip the normal command unlock sequences and program word locations directly. During accelerated programming, the current drawn from the WP#/ACC pin is no more than ICP1.

WRITE BUFFER PROGRAMMING OPERATION

Programs 32words in a programming operation. To trigger the Write Buffer Programming, start by the first two unlock cycles, then third cycle writes the Write Buffer Load command at the destined programming Sector Address. The forth cycle writes the "word locations subtract one" number.

Following above operations, system starts to write the mingling of address and data. After the programming of the first address or data, the "write-buffer-page" is selected. The following data should be within the above mentioned page.

The "write-buffer-page" is selected by choosing address Amax-A5.

"Write-Buffer-Page" address has to be the same for all address/ data write into the write buffer. If not, operation will ABORT.

To program the content of the write buffer page this command must be followed by a write to buffer Program confirm command.

The operation of write-buffer can be suspended or resumed by the standard commands, once the write buffer programming operation is finished, it'll return to normal READ mode.

ABORT will be executed for the Write Buffer Programming Sequence if following condition occurs:
- The value loaded is bigger than the page buffer size during "Number of Locations to Program"
- Address written in a sector is not the same as the one assigned during the Write-Buffer-Load command.
- Address/ Data pair written to a different write-buffer-page than the one assigned by the "Starting Address" during
  the "write buffer data loading" operation.
- Writing not "Confirm Command" after the assigned number of "data load" cycles.

At Write Buffer Abort mode, the status register will be Q1=1, Q7=DATA# (last address written), Q6=toggle.
A Write-to-Buffer-Abort Reset command sequence has to be written to reset the device for the next operation.

FUNCTIONAL OPERATION DESCRIPTION (cont'd)

WRITE BUFFER PROGRAMMING OPERATION (cont'd)

Write buffer programming can be conducted in any sequence. However the CFI functions, autoselect, Secured Silicon sector are not functional when program operation is in progress. Multiple write buffer programming operations on the same write buffer address range without intervening erases is available. Any bit in a write buffer address range can't be programmed from 0 back to 1.

SECTOR PROTECT OPERATION

The device provides user programmable protection against program/erase operations for selected sectors. Please refer to Table 1 which show all Sector assignments.

During the protection operation, the sector address of any sector within a Sector may be used to specify the Sector being protected.

AUTOMATIC SELECT BUS OPERATIONS

The following five bus operations require A9 to be raised to Vhv. Please see AUTOMATIC SELECT COMMAND SEQUENCE in the COMMAND OPERATIONS section for details of equivalent command operations that do not require the use of Vhv.

SECTOR LOCK STATUS VERIFICATION

To determine the protected state of any sector using bus operations, the system performs a READ OPERATION with A9 raised to Vhv, the sector address applied to address pins Amx to A12, address pins A6, A3, A2 & A0 held LOW, and address pin A1 held HIGH. If data bit Q0 is LOW, the sector is not protected, and if Q0 is HIGH, the sector is protected.

READ SILICON ID MANUFACTURER CODE

To determine the Silicon ID Manufacturer Code, the system performs a READ OPERATION with A9 raised to Vhv and address pins A6, A3, A2, A1, & A0 held LOW. The Macronix ID code of C2h should be present on data bits Q7 to Q0.

READ INDICATOR BIT (Q7) FOR SECURITY SECTOR

To determine if the Security Sector has been locked at the factory, the system performs a READ OPERATION with A9 raised to Vhv, address pin A6, A3 & A2 held LOW, and address pins A1 & A0 held HIGH. If the Security Sector has been locked at the factory, the code 99h(H)/89h(L) will be present on data bits Q7 to Q0. Otherwise, the factory unlocked code of 19h(H)/09h(L) will be present.

FUNCTIONAL OPERATION DESCRIPTION (cont'd)

INHERENT DATA PROTECTION

To avoid accidental erasure or programming of the device, the device is automatically reset to Read mode during power up. Additionally, the following design features protect the device from unintended data corruption.

COMMAND COMPLETION

Only after the successful completion of the specified command sets will the device begin its erase or program operation. The failure in observing valid command sets will result in the memory returning to read mode.

LOW VCC WRITE INHIBIT

The device refuses to accept any write command when Vcc is less than VLKO. This prevents data from spuriously being altered during power-up, power-down, or temporary power interruptions. The device automatically resets itself when Vcc is lower than VLKO and write cycles are ignored until Vcc is greater than VLKO. The system must provide proper signals on control pins after Vcc rises above VLKO to avoid unintentional program or erase operations.

WRITE PULSE "GLITCH" PROTECTION

CE#, WE#, OE# pulses shorter than 5ns are treated as glitches and will not be regarded as an effective write cycle.

LOGICAL INHIBIT

A valid write cycle requires both CE# and WE# at Vil with OE# at Vih. Write cycle is ignored when either CE# at Vih, WE# at Vih, or OE# at Vil.

POWER-UP SEQUENCE

Upon power up, the device is placed in Read mode. Furthermore, program or erase operation will begin only after successful completion of specified command sequences.

POWER-UP WRITE INHIBIT

When WE#, CE# is held at Vil and OE# is held at Vih during power up, the device ignores the first command on the rising edge of WE#.

POWER SUPPLY DECOUPLING

A 0.1uF capacitor should be connected between the Vcc and GND to reduce the noise effect.

COMMAND OPERATIONS

READING THE MEMORY ARRAY

Read mode is the default state after power up or after a reset operation. To perform a read operation, please refer to READ OPERATION in the BUS OPERATIONS section above.

If the device receives an Erase Suspend command while in the Sector Erase state, the erase operation will pause (after a time delay not exceeding 20us) and the device will enter Erase-Suspended Read mode. While in the Erase-Suspended Read mode, data can be programmed or read from any sector not being erased. Reading from addresses within sector(s) being erased will only return the contents of the status register, which is in fact how the current status of the device can be determined.

If a program command is issued to any inactive (not currently being erased) sector during Erase-Suspended Read mode, the device will perform the program operation and automatically return to Erase-Suspended Read mode after the program operation completes successfully.

While in Erase-Suspended Read mode, an Erase Resume command must be issued by the system to reactivate the erase operation. The erase operation will resume from where is was suspended and will continue until it completes successfully or another Erase Suspend command is received.

After the memory device completes an embedded operation (automatic Chip Erase, Sector Erase, or Program) successfully, it will automatically return to Read mode and data can be read from any address in the array. If the embedded operation fails to complete, as indicated by status register bit Q5 (exceeds time limit flag) going HIGH during the operations, the system must perform a reset operation to return the device to Read mode.

There are several states that require a reset operation to return to Read mode:

1. A program or erase failure--indicated by status register bit Q5 going HIGH during the operation. Failures during either of these states will prevent the device from automatically returning to Read mode.

2. The device is in Auto Select mode or CFI mode. These two states remain active until they are terminated by a reset operation.

In the two situations above, if a reset operation (either hardware reset or software reset command) is not performed, the device will not return to Read mode and the system will not be able to read array data.

AUTOMATIC PROGRAMMING OF THE MEMORY ARRAY

The device provides the user the ability to program the memory array in Word mode. As long as the users enters the correct cycle defined in the Table 3 (including 2 unlock cycles and the A0H program command), any word data provided on the data lines by the system will automatically be programmed into the array at the specified location.

After the program command sequence has been executed, the internal write state machine (WSM) automatically executes the algorithms and timings necessary for programming and verification, which includes generating suitable program pulses, checking cell threshold voltage margins, and repeating the program pulse if any cells do not pass verification or have low margins. The internal controller protects cells that do pass verification and margin tests from being over-programmed by inhibiting further program pulses to these passing cells as weaker cells continue to be programmed.

With the internal WSM automatically controlling the programming process, the user only needs to enter the program command and data once.

COMMAND OPERATIONS (cont'd)

AUTOMATIC PROGRAMMING OF THE MEMORY ARRAY (cont'd)

Programming will only change the bit status from "1" to "0". It is not possible to change the bit status from "0" to "1" by programming. This can only be done by an erase operation. Furthermore, the internal write verification only checks and detects errors in cases where a "1" is not successfully programmed to "0".

Any commands written to the device during programming will be ignored except hardware reset or program suspend. Hardware reset will terminate the program operation after a period of time no more than 10us. When the embedded program algorithm is complete or the program operation is terminated by a hardware reset, the device will return to Read mode. Program suspend ready, the device will enter program suspend read mode.

After the embedded program operation has begun, the user can check for completion by reading the following bits in the status register:

Status	Q7*1	Q6*1	Q5	Q1	RY/BY# (Note)
In progress	Q7#	Toggling	0	0	0
Exceed time limit	Q7#	Toggling	1	N/A	0

Note: RY/BY# is an open drain output pin and should be connected to VCC through a high value pull-up resistor.

ERASING THE MEMORY ARRAY

There are two types of erase operations performed on the memory array -- Sector Erase and Chip Erase. In the Sector Erase operation, one or more selected sectors may be erased simultaneously. In the Chip Erase operation, the complete memory array is erased except for any protected sectors. More details of the protected sectors are explained in section 5.

SECTOR ERASE

The sector erase operation is used to clear data within a sector by returning all of its memory locations to the "1" state. It requires six command cycles to initiate the erase operation. The first two cycles are "unlock cycles", the third is a configuration cycle, the fourth and fifth are also "unlock cycles", and the sixth cycle is the Sector Erase command. After the sector erase command sequence has been issued, an internal 50us time-out counter is started. Until this counter reaches zero, additional sector addresses and Sector Erase commands may be issued thus allowing multiple sectors to be selected and erased simultaneously. After the 50us time-out counter has expired, no new commands will be accepted and the embedded sector erase operation will begin. Note that the 50us timer-out counter is restarted after every erase command sequence. If the user enters any command other than Sector Erase or Erase Suspend during the time-out period, the erase operation will abort and the device will return to Read mode.

After the embedded sector erase operation begins, all commands except Erase Suspend will be ignored. The only way to interrupt the operation is with an Erase Suspend command or with a hardware reset. The hardware reset will completely abort the operation and return the device to Read mode.

COMMAND OPERATIONS (cont'd)

SECTOR ERASE (cont'd)

The system can determine the status of the embedded sector erase operation by the following methods:

Status	Q7	Q6	Q5	Q3*1	Q2	RY/BY#*2
Time-out period	0	Toggling	0	0	Toggling	0
In progress	0	Toggling	0	1	Toggling	0
Exceeded time limit	0	Toggling	1	1	Toggling	0

Note:
1. The Q3 status bit is the 50us time-out indicator. When Q3=0, the 50us time-out counter has not yet reached zero and a new Sector Erase command may be issued to specify the address of another sector to be erased. When Q3=1, the 50us time-out counter has expired and the Sector Erase operation has already begun. Erase Suspend is the only valid command that may be issued once the embedded erase operation is underway.
2. RY/BY# is open drain output pin and should be connected to VCC through a high value pull-up resistor.
3. When an attempt is made to erase only protected sector(s), the erase operation will abort thus preventing any data changes in the protected sector(s). Q7 will output "0" and Q6 will toggle briefly (100us or less) before aborting and returning the device to Read mode. If unprotected sectors are also specified, however, they will be erased normally and the protected sector(s) will remain unchanged.
4. Q2 is a localized indicator showing a specified sector is undergoing erase operation or not. Q2 toggles when user reads at addresses where the sectors are actively being erased (in erase mode) or to be erased (in erase suspend mode).

CHIP ERASE

The Chip Erase operation is used erase all the data within the memory array. All memory cells containing a "0" will be returned to the erased state of "1". This operation requires 6 write cycles to initiate the action. The first two cycles are "unlock" cycles, the third is a configuration cycle, the fourth and fifth are also "unlock" cycles, and the sixth cycle initiates the chip erase operation.

During the chip erase operation, no other software commands will be accepted, but if a hardware reset is received or the working voltage is too low, that chip erase will be terminated. After Chip Erase, the chip will automatically return to Read mode.

The system can determine the status of the embedded chip erase operation by the following methods:

Status	Q7	Q6	Q5	Q2	RY/BY#*1
In progress	0	Toggling	0	Toggling	0
Exceed time limit	0	Toggling	1	Toggling	0

*1: RY/BY# is open drain output pin and should be connected to VCC through a high value pull-up resistor.

COMMAND OPERATIONS (cont'd)

ERASE SUSPEND/RESUME

After beginning a sector erase operation, Erase Suspend is the only valid command that may be issued. If system issues an Erase Suspend command during the 50us time-out period following a Sector Erase command, the time-out period will terminate immediately and the device will enter Erase-Suspended Read mode. If the system issues an Erase Suspend command after the sector erase operation has already begun, the device will not enter Erase-Suspended Read mode until 20us time has elapsed. The system can determine if the device has entered the Erase-Suspended Read mode through Q6, Q7, and RY/BY#.

After the device has entered Erase-Suspended Read mode, the system can read or program any sector(s) except those being erased by the suspended erase operation. Reading any sector being erased or programmed will return the contents of the status register. Whenever a suspend command is issued, user must issue a resume command and check Q6 toggle bit status, before issue another erase command. The system can use the status register bits shown in the following table to determine the current state of the device:

Status	Q7	Q6	Q5	Q3	Q2	Q1	RY/BY#
Erase suspend read in erase suspended sector	1	No toggle	0	N/A	toggle	N/A	1
Erase suspend read in non-erase suspended sector	Data	Data	Data	Data	Data	Data	1
Erase suspend program in non-erase suspended sector	Q7#	Toggle	0	N/A	N/A	N/A	0

When the device has suspended erasing, user can execute the command sets except sector erase and chip erase, such as read silicon ID, sector protect verify, program, CFI query and erase resume.

After the device has entered Erase-Suspended Read Mode, Sector Erase, Chip Erase and Program Suspend commands are forbidden.

SECTOR ERASE RESUME

The sector Erase Resume command is valid only when the device is in Erase-Suspended Read mode. After erase resumes, the user can issue another Ease Suspend command, but there should be a 400us interval between Ease Resume and the next Erase Suspend command.

COMMAND OPERATIONS (cont'd)

PROGRAM SUSPEND/RESUME

After beginning a program operation, Program Suspend is the only valid command that may be issued. The system can determine if the device has entered the Program-Suspended Read mode through Q6, and RY/BY#.

After the device has entered Program-Suspended mode, the system can read any sector(s) except those being programd by the suspended program operation. Reading the sector being program suspended is invalid. Whenever a suspend command is issued, user must issue a resume command and check Q6 toggle bit status, before issue another program command. The system can use the status register bits shown in the following table to determine the current state of the device:

Status	Q7	Q6	Q5	Q3	Q2	Q1	RY/BY#
Program suspend read in program suspended sector	Invalid						1
Program suspend read in non-program suspended sector	Data	Data	Data	Data	Data	Data	1

When the device has Program/Erase suspended, user can execute read array, auto-select, read CFI, read security silicon. Program and Erase Suspend commands are forbidden after the device entered Program-Suspend mode.

PROGRAM RESUME

The Program Resume command is valid only when the device is in Program-Suspended mode. After program resumes, the user can issue another Program Suspend command, but there should be a 5us interval between Program Resume and the next Program Suspend command.

BUFFER WRITE ABORT

Q1 is the indicator of Buffer Write Abort. When Q1=1, the device will abort from buffer write and go back to read status register shown as following table:

Status	Q7	Q6	Q5	Q3	Q2	Q1	RY/BY#
Buffer Write Busy	Q7#	Toggle	0	N/A	N/A	0	0
Buffer Write Abort	Q7#	Toggle	0	N/A	N/A	1	0
Buffer Write Exceeded Time Limit	Q7#	Toggle	1	N/A	N/A	0	0

COMMAND OPERATIONS (cont'd)

AUTOMATIC SELECT OPERATIONS

When the device is in Read mode, Program Suspend Read mode, Erase-Suspended Read mode, or CFI mode, the user can issue the Automatic Select command shown in Table 3 (two unlock cycles followed by the Automatic Select command 90h) to enter Automatic Select mode. After entering Automatic Select mode, the user can query the Manufacturer ID, Device ID, Security Sector locked status, or Sector protected status multiple times without issuing a new Automatic Select command.

While In Automatic Select mode, issuing a Reset command (F0h) will return the device to Read mode (or Ease-Suspended Read mode if Erase-Suspend was active or Program Suspend Read mode if Program Suspend was active).

Another way to enter Automatic Select mode is to use one of the bus operations shown in Table 2. BUS OPERATION_2. After the high voltage (Vhv) is removed from the A9 pin, the device will automatically return to Read mode or Erase-Suspended Read mode.

AUTOMATIC SELECT COMMAND SEQUENCE

Automatic Select mode is used to access the manufacturer ID, device ID and to verify whether or not secured silicon is locked and whether or not a sector is protected. The automatic select mode has four command cycles. The first two are unlock cycles, and followed by a specific command. The fourth cycle is a normal read cycle, and user can read at any address any number of times without entering another command sequence. The Reset command is necessary to exit the Automatic Select mode and back to read array. The following table shows the identification code with corresponding address.

	Address		Data (Hex)	Representation
Manufacturer ID	Word	X00	C2	
Device ID	Word	X01/0E/0F	227E/2239/2201	
Secured Silicon	Word	X03	99/19 (H) 89/09 (L)	Factory locked/unlocked
Sector Protect Verify	Word	(Sector address) X 02	00/01	Unprotected/protected

After entering automatic select mode, no other commands are allowed except the reset command.

COMMAND OPERATIONS (cont'd)

READ MANUFACTURER ID OR DEVICE ID

The Manufacturer ID (identification) is a unique hexadecimal number assigned to each manufacturer by the JEDEC committee. Each company has its own manufacturer ID, which is different from the ID of all other companies. The number assigned to Macronix is C2h.

After entering Automatic Select mode, performing a read operation with A1 & A0 held LOW will cause the device to output the Manufacturer ID on the Data I/O (Q7 to Q0) pins.

RESET

In the following situations, executing reset command will reset device back to Read mode:

- Among erase command sequence (before the full command set is completed)
- Sector erase time-out period
- Erase fail (while Q5 is high)
- Among program command sequence (before the full command set is completed, erase-suspended program included)
- Program fail (while Q5 is high, and erase-suspended program fail is included)
- Auto-Select mode
- CFI mode

While device is at the status of program fail or erase fail (Q5 is high), user must issue reset command to reset device back to read array mode. While the device is in Auto-Select mode or CFI mode, user must issue reset command to reset device back to read array mode.

When the device is in the progress of programming (not program fail) or erasing (not erase fail), device will ignore reset command.

SECURITY SECTOR FLASH MEMORY REGION

The Security Sector region is an extra OTP memory space of 128 words in length. The security sector can be locked upon shipping from factory, or it can be locked by customer after shipping. Customer can issue Security Sector Factory Protect Verify and/or Security Sector Protect Verify to query the lock status of the device. After enter Security Sector region, it is forbidden to enter Lock Register, DPB, SPB, SPB lock region.

In factory-locked device, security sector region is protected when shipped from factory and the security silicon sector indicator bit is set to "1". In customer lockable device, security sector region is unprotected when shipped from factory and the security silicon indicator bit is set to "0".

Factory Locked: Security Sector Programmed and Protected at the Factory

In a factory locked device, the Security Sector is permanently locked before shipping from the factory. The device will have a 8-word ESN in the security region. The ESN occupies addresses 00000h to 00007h in word mode.

Secured Silicon Sector Address Range	Standard Factory Locked	Express Flash Factory Locked	Customer Lockable
000000h-000007h	ESN	ESN or Determined by Customer	Determined by Customer
000008h-00007Fh	Unavailable	Determined by Customer	

Customer Lockable: Security Sector NOT Programmed or Protected at the Factory

When the security feature is not required, the security region can act as an extra memory space.

Security silicon sector can also be protected by two methods. Note that once the security silicon sector is protected, there is no way to unprotect the security silicon sector and the content of it can no longer be altered.

After the security silicon is locked and verified, system must write Exit Security Sector Region, go through a power cycle, or issue a hardware reset to return the device to read normal array mode.

TABLE 3. COMMAND DEFINITIONS

Command		Read Mode	Reset Mode	Automatic Select				Security Sector Region	Exit Security Sector	Program
				Silicon ID	Device ID	Factory Protect Verify	Sector Protect Verify			
1st Bus Cycle	Addr	Addr	XXX	555	555	555	555	555	555	555
	Data	Data	F0	AA	AA	AA	AA	AA	AA	AA
2nd Bus Cycle	Addr			2AA	2AA	2AA	2AA	2AA	2AA	2AA
	Data			55	55	55	55	55	55	55
3rd Bus Cycle	Addr			555	555	555	555	555	555	555
	Data			90	90	90	90	88	90	A0
4th Bus Cycle	Addr			X00	X01	X03	(Sector) X02		XXX	Addr
	Data			C2h	ID1	99/19(H) 89/09(L)	00/01		00	Data
5th Bus Cycle	Addr				X0E					
	Data				ID2					
6th Bus Cycle	Addr				X0F					
	Data				ID3					

Command		Write to Buffer Program	Write to Buffer Program Abort Reset	Write to Buffer Program confirm	Chip Erase	Sector Erase	CFI Read	Program/ Erase Suspend	Program/ Erase Resume	Deep Power Down	
										Enter	Exit
1st Bus Cycle	Addr	555	555	SA	555	555	55	XXX	XXX	555	XXX
	Data	AA	AA	29	AA	AA	98	B0	30	AA	AB
2nd Bus Cycle	Addr	2AA	2AA		2AA	2AA				2AA	
	Data	55	55		55	55				55	
3rd Bus Cycle	Addr	SA	555		555	555				XXX	
	Data	25	F0		80	80				B9	
4th Bus Cycle	Addr	SA			555	555					
	Data	N-1			AA	AA					
5th Bus Cycle	Addr	WA			2AA	2AA					
	Data	WD			55	55					
6th Bus Cycle	Addr	WBL			555	Sec-tor					
	Data	WD			10	30					

WA= Write Address
WD= Write Data
SA= Sector Address
N= Word Count
WBL= Write Buffer Location
ID1/ID2/ID3: Refer to Table 2-2 for detail ID of each device.

Notes:
* It is not recommended to adopt any other code not in the command definition table which will potentially enter the hidden mode.

COMMON FLASH MEMORY INTERFACE (CFI) MODE

QUERY COMMAND AND COMMAND FLASH MEMORY INTERFACE (CFI) MODE

The device features CFI mode. Host system can retrieve the operating characteristics, structure and vendor-specified information such as identifying information, memory size, byte/word configuration, operating voltages and timing information of this device by CFI mode. If the system writes the CFI Query command "98h", to address "55h"/"AAh", the device will enter the CFI Query Mode, any time the device is ready to read array data. The system can read CFI information at the addresses given in Table 4.

Once user enters CFI query mode, user can issue reset command to exit CFI mode and return to read array mode. The unused CFI area is reserved by Macronix.

Table 4-1. CFI mode: Identification Data Values
(All values in these tables are in hexadecimal)

Description	Address (h) (Word Mode)	Data (h)
Query-unique ASCII string "QRY"	10	0051
	11	0052
	12	0059
Primary vendor command set and control interface ID code	13	0002
	14	0000
Address for primary algorithm extended query table	15	0040
	16	0000
Alternate vendor command set and control interface ID code	17	0000
	18	0000
Address for alternate algorithm extended query table	19	0000
	1A	0000

Table 4-2. CFI mode: System Interface Data Values

Description	Address (h) (Word Mode)	Data (h)
Vcc supply minimum program/erase voltage	1B	0027
Vcc supply maximum program/erase voltage	1C	0036
VPP supply minimum program/erase voltage	1D	0000
VPP supply maximum program/erase voltage	1E	0000
Typical timeout per single word/byte write, 2^n us	1F	0003
Typical timeout for maximum-size buffer write, 2^n us (00h, not support)	20	0006
Typical timeout per individual block erase, 2^n ms	21	0009
Typical timeout for full chip erase, 2^n ms (00h, not support)	22	0013
Maximum timeout for word/byte write, 2^n times typical	23	0003
Maximum timeout for buffer write, 2^n times typical	24	0005
Maximum timeout per individual block erase, 2^n times typical	25	0003
Maximum timeout for chip erase, 2^n times typical (00h, not support)	26	0002

Table 4-3. CFI mode: Device Geometry Data Values

Description	Address (h) (Word Mode)	Data (h)
Device size = 2^n in number of bytes (20=512Mb)	27	001A
Flash device interface description (02=asynchronous x8/x16)	28	0002
	29	0000
Maximum number of bytes in buffer write = 2^n (00h, not support)	2A	0006
	2B	0000
Number of erase regions within device (01h:uniform, 02h:boot)	2C	0001
Index for Erase Bank Area 1: [2E,2D] = # of same-size sectors in region 1-1 [30, 2F] = sector size in multiples of 256Byte	2D	00FF
	2E	0001
	2F	0000
	30	0002
Index for Erase Bank Area 2	31	0000
	32	0000
	33	0000
	34	0000
Index for Erase Bank Area 3	35	0000
	36	0000
	37	0000
	38	0000
Index for Erase Bank Area 4	39	0000
	3A	0000
	3B	0000
	3C	0000

Table 4-4. CFI mode: Primary Vendor-Specific Extended Query Data Values

Description	Address (h) (Word Mode)	Data (h)
Query - Primary extended table, unique ASCII string, PRI	40	0050
	41	0052
	42	0049
Major version number, ASCII	43	0031
Minor version number, ASCII	44	0033
Unlock recognizes address (0= recognize, 1= don't recognize)	45	0014
Erase suspend (2= to both read and program)	46	0002
Sector protect (N= # of sectors/group)	47	0001
Temporary sector unprotect (1=supported)	48	0000
Sector protect/Chip unprotect scheme	49	0008
Simultaneous R/W operation (0=not supported)	4A	0000
Burst mode (0=not supported)	4B	0000
Page mode (0=not supported, 01 = 4 word page, 02 = 8 word page)	4C	0002
Minimum ACC(acceleration) supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV	4D	0095
Maximum ACC(acceleration) supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV	4E	00A5
WP# Protection 04=Uniform sectors bottom WP# protect 05=Uniform sectors top WP# protect	4F	0004/ 0005
Program Suspend (0=not support, 1=support)	50	0001

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM STRESS RATINGS

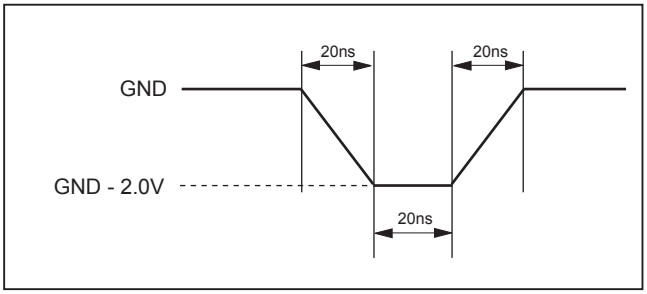
Surrounding Temperature with Bias		-65°C to +125°C
Storage Temperature		-65°C to +150°C
Voltage Range	VCC	-0.5V to +4.0V
	VI/O	-0.5V to +4.0V
	A9 , WP#/ACC	-0.5V to +10.5V
	The other pins.	-0.5V to Vcc +0.5V
Output Short Circuit Current (less than one second)		200 mA

OPERATING TEMPERATURE AND VOLTAGE

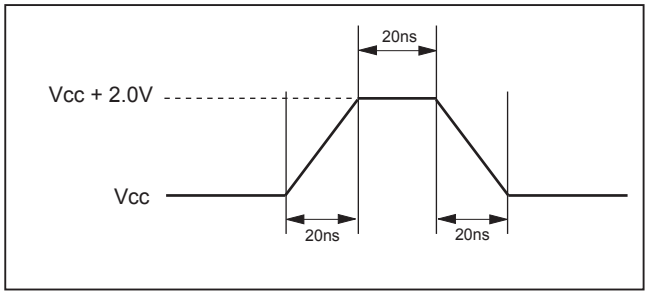
Industrial (I) Grade	Surrounding Temperature (T_A)	-40°C to +85°C
VCC Supply Voltages	Full VCC range	+2.7V to 3.6V
	Regulated VCC range	+3.0V to 3.6V
	VI/O range	+2.7V to 3.6V

NOTICE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot GND to -2.0V and Vcc to +2.0V for periods up to 20ns, see below Figure.

Maximum Negative Overshoot Waveform



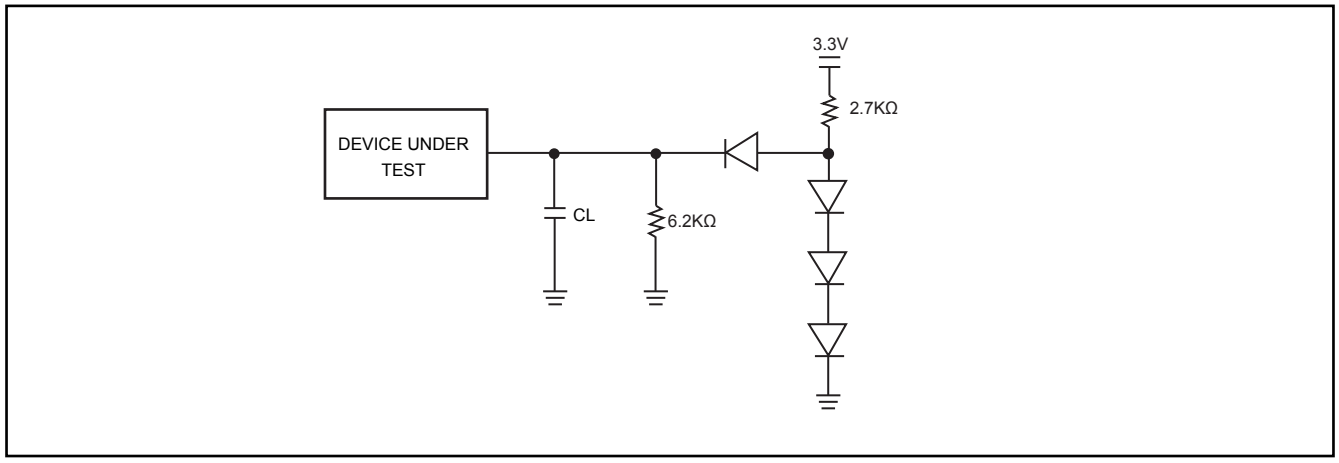
Maximum Positive Overshoot Waveform



DC CHARACTERISTICS

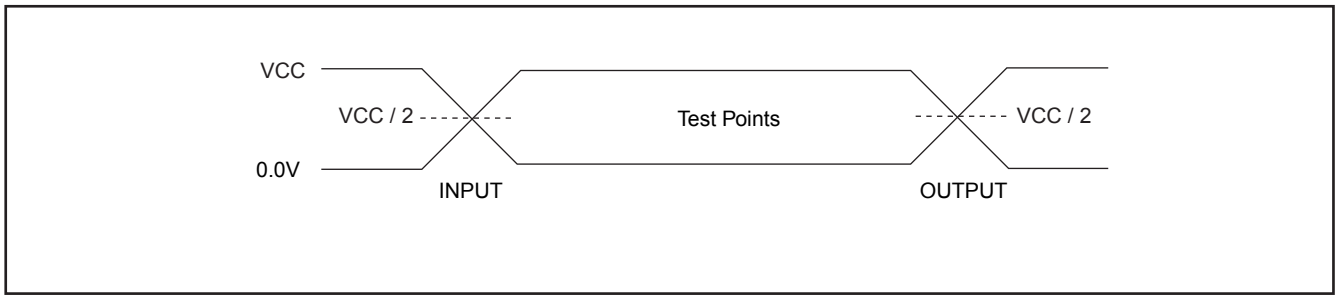
Symbol	Description	Min.	Typ.	Max.	Remark
Iilk	Input Leak			±2.0uA	
Iilk9	A9 Leak			35uA	A9=10.5V
Iolk	Output Leak			±1.0uA	
Icr1	Read Current		6mA	20mA	CE#=Vil, OE#=Vih, Vcc=Vccmax; f=1MHz
			20mA	50mA	CE#=Vil, OE#=Vih, Vcc=Vccmax; f=5MHz
			35mA	100mA	CE#=Vil, OE#=Vih, Vcc=Vccmax; f=10MHz
Icr2	VCC Page Read Current		2mA	10mA	CE#=Vil, OE#=Vih, Vcc=Vccmax; f=10MHz
			5mA	20mA	CE#=Vil, OE#=Vih, Vcc=Vccmax; f=33MHz
Icw	Write Current		26mA	30mA	CE#=Vil, OE#=Vih, WE#=Vil
Isb	Standby Current		60uA	200uA	Vcc=Vcc max, other pin disable
Isbr	Reset Current		60uA	200uA	Vcc=Vccmax, RESET# enable, other pin disable
Idpd	Vcc deep power down current		10uA	30uA	
Icp1	Accelerated Pgm Current, WP#/Acc pin(Word/Byte)		5mA	10mA	CE#=Vil, OE#=Vih
Icp2	Accelerated Pgm Current, Vcc pin, (Word/Byte)		20mA	30mA	CE#=Vil, OE#=Vih
Vil	Input Low Voltage	-0.1V		0.3xVCC	
Vih	Input High Voltage	0.7xVCC		VCC+0.3V	
Vhv	Very High Voltage for hardware Auto Select/Accelerated Program	9.5V		10.5V	
Vol	Output Low Voltage			0.45V	Iol=100uA
Voh	Ouput High Voltage	0.85xVCC			Ioh=-100uA
Vlko	Low Vcc Lock-out voltage	2.1V		2.4V	

SWITCHING TEST CIRCUITS



Test Condition
Output Load Capacitance, CL : 1TTL gate, 30pF
Rise/Fall Times : 5ns
Input pulse levels : 0.0 ~ VCC
In/Out reference levels : VCC / 2

SWITCHING TEST WAVEFORMS

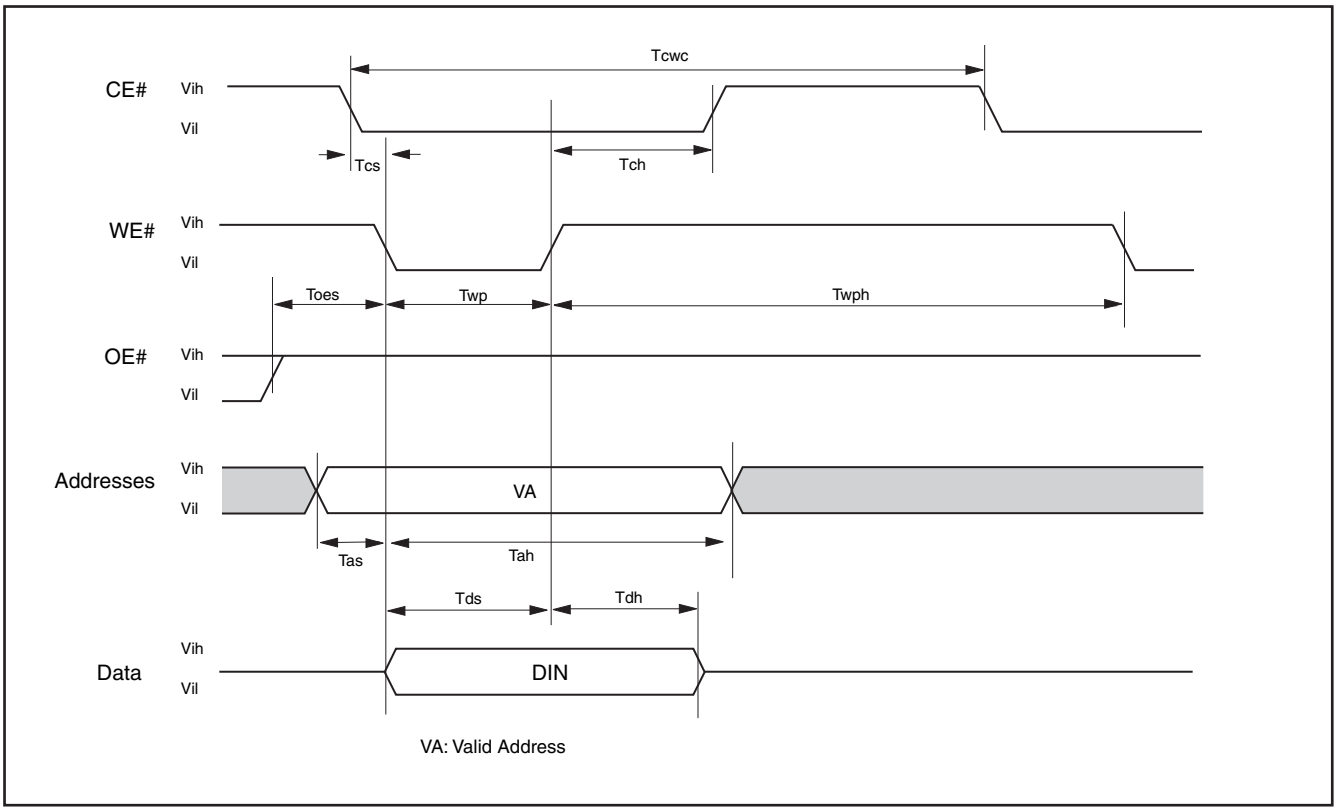


AC CHARACTERISTICS

Symbol	Description		100ns (VCC=3.0V~3.6V)			110ns (VCC=2.7V~3.6V)			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Taa	Valid data output after address				100			110	ns
Tpa	Page access time				25			25	ns
Tce	Valid data output after CE# low				100			110	ns
Toe	Valid data output after OE# low				25			25	ns
Tdf	Data output floating after OE# high or CE# high				20			20	ns
Tsrw	Latency between read and write operation		35			35			ns
Toh	Output hold time from the earliest rising edge of address, CE#, OE#		0			0			ns
Trc	Read period time		100			110			ns
Twc	Write period time		100			110			ns
Tcwc	Command write period time		100			110			ns
Tas	Address setup time		0			0			ns
Taso	Address setup time to OE# low during toggle bit polling		15			15			ns
Tah	Address hold time		45			45			ns
Taht	Address hold time from CE# or OE# high during toggle bit polling		0			0			ns
Tds	Data setup time		30			30			ns
Tdh	Data hold time		0			0			ns
Tvcs	Vcc setup time		500			500			us
Tcs	Chip enable Setup time		0			0			ns
Tch	Chip enable hold time		0			0			ns
Toes	Output enable setup time		0			0			ns
Toeh	Output enable hold time	Read	0			0			ns
		Toggle & Data# Polling	10			10			ns
Tws	WE# setup time		0			0			ns
Twh	WE# hold time		0			0			ns
Tcepw	CE# pulse width		35			35			ns
Tcepwh	CE# pulse width high		30			30			ns
Twp	WE# pulse width		35			35			ns
Twph	WE# pulse width high		30			30			ns
Tbusy	Program/Erase active time by RY/BY#				100			110	ns
Tghwl	Read recover time before write		0			0			ns
Tghel	Read recover time before write		0			0			ns
Twhwh1	Program operation (Word mode)			11			11		us
Twhwh1	Acc program operation (Word)			11			11		us
Twhwh2	Sector erase operation			0.6	5		0.6	5	sec
Tbal	Sector add hold time				50			50	us
Trdp	Release from deep power down mode				200			200	us

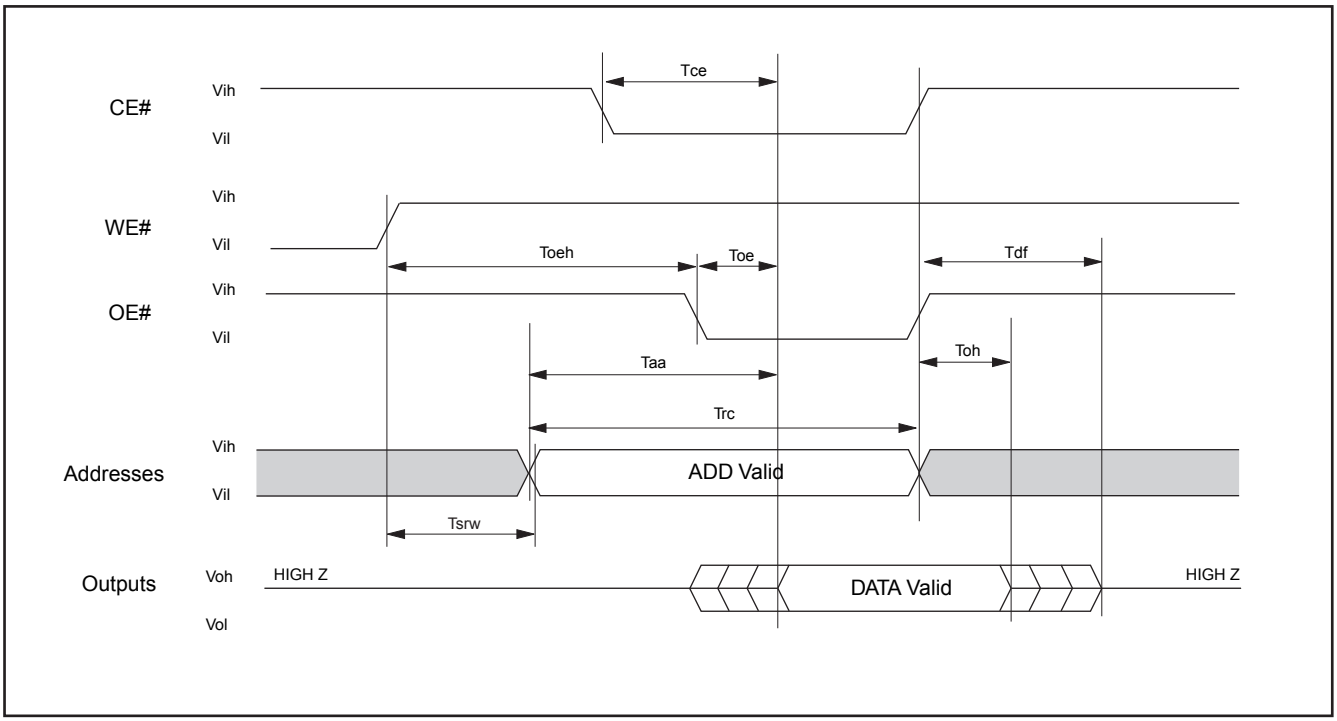
WRITE COMMAND OPERATION

Figure 1. COMMAND WRITE OPERATION



READ/RESET OPERATION

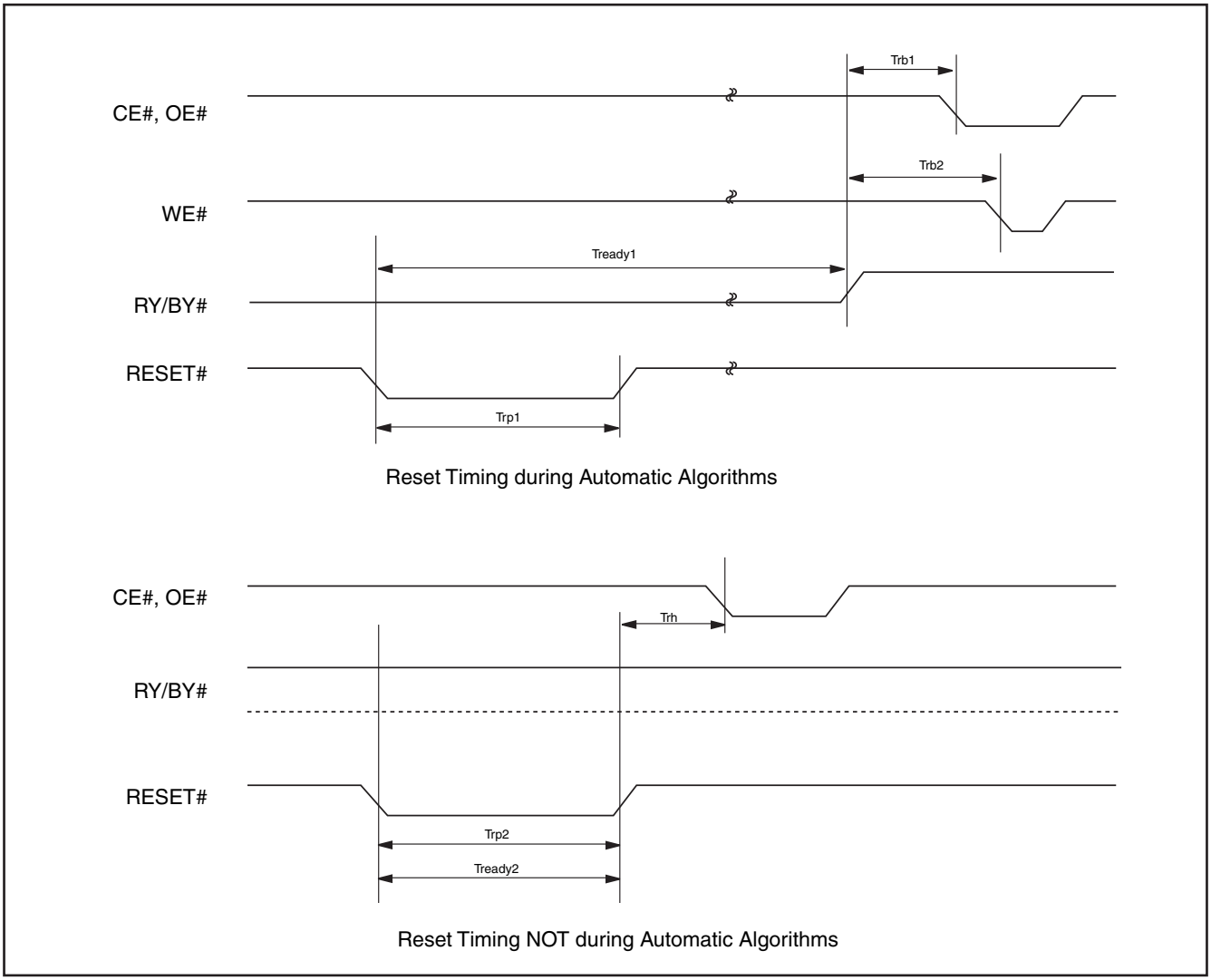
Figure 2. READ TIMING WAVEFORMS



AC CHARACTERISTICS

Item	Description	MIN/MAX	Speed	Unit
Trp1	RESET# Pulse Width (During Automatic Algorithms)	MIN	10	us
Trp2	RESET# Pulse Width (NOT During Automatic Algorithms)	MIN	500	ns
Trh	RESET# High Time Before Read	MIN	200	ns
Trb1	RY/BY# Recovery Time (to CE#, OE# go low)	MIN	0	ns
Trb2	RY/BY# Recovery Time (to WE# go low)	MIN	50	ns
Tready1	RESET# PIN Low (During Automatic Algorithms) to Read or Write	MAX	20	us
Tready2	RESET# PIN Low (NOT During Automatic Algorithms) to Read or Write	MAX	500	ns

Figure 3. RESET# TIMING WAVEFORM



ERASE/PROGRAM OPERATION

Figure 4. AUTOMATIC CHIP ERASE TIMING WAVEFORM

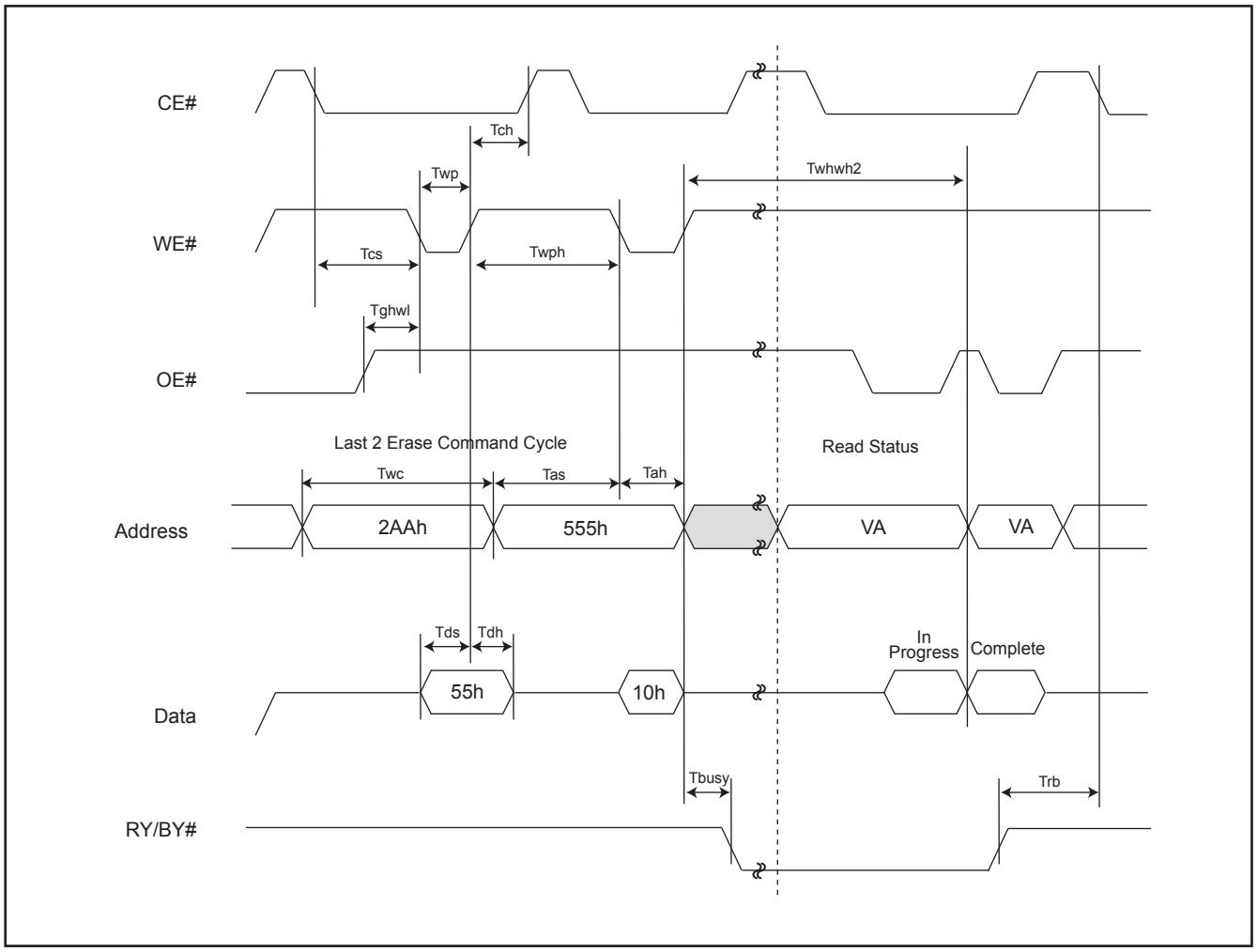


Figure 5. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART

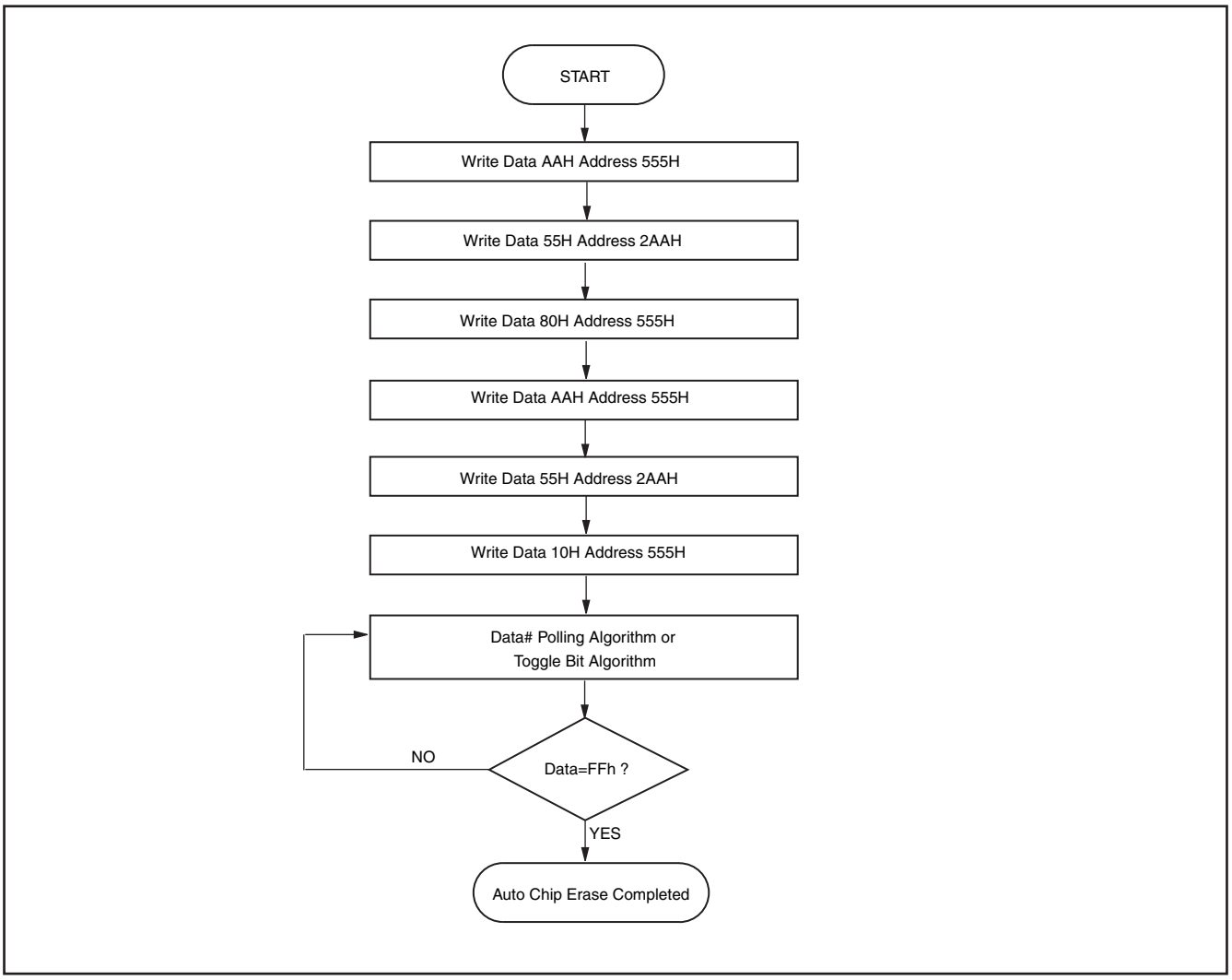


Figure 6. AUTOMATIC SECTOR ERASE TIMING WAVEFORM

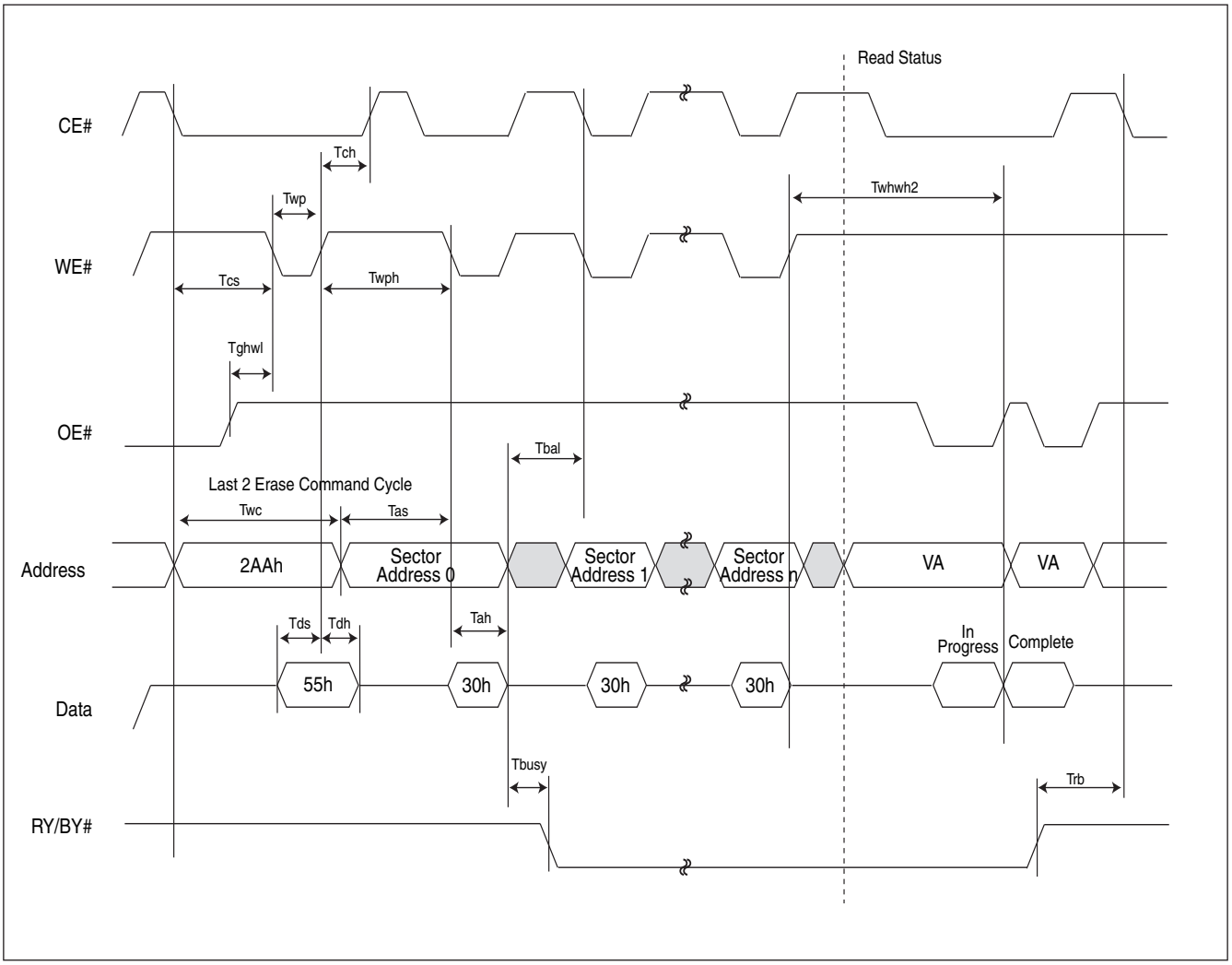


Figure 7. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART

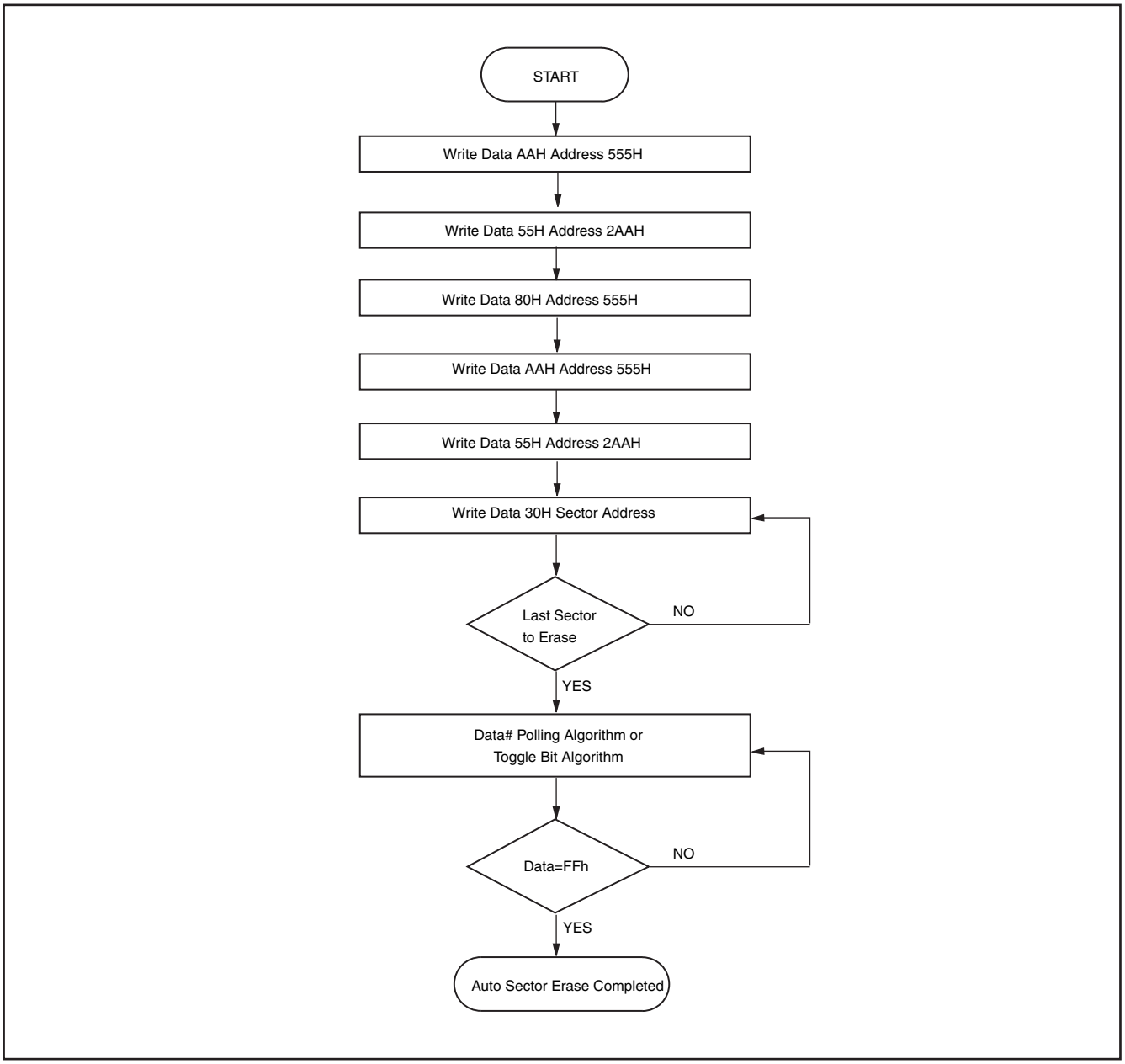


Figure 8. ERASE SUSPEND/RESUME FLOWCHART

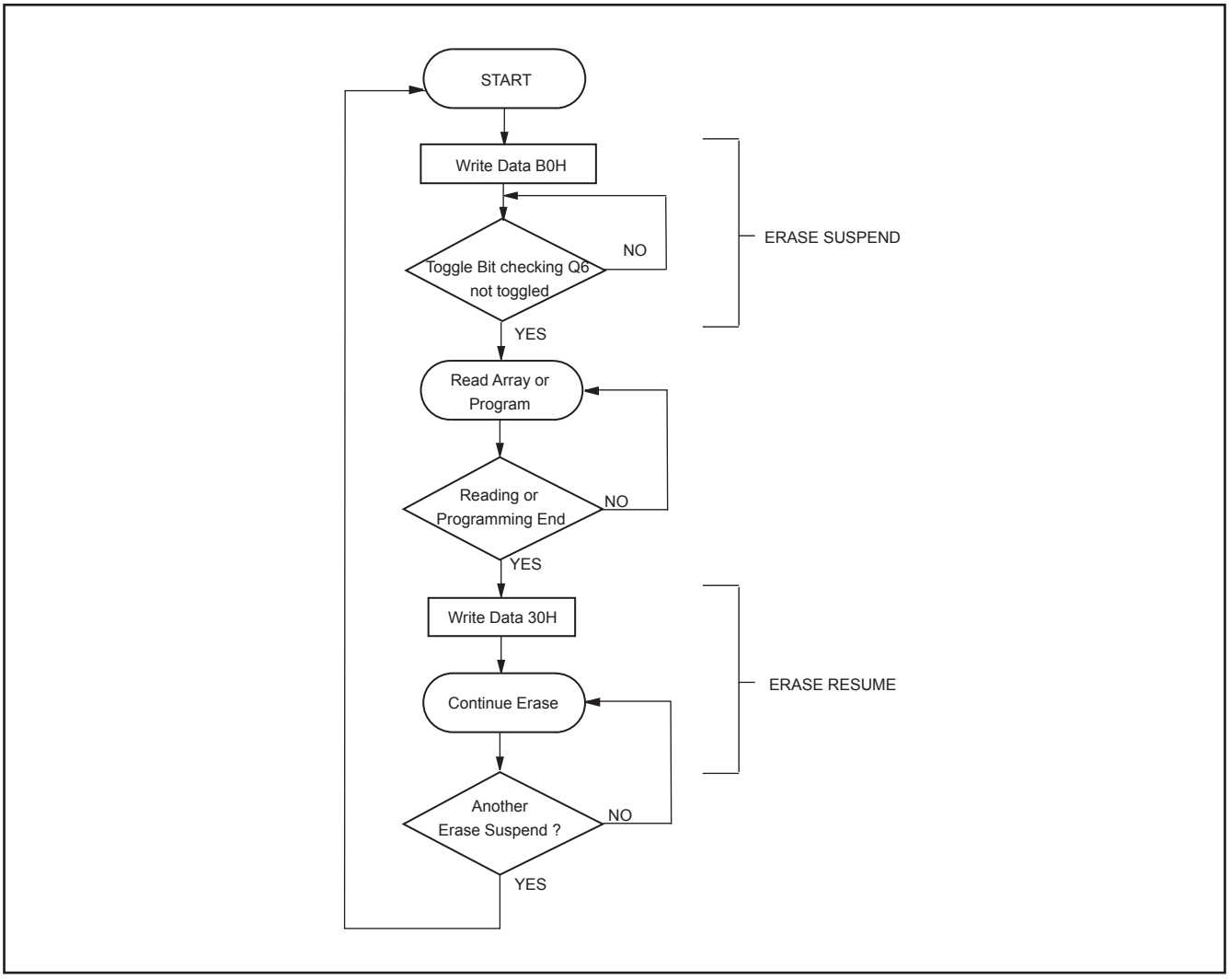


Figure 9. AUTOMATIC PROGRAM TIMING WAVEFORMS

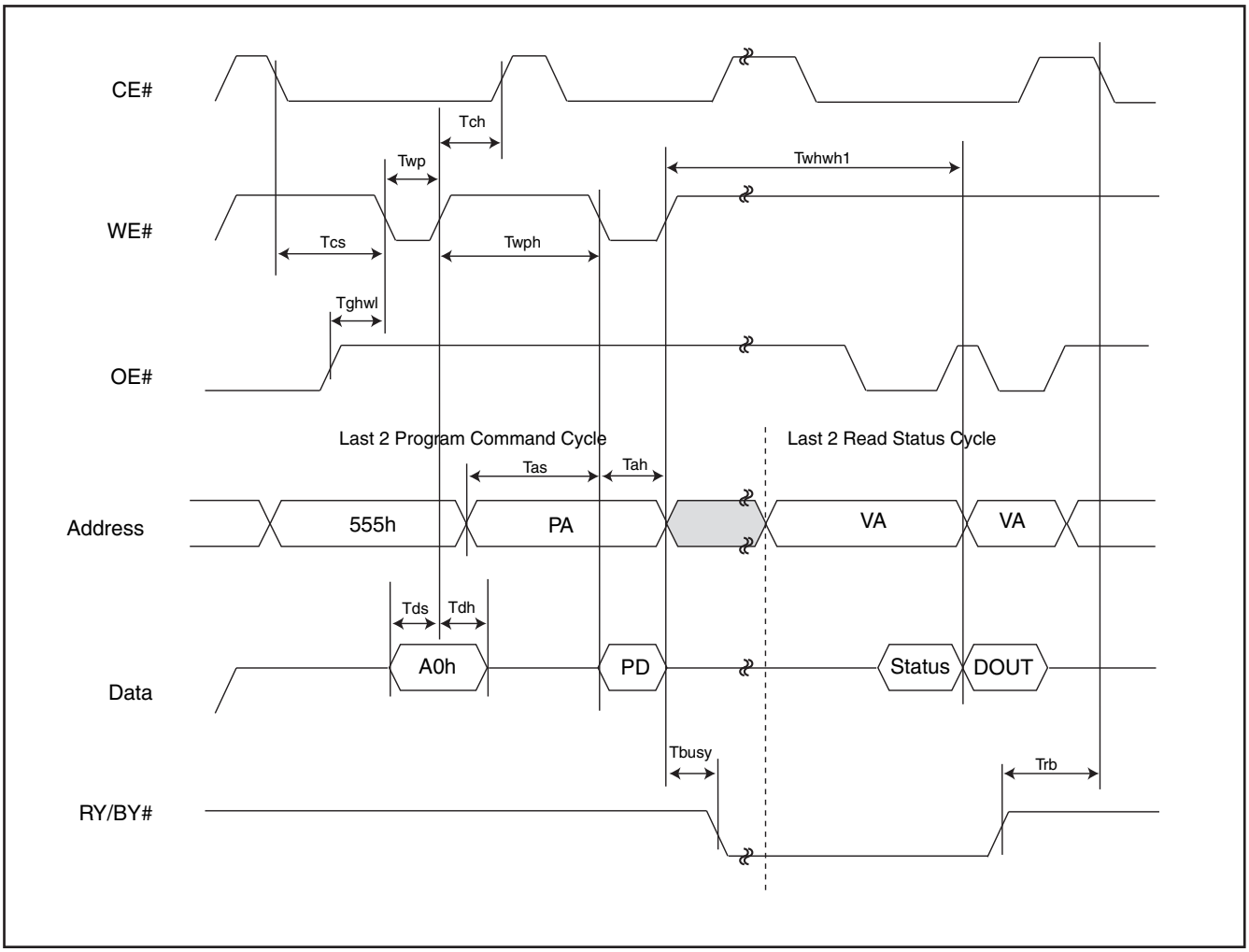


Figure 10. ACCELERATED PROGRAM TIMING DIAGRAM

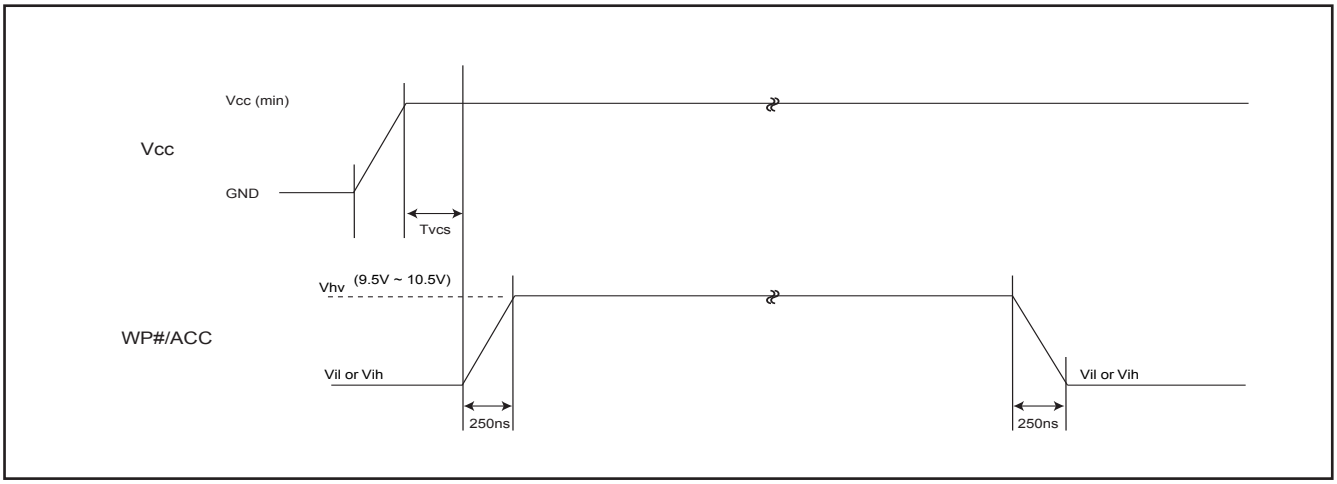


Figure 11. CE# CONTROLLED WRITE TIMING WAVEFORM

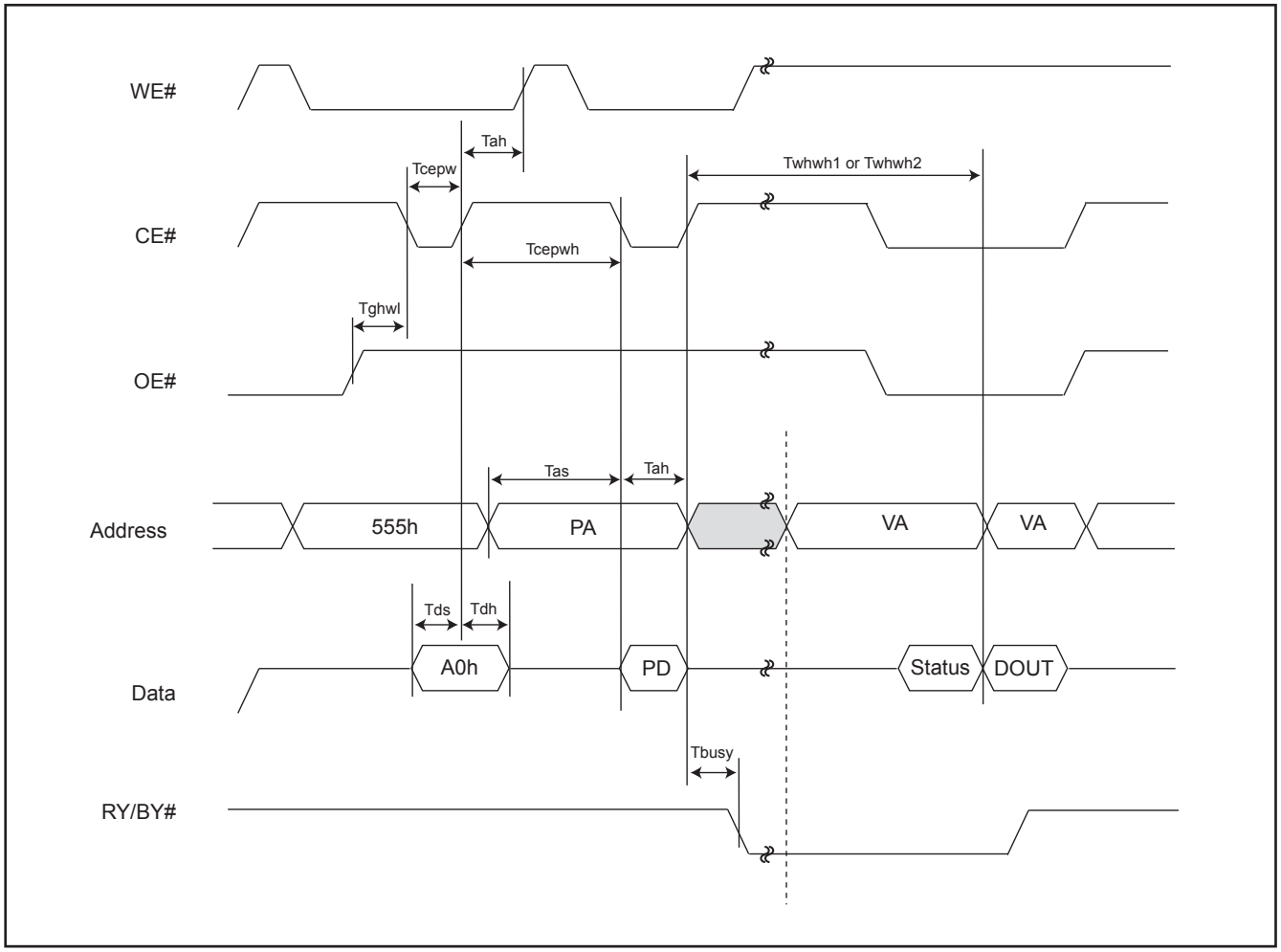


Figure 12. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART

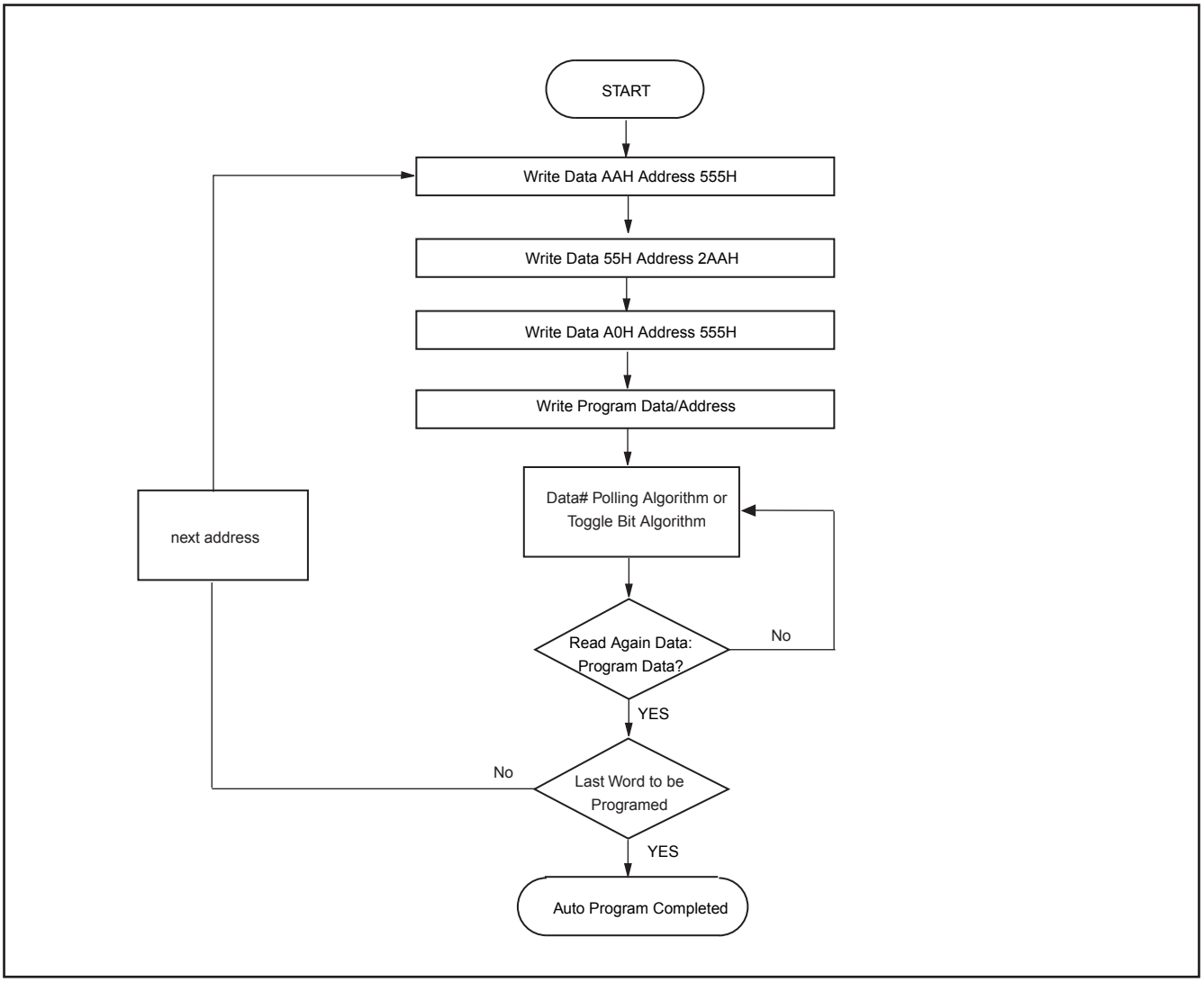
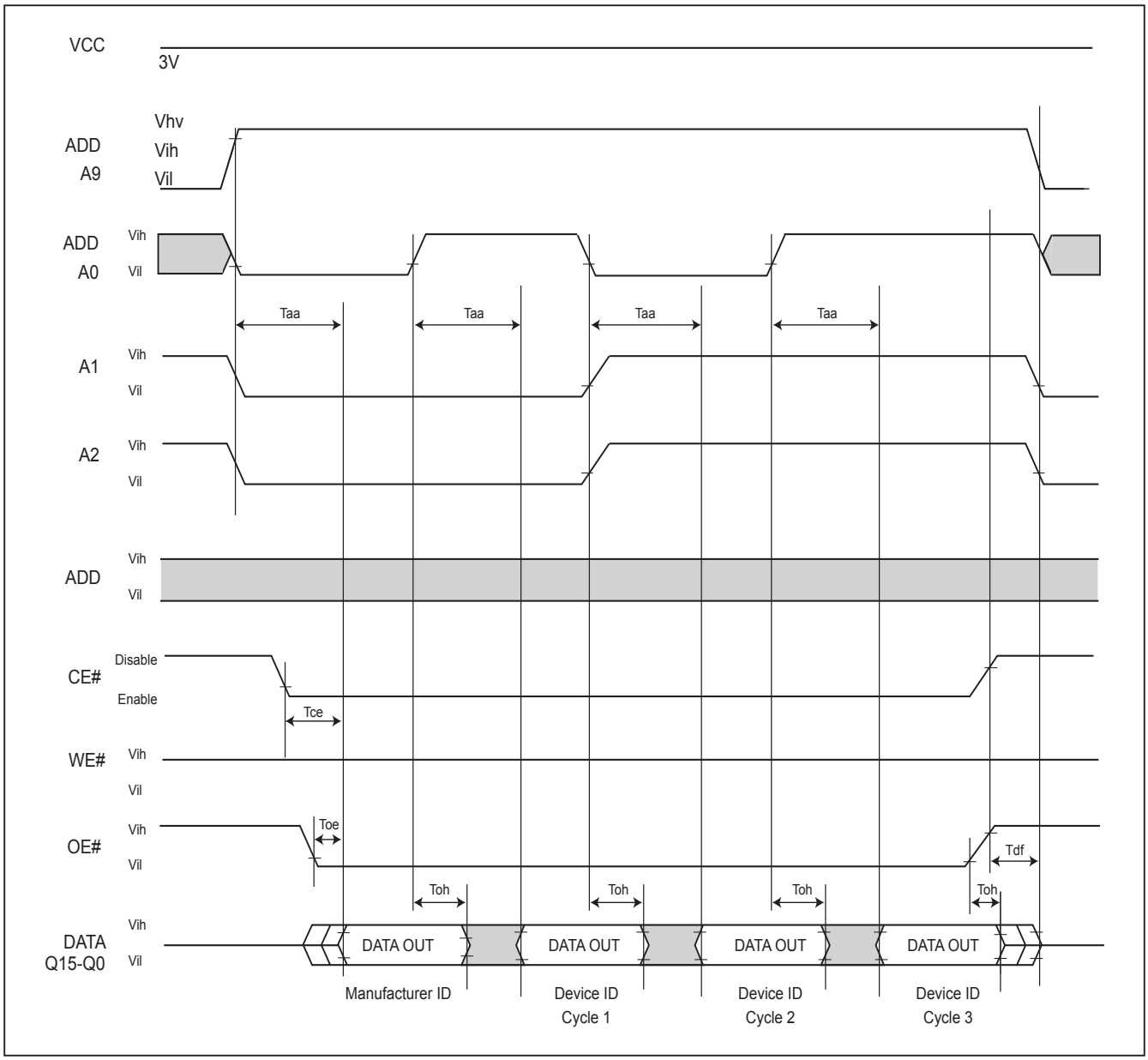


Figure 13. SILICON ID READ TIMING WAVEFORM



WRITE OPERATION STATUS

Figure 14. DATA# POLLING TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)

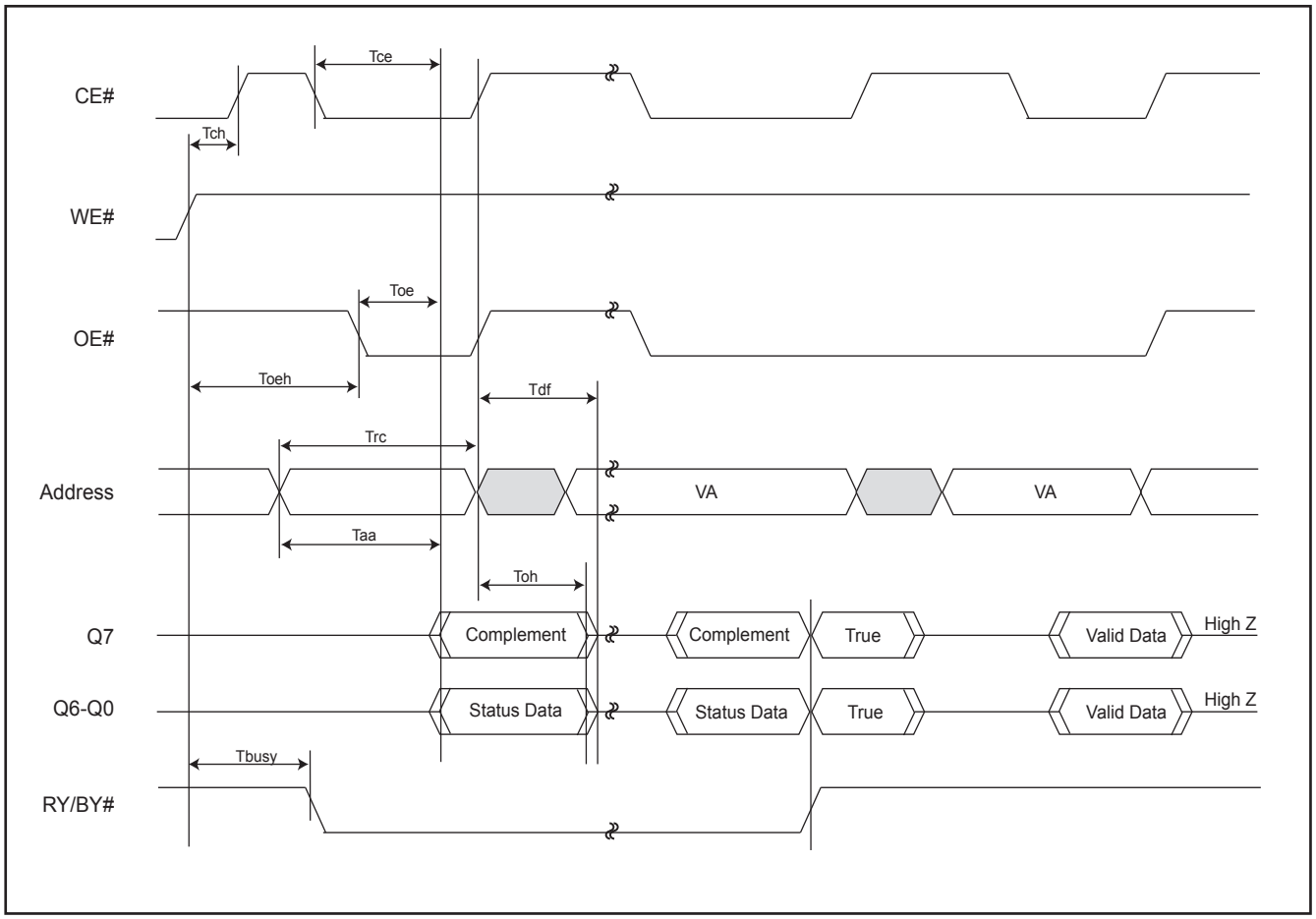
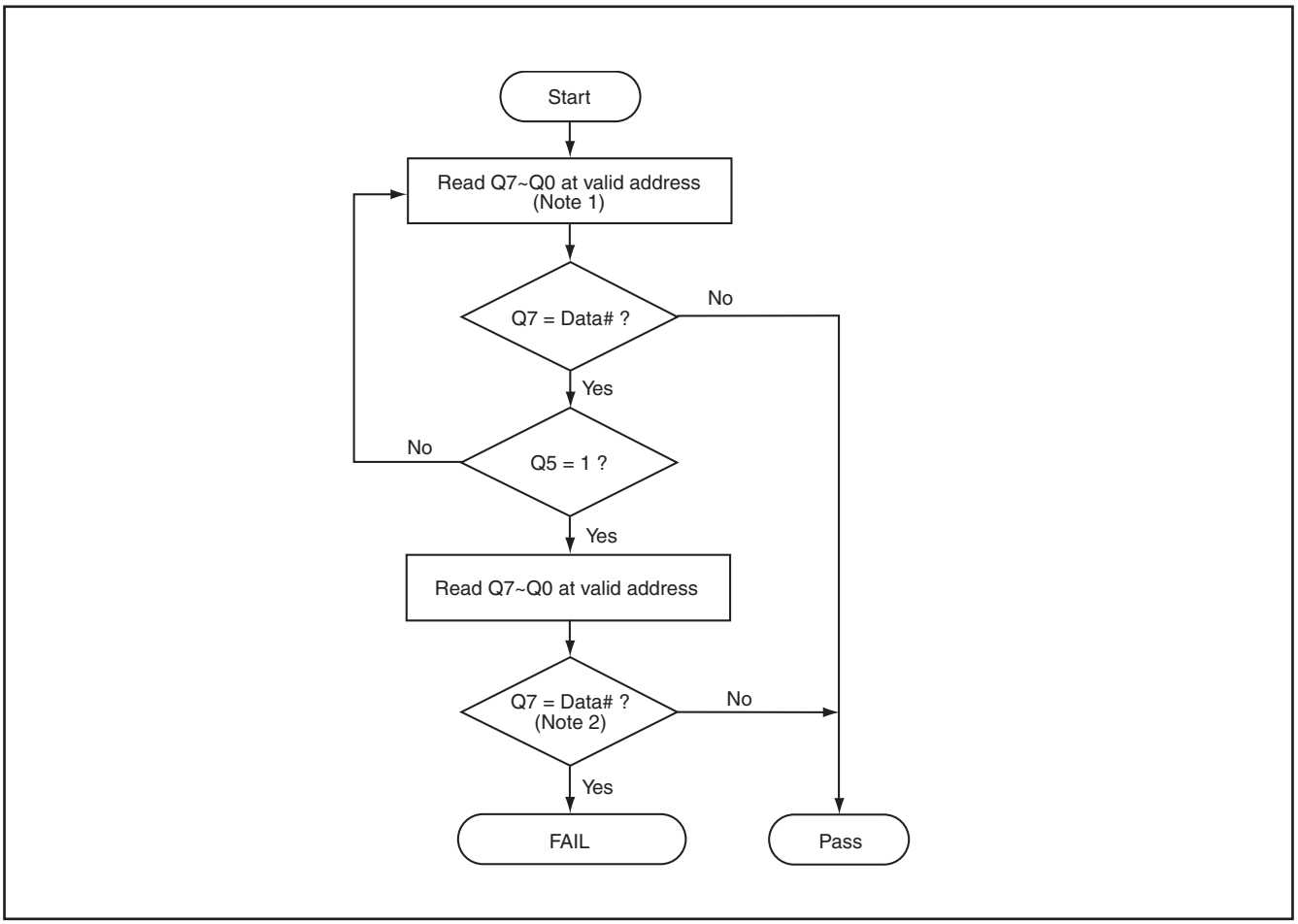
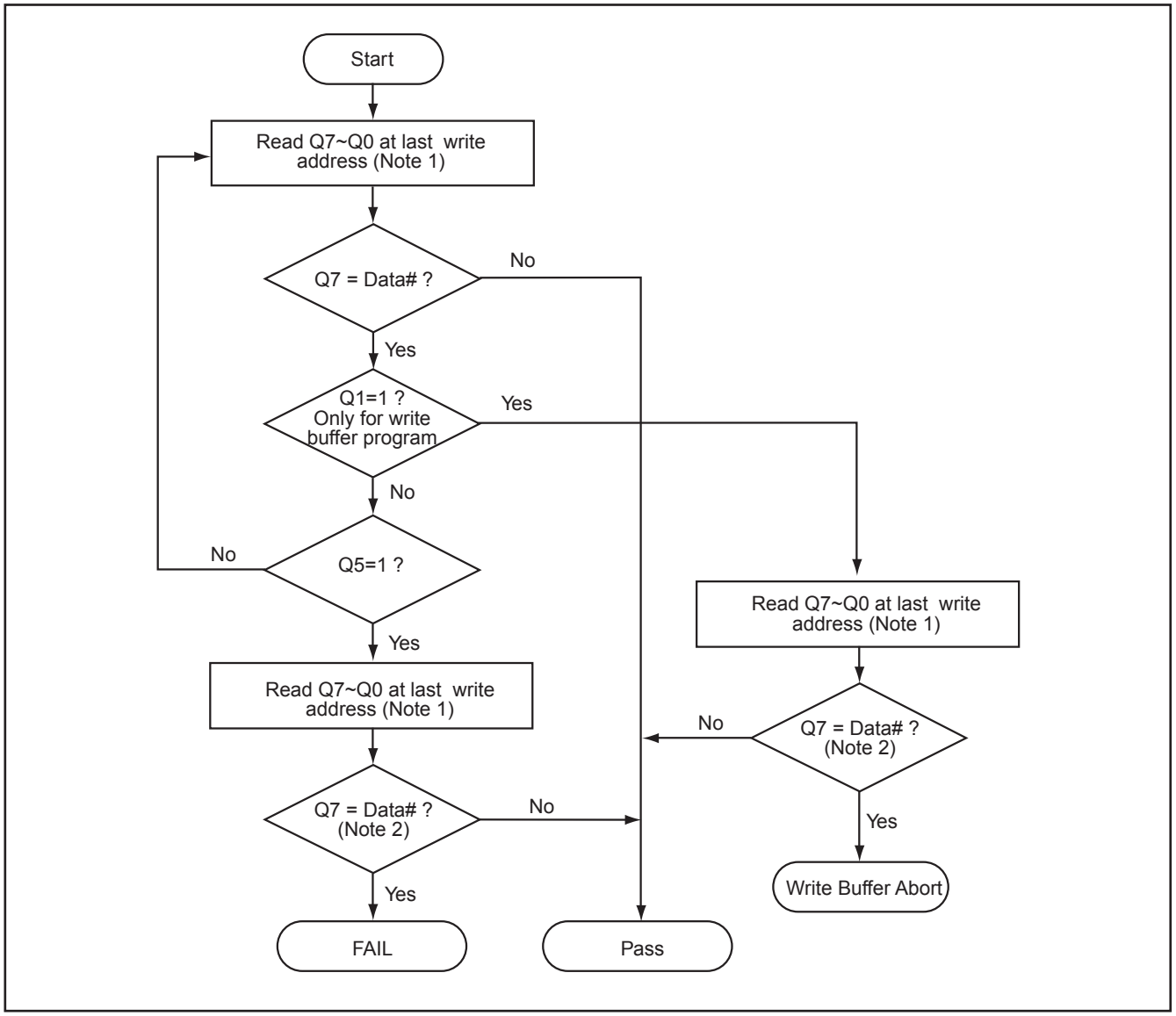


Figure 15. STATUS POLLING FOR PROGRAM/ERASE



Notes:
1. Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.
2. It is requested to provide valid address to read out correct Q5 status. For program mode and single sector erase mode: means polling status with the program/page program address or sector address.
   For multi-sector erase mode and chip erase mode: The lowest and highest erased sector need to be provided for time-out check. If Q5=1 when do status polling check for one sector address, it means erase time out.
3. During erase mode: Q2 is "don't care" after erase time out.

Figure 16. STATUS POLLING FOR WRITE BUFFER PROGRAM



Notes:
1. Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.
2. It is requested to provide valid address to read out correct Q5 status. For program mode and single sector erase mode: means polling status with the program/page program address or sector address.
   For multi-sector erase mode and chip erase mode: The lowest and highest erased sector need to be provided for time-out check. If Q5=1 when do status polling check for one sector address, it means erase time out.
3. During erase mode: Q2 is "don't care" after erase time out.

Figure 17. TOGGLE BIT TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)

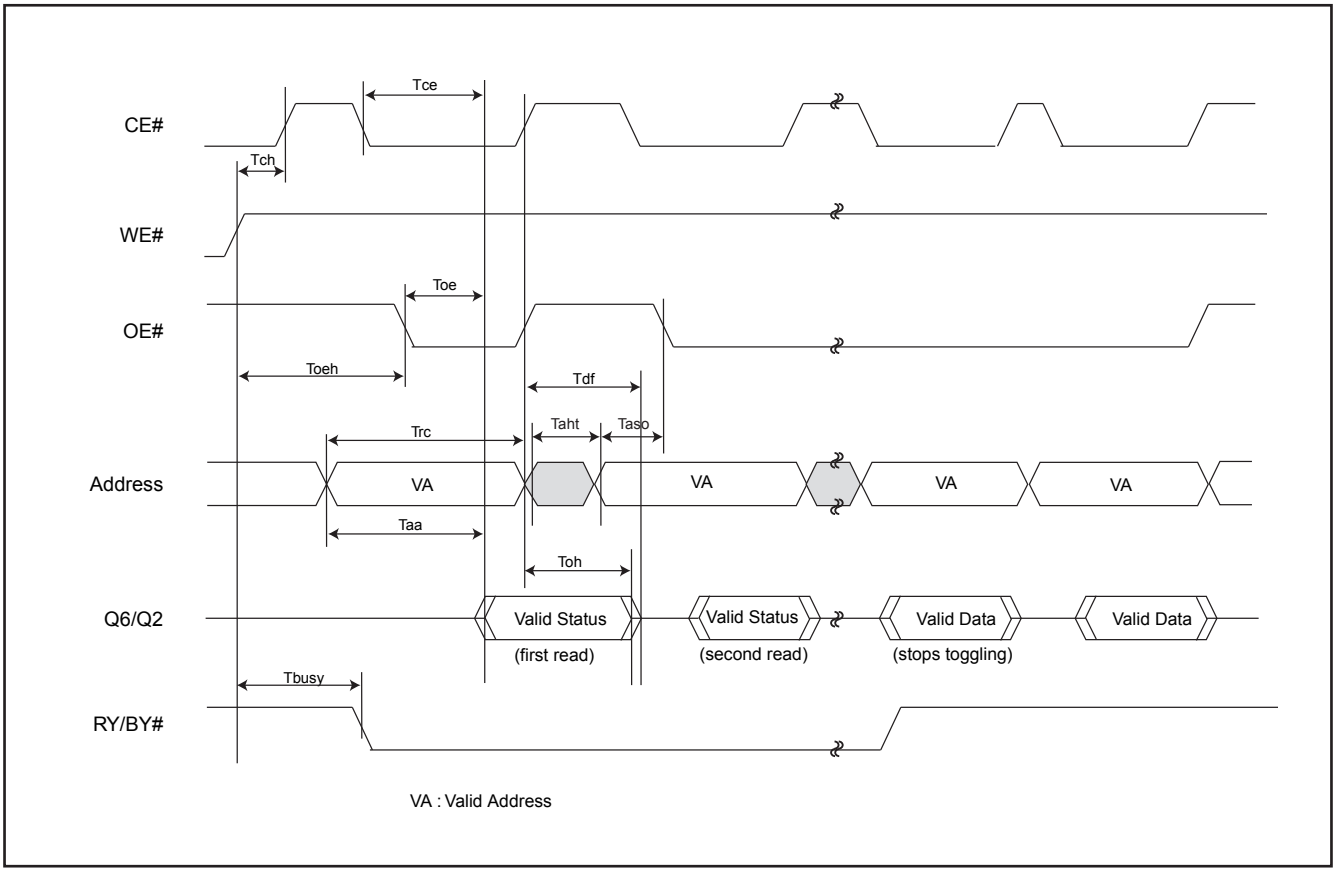
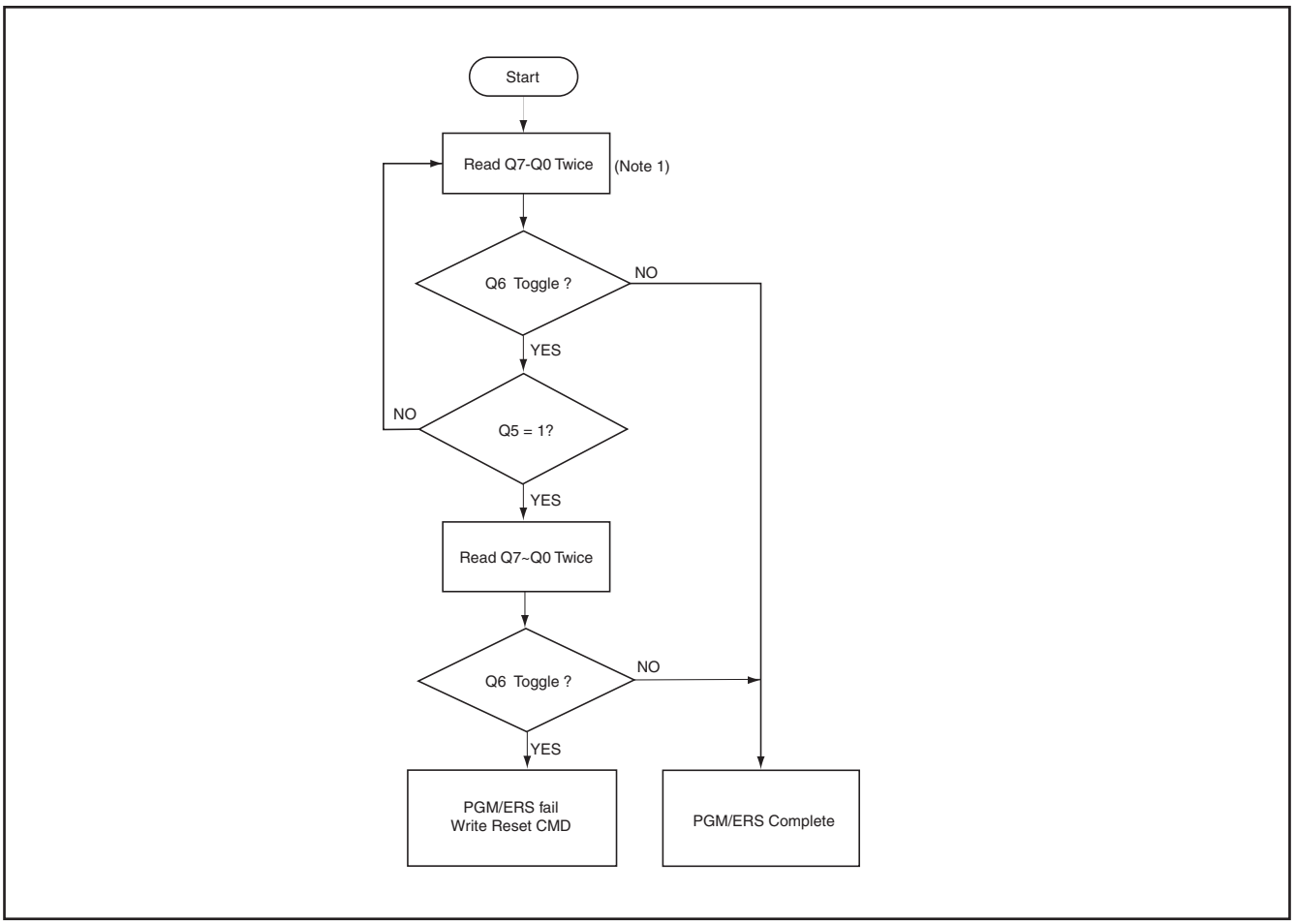
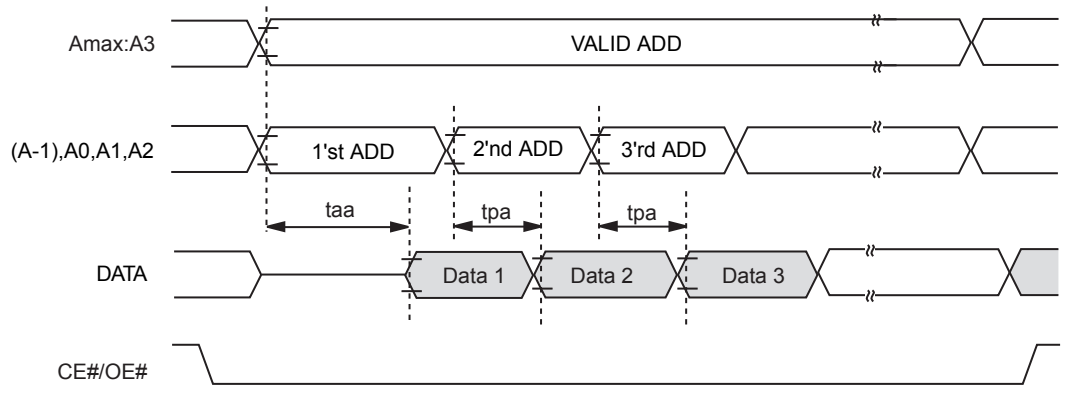


Figure 18. TOGGLE BIT ALGORITHM



Notes:
1. Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as Q5 changes to "1".

Figure 19. PAGE READ TIMING WAVEFORM



Note: CE#, OE# are enable.
Page size is 8 words in 16-bit mode.
Address are A2~A0 for Word mode.

AC CHARACTERISTICS

ITEM		TYP.	MAX.
WEB high to release from deep power down mode	tRDP	100us	200us
WEB high to deep power down mode	tDP	10us	20us

Figure 20. DEEP POWER DOWN MODE WAVEFORM

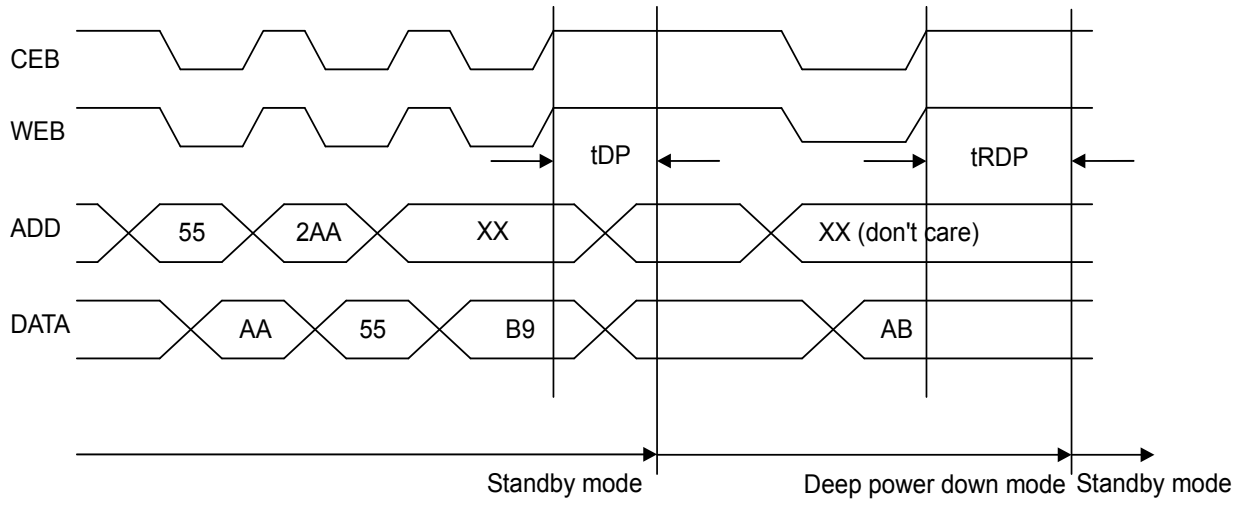
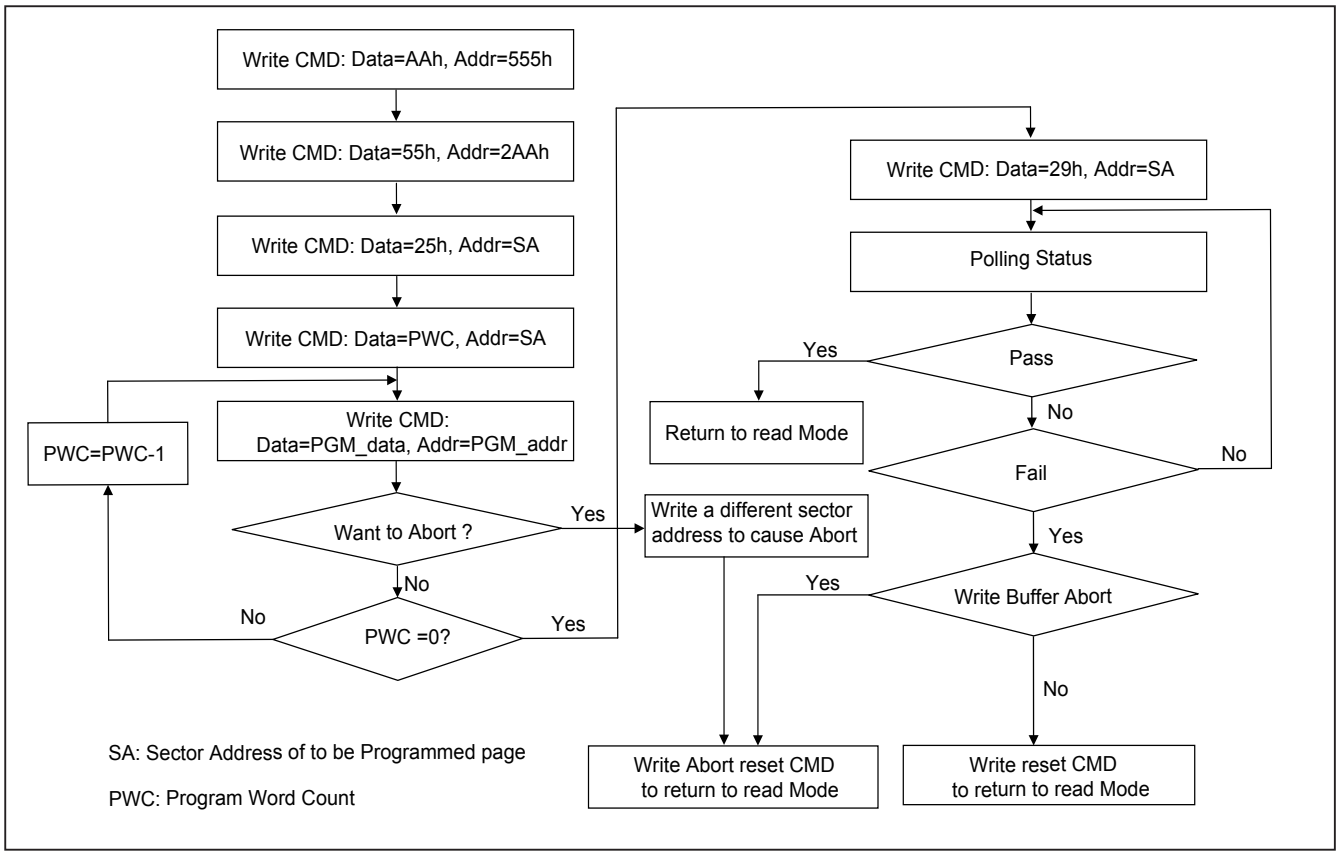


Figure 21. WRITE BUFFER PROGRAM FLOWCHART



RECOMMENDED OPERATING CONDITIONS

At Device Power-Up

AC timing illustrated in Figure A is recommended for the supply voltages and the control signals at device power-up (e.g. Vcc and CE# ramp up simultaneously). If the timing in the figure is ignored, the device may not operate correctly.

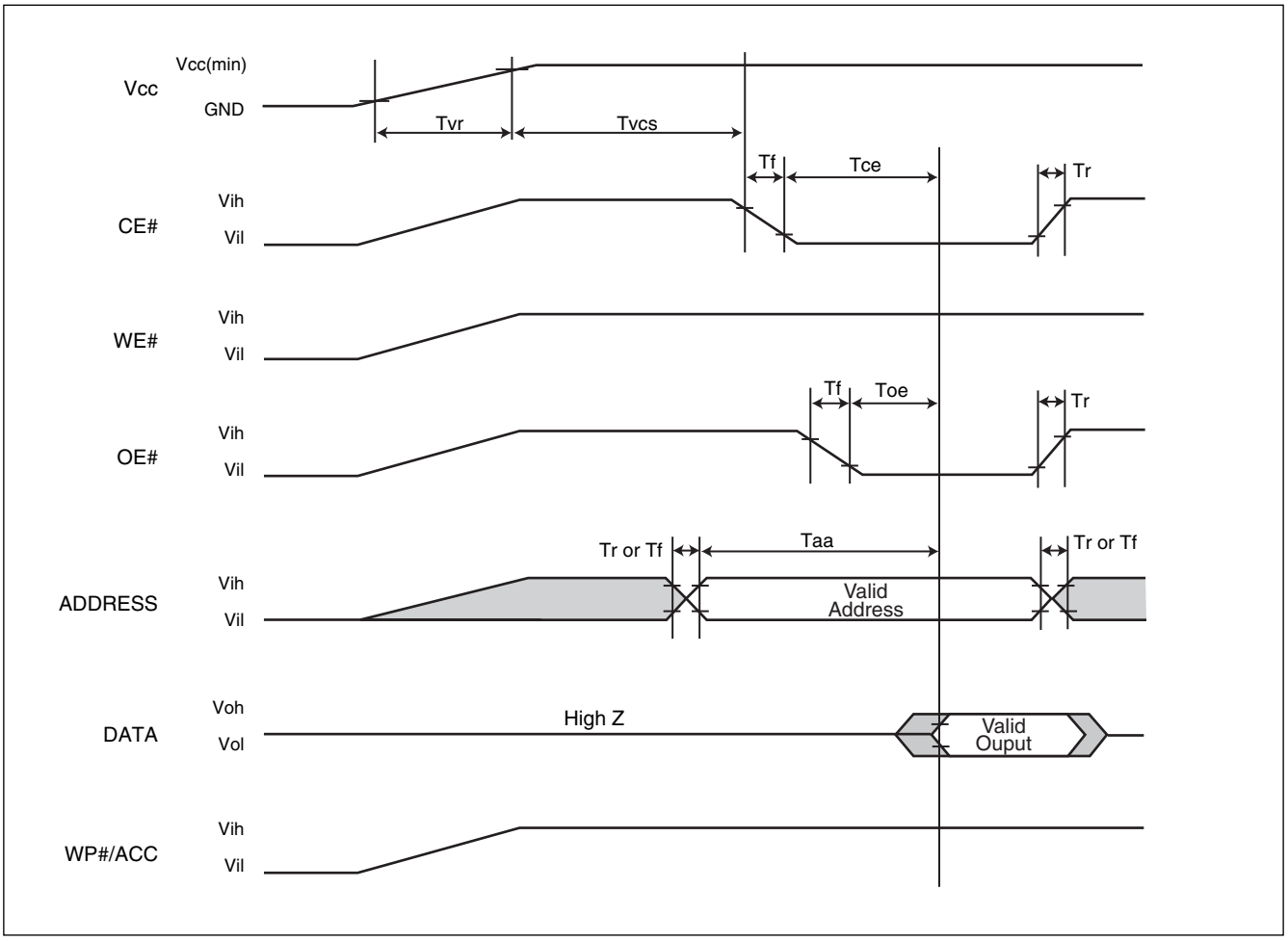


Figure A. AC Timing at Device Power-Up

Symbol	Parameter	Min.	Max.	Unit
Tvr	Vcc Rise Time	20	500000	us/V
Tr	Input Signal Rise Time		20	us/V
Tf	Input Signal Fall Time		20	us/V
Tvcs	Vcc Setup Time	500		us

Notes:
1. Not test 100%.

ERASE AND PROGRAMMING PERFORMANCE

Parameter		Limits			Units
		Min.	Typ. (1)	Max. (2)	
Chip Erase Time			256	600	sec
Sector Erase Time			0.6	5	sec
Chip Programming Time			200	700	sec
Word Program Time			11	360	us
Total Write Buffer Time	EPN for 10Q		120		us
	EPN for 11G		70		us
ACC Total Write Buffer Time	EPN for 10Q		100		us
	EPN for 11G		70		us
Erase/Program Cycles		100,000			Cycles

Notes:
1. Typical program and erase times assume the following conditions: 25°C, 3.0V VCC. Programming specifications assume checkboard data pattern.
2. Maximum values are measured at VCC = 3.0 V, worst case temperature. Maximum values are valid up to and including 100,000 program/erase cycles.
3. Exclude 00h program to all bits before erase operation.

DATA RETENTION

Parameter	Condition	Min.	Max.	Unit
Data retention	55˚C	20		years

LATCH-UP CHARACTERISTICS

	Min.	Max.
Input Voltage voltage difference with GND on WP#/ACC, A9	-1.0V	10.5V
Input Voltage voltage difference with GND on all normal pins input	-1.0V	1.5Vcc
Vcc Current	-100mA	+100mA
All pins included except Vcc. Test conditions: Vcc = 3.0V, one pin per testing		

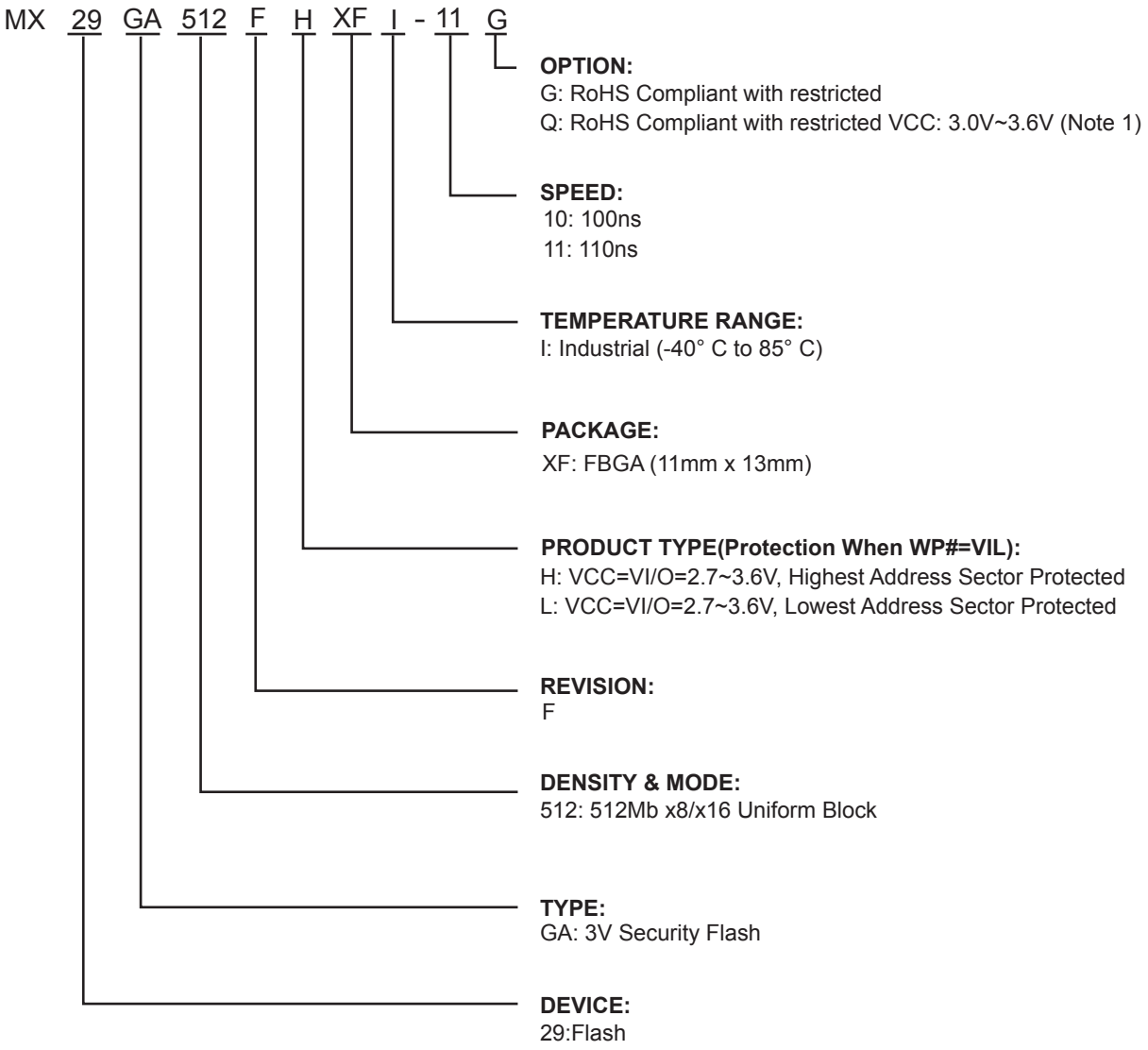
PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Set	Typ.	Max.	Unit
CIN2	Control Pin Capacitance	VIN=0	7.5	35	pF
COUT	Output Capacitance	VOUT=0	8.5	12	pF
CIN	Input Capacitance	VIN=0	6	7.5	pF

ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	PACKAGE	Remark
MX29GA512FHXFI-10Q	100	64 FBGA	Slow Total Write Buffer Time
MX29GA512FLXFI-10Q	100	64 FBGA	Slow Total Write Buffer Time
MX29GA512FHXFI-11G	110	64 FBGA	Fast Total Write Buffer Time
MX29GA512FLXFI-11G	110	64 FBGA	Fast Total Write Buffer Time

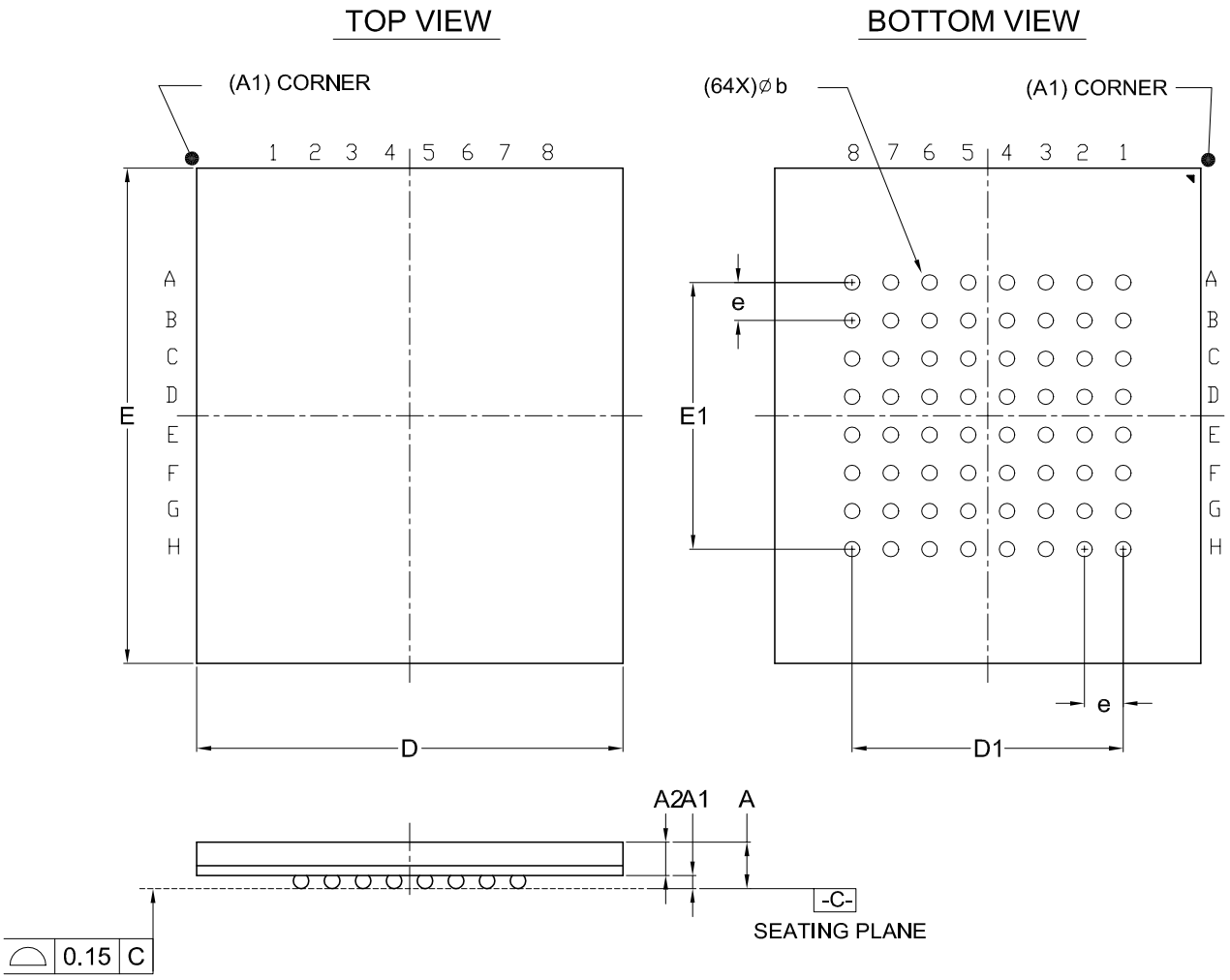
PART NAME DESCRIPTION



Note 1: 10Q covers 2.7V~3.6V for 110ns and 3.0V~3.6V for 100ns

PACKAGE INFORMATION

Doc. Title: Package Outline for CSP 64BALL(11X13X1.4MM,BALL PITCH 1.00MM,BALL DIAMETER 0.6MM)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	--	0.40	0.65	0.50	10.90		12.90		
	Nom.	--	0.50	---	0.60	11.00	7.00	13.00	7.00	1.00
	Max.	1.40	0.60	---	0.70	11.10		13.10		
Inch	Min.	--	0.016	0.026	0.020	0.429		0.508		
	Nom.	--	0.020	---	0.024	0.433	0.276	0.512	0.276	0.039
	Max.	0.055	0.024	---	0.028	0.437		0.516		

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-4247	1	MO-192			

REVISION HISTORY

Revision No.	Description	Page	Date
1.0	1. Removed the title "Advanced Information"	P5	JUL/11/2011
	2. Modified Figure 16. Status Polling For Write Buffer Program for Abort function	P13,46	
	3. Modified Total Write Buffer Time from 200us(typ.) to 120us(typ.)	P52	
1.1	1. Modified Total Write Buffer Time & ACC Total Write Buffer Time	P52	JUN/28/2012
	2. Modified Ordering Information & Part Name Description	P53,54	

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