

2N6905 SERIES

N-Channel JFET Pairs

T-27-27

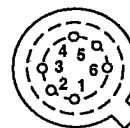
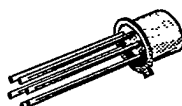
The 2N6905 Series of high-performance monolithic dual JFETs features extremely low noise, tight offset voltage and drift over temperature specifications. It is targeted for use in a wide range of precision instrumentation applications. The 2N6905 Series has a wide selection of both offset and drift ranges with the prime device, the 2N6905, featuring 5 mV offset and 10 $\mu\text{V}/^\circ\text{C}$ drift. The three devices allow designers to make important cost/benefit decisions. This series is available in a TO-71 hermetically sealed package and is available with military screening. (See Section 1.)

For additional design information please see performance curves NNR, which are located in Section 7.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$ V_{GS1} - V_{GS2} $ MAX (mV)
2N6905	-35	2	-5	5
2N6906	-35	2	-5	10
2N6907	-35	2	-5	25

TO-71

BOTTOM VIEW



- 1 SOURCE 1
- 2 DRAIN 1
- 3 GATE 1
- 4 SOURCE 2
- 5 DRAIN 2
- 6 GATE 2

SIMILAR PRODUCTS

- High-Gain, See 2N5911 Series
- SO-8, See SST404 Series
- Chips, Order 2N690XCHP

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT	UNITS
Gate-Drain Voltage		V_{GD}	-35	V
Gate-Source Voltage		V_{GS}	-35	
Forward Gate Current		I_G	10	mA
Power Dissipation	Per Side	P_D	300	mW
	Total		500	
Power Derating	Per Side		2.6	mW/ $^\circ\text{C}$
	Total		5	
Operating Junction Temperature		T_J	-55 to 150	$^\circ\text{C}$
Storage Temperature		T_{stg}	-65 to 200	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	



2N6905 SERIES

T-27-27

ELECTRICAL CHARACTERISTICS ¹				LIMITS						
PARAMETER	SYMBOL	TEST CONDITIONS	TYP ²	2N6905		2N6906		2N6907		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
STATIC										
Gate-Source Breakdown Voltage	V _{(BR)GSS}	I _G = -1 μA, V _{DS} = 0 V	-55	-35		-35		-35		V
Gate-Source Cutoff Voltage	V _{GS(OFF)}	V _{DS} = 15 V, I _D = 1 nA	-1.5	-0.2	-3	-0.2	-3	-0.2	-3	
Saturation Drain Current ³	I _{DSS}	V _{DS} = 10 V, V _{GS} = 0 V	3.5	0.5	10	0.5	10	0.5	10	mA
Gate Reverse Current	I _{GSS}	V _{GS} = -15 V	-2		-15		-15		-15	pA
		V _{DS} = 0 V T _A = 125°C	-1							nA
Gate Operating Current	I _G	V _{DG} = 15 V	-2		-5		-5		-5	pA
		I _D = 200 μA T _A = 125°C	-0.8		-5		-5		-5	nA
Drain-Source On-Resistance ⁴	r _{DS(ON)}	V _{GS} = 0 V, I _D = 0.1 mA	250							Ω
Gate-Source Voltage	V _{GS}	V _{DG} = 15 V, I _D = 200 μA	-1		-2.3		-2.3		-2.3	V
Gate-Source Forward Voltage ⁴	V _{GS(F)}	I _G = 1 mA, V _{DS} = 0 V	0.7							
DYNAMIC										
Common-Source Forward Transconductance	g _{fs}	V _{DS} = 10 V, V _{GS} = 0 V f = 1 kHz	4	2	7	2	7	2	7	mS
Common-Source Output Conductance	g _{os}		4		20		20		20	μS
Common-Source Input Capacitance	C _{iss}	V _{DG} = 15 V, I _D = 200 μA f = 1 MHz	4		8		8		8	pF
Common-Source Reverse Transfer Capacitance	C _{rss}		1.5		3		3		3	
Equivalent Input Noise Voltage	e _n	V _{DS} = 10 V, V _{GS} = 0 V f = 10 Hz	10		15		15		15	nV/√Hz
MATCHING										
Differential Gate-Source Voltage	V _{GS1} - V _{GS2}	V _{DG} = 10 V, I _D = 200 μA			5		10		25	mV
Gate-Source Voltage Differential Change with Temperature	Δ V _{GS1} - V _{GS2} ΔT	V _{DG} = 10 V			10		25		25	μV/°C
		I _D = 200 μA			10		25		50	
Saturation Drain Current Ratio ⁴	I _{DSS1} I _{DSS2}	V _{DS} = 10 V, V _{GS} = 0 V	0.97							
Transconductance Ratio ⁴	g _{fs1} g _{fs2}	V _{DG} = 10 V, I _D = 0.2 mA f = 1 kHz	0.97							
Differential Output Conductance ⁴	g _{os1} - g _{os2}		0.1							μS
Differential Gate Current ⁴	I _{G1} - I _{G2}	V _{DG} = 15 V, I _D = 0.2 mA T _A = 25°C	1							pA
Common Mode Rejection Ratio	CMRR	V _{DG} = 10 to 20 V, I _D = 200 μA	102	95		95		95		dB

- NOTES: 1. $T_A = 25^\circ C$ unless otherwise noted.
 2. For design aid only, not subject to production testing.
 3. Pulse test; PW = 300 μs , duty cycle $\leq 3\%$.
 4. This parameter not registered with JEDEC.

4