# SONET/SDH CLOCK RECOVERY AND SYNTHESIS UNIT S3014

## FEATURES

- Complies with ANSI, Bellcore, and CCITT specifications for jitter tolerance
- On-chip high frequency PLL with internal loop filter for clock generation or clock recovery
- Supports clock generation for STS-3/STM-1 (155.52 MHz)
- Supports clock recovery for STS-3/STM-1 (155.52 Mbit/s) or STS-12/STM-4 (622.08 Mbit/s) NRZ data
- Selectable 19.44 MHz, 51.84 MHz, or 155.52 MHz reference frequency
- Lock detect—monitors transition density and run length
- Low power
- Low-jitter ECL interface
- Small 44 PLCC or CLCC package
- TTL reference clock output

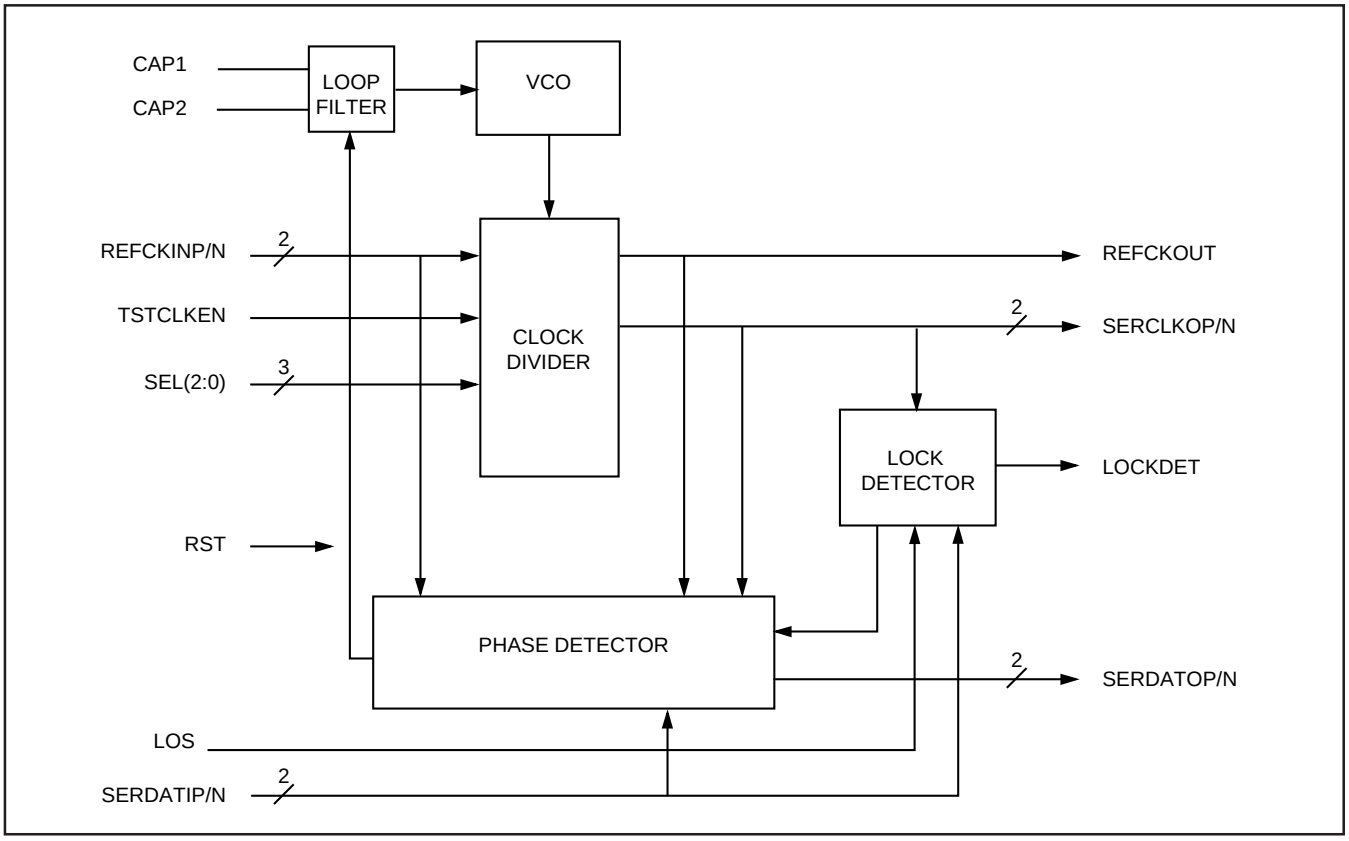
## GENERAL DESCRIPTION

The function of the S3014 clock synthesis and recovery unit is to derive high speed timing signals for SONET/SDH-based equipment. The S3014 is implemented using AMCC's proven Phase Locked Loop (PLL) technology.

In Clock Recovery mode, the S3014 receives either an STS-3/STM-1 or STS-12/STM-4 scrambled NRZ signal and recovers the clock from the data. The chip outputs a differential ECL bit clock and retimed data. In Clock Synthesis mode, the S3014 receives a 19.44, 51.84, or 155.52 MHz reference clock and outputs an STS-3/STM-1 or STS-12/STM-4 differential ECL clock.

The S3014 utilizes an on-chip PLL which consists of a phase detector, a loop filter, and a voltage controlled oscillator (VCO). The phase detector compares the phase relationship between the VCO output and the REFCLK input, a loop filter converts the phase detector output into a smooth DC voltage, and the DC voltage is input to the VCO whose frequency is varied by this voltage. A block diagram is shown in Figure 1.

***Figure 1. System Block Diagram***



## S3014 OVERVIEW

### Clock Recovery Mode

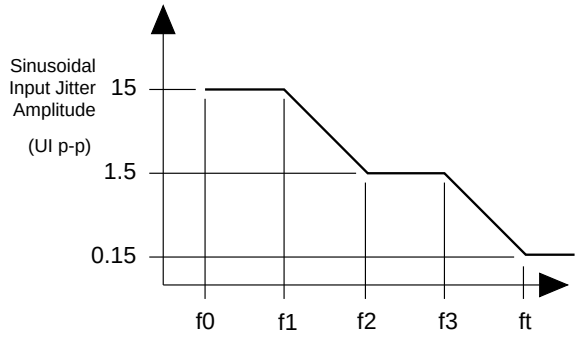
In the Clock Recovery mode, the S3014 supports clock recovery for the STS-3/STM-1 and STS-12/STM-4 rates. In this mode, ECL differential serial data is input to the chip at the rate specified by the three SEL pins, and clock recovery is performed on the incoming data stream. An external ECL differential reference clock (19.44, 51.84, or 155.52 MHz) is required to minimize the PLL lock time and provide a stable output clock source in the absence of serial input data. Retimed data and clock are output from the S3014.

### Clock Synthesis Mode

In the Clock Synthesis mode, the S3014 synthesizes up to the STS-3/STM-1 and STS-12/STM-4 clock rates from either a 19.44 MHz, 51.84 MHz, or 155.52 MHz input reference frequency. STS-3/STM-1 jitter generation is compliant with the SONET/SDH requirement for 0.01 U.I. (rms) maximum, given 14.1 ps (rms) jitter on REFCLK in the 12 KHz to 1 MHz frequency band.

In this mode, a crystal oscillator is connected to the ECL differential reference input and synthesized up to the output frequency selected using the three SEL pins. The Clock Synthesis mode is recognized by the absence of data on the SERDATIP/N input pins. In this mode, tie the SERDATIP pin to ground and tie the SERDATIN pin to VTT (-2.0v) or to an ECL low level. A programmable internal divider outputs a TTL clock at the same frequency as the reference clock input via the REFCKOUT output. The lock detect output will remain consistently low in the Clock Synthesis mode.

***Figure 2. Input Jitter Tolerance Specification***




| OC/STS Level | f0 (Hz) | f1 (Hz) | f2 (Hz) | f3 (kHz) | ft (kHz) |
|---|---|---|---|---|---|
| 3 | 10 | 30 | 300 | 6.5 | 75 |
| 12 | 10 | 30 | 300 | 25 | 250 |

## CHARACTERISTICS

### Performance

The S3014 PLL complies with the minimum jitter tolerance for clock recovery proposed for SONET/SDH equipment defined by the T1X1.6/91-022 document, when used with differential inputs and outputs as shown in Figure 2.

### Input Jitter Tolerance

Input jitter tolerance is defined as the peak to peak amplitude of sinusoidal jitter applied on the input signal that causes an equivalent 1 dB optical/electrical power penalty. SONET input jitter tolerance requirements are shown in Figure 2. The measurement condition is the input jitter amplitude which causes an equivalent of 1 dB power penalty.

### Jitter Generation

Jitter generation is defined as the amount of jitter at the OC-N/STS-N output of a SONET equipment.

Jitter generation shall not exceed 0.01 UI rms in OC-3 mode and 0.03 UI rms in OC-12 mode when measured using a highpass filter with a 12 kHz cutoff frequency.

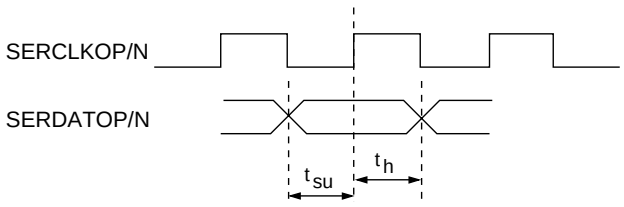
### Serial Data Output Set-up and Hold Time

The output set-up and hold times are represented by the waveforms shown in Figure 3.

### Reference Clock Input

The required characteristics of the reference clock are outlined below. Unless otherwise noted, specifications refer to both Clock Recovery and Clock Synthesis modes of operation. While a single-ended ECL reference clock may be used, additional jitter due to edge movement related to threshold variations from DC offsets may be induced.

***Figure 3. Clock Output to Data Transition Delay***




| | Output Frequency | |
|---|---|---|
| | 155.52 MHz | 622.08 MHz |
| SERDATOP/N Setup Time | 2.5 ns | 450 ps |
| SERDATOP/N Hold Time | 2.5 ns | 650 ps |

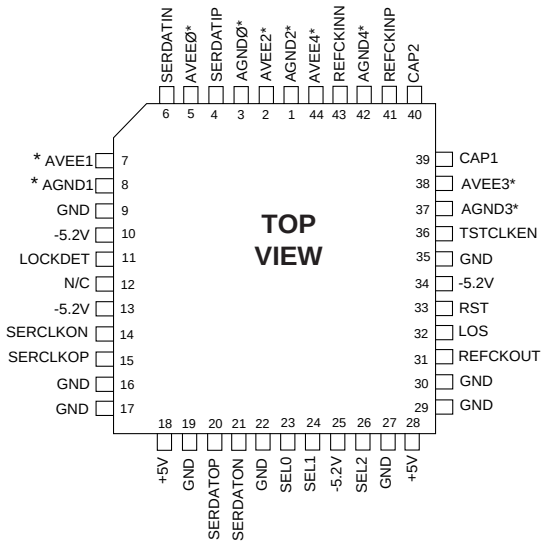
***Pin Assignment and Descriptions***

| Pin Name | Level | I/O | Pin # | Description |
|---|---|---|---|---|
| REFCKINP<br>REFCKINN | Diff.<br>ECL | I | 41<br>43 | Reference clock. Input used as the reference for the internal bit clock in frequency synthesis mode. Used as standby clock in the absence of data or during reset in clock recovery mode. |
| SERDATIP<br>SERDATIN | Diff.<br>ECL | I | 4<br>6 | Serial data in. When the S3014 is used in the Clock Recovery mode, clock is recovered from the transitions on these inputs. |
| TSTCLKEN | TTL | I | 36 | Test clock enable, active high. Used during production test to bypass the VCO in the PLL. Tie to ground for normal operation. |
| SEL2<br>SEL1<br>SEL0 | TTL | I | 26<br>24<br>23 | Mode select, used to select output and input frequencies. Refer to Table 1 for explanation. |
| RST | TTL | I | 33 | Reset, active low. Initializes the device to a known state and forces the PLL to acquire to the reference clock. RST, when held low, also forces the REFCKOUT and LOCKDET outputs to the Hi-Z state. A reset of at least 16 ms should be applied at power-up and whenever it is necessary to reacquire to the reference clock. The S3014 will also reacquire to the reference clock if the serial data is held quiescent (constant ones or constant zeros) for at least 16 ms. |
| LOS | ECL | I | 32 | Loss of signal, active low. A single-ended 10K ECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When LOS is low, the data on the Serial Data In (SERDATIP/N) pins will be internally forced to a constant zero, LOCKDET forced low, and the PLL forced to lock to the REFCKINP/N inputs. This signal must be used to assure correct automatic reacquisition to serial data following an interruption and subsequent reconnection of the optical path. This will assure that the PLL does not "wander" out of reacquisition range by tracking the random phase/frequency content of the optical detector's noise floor while monitoring "dark" fiber. When LOS is high, data on the SERDATIP/N pins will be processed normally. |
| CAP1, CAP2 | – | I | 39<br>40 | Loop filter capacitor, connected to these pins. The capacitor value should be 0.1 µf ±10% tolerance, X7R dielectric ceramic chip capacitor. 50V is recommended. |
| LOCKDET | TTL | O | 11 | Lock detect, active high. Clock recovery indicator. Set high when the internal clock recovery has locked onto the incoming datastream. LOCKDET is an asynchronous output. This output is deasserted when there is no incoming serial data input; in which case the PLL locks to the reference clock. |

***Pin Assignment and Descriptions (Continued)***

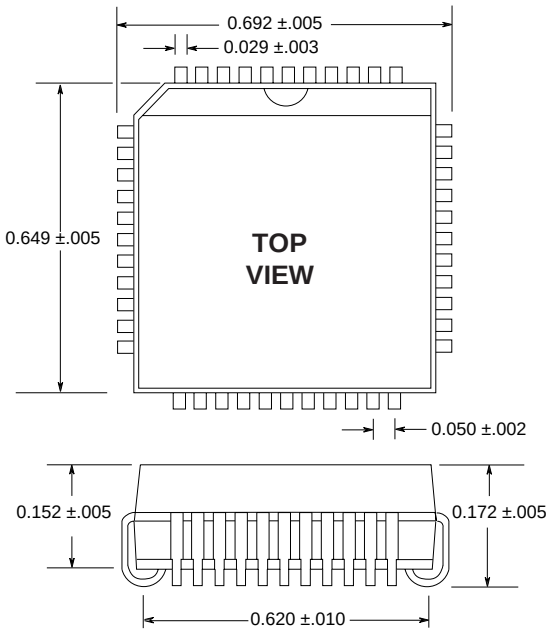
| Pin Name | Level | I/O | Pin # | Description |
|---|---|---|---|---|
| SERDATOP<br>SERDATON | Diff.<br>ECL | O | 20<br>21 | Serial data out signal. In the Clock Recovery mode, this signal is the delayed version of the incoming data stream (SERDATI) updated on the falling edge of Serial Clock Out (SERCLKOP). |
| SERCLKOP<br>SERCLKON | Diff.<br>ECL | O | 15<br>14 | Serial clock out signal that is phase aligned with Serial Data Out (SERDATO) when Lock Detect (LOCKDET) is high. When Lock Detect is low, the signal is synchronous with Reference Clock (REFCKINP/N). |
| REFCKOUT | TTL | O | 31 | Single-ended TTL reference clock output. See Table 1. |
| AVEE | -5.2V | – | 2, 5, 7, 38, 44 | Analog power (-5.2V) |
| AGND | GND | – | 1, 3, 8, 37, 42 | Analog ground (0V) |
| GND | GND | – | 9, 16, 17, 19, 22, 27, 29, 30, 35 | Ground |
| -5.2V | -5.2V | – | 10, 13, 25, 34 | -5.2V |
| +5V | +5V | – | 18, 28 | +5V |
| NC | – | – | 12 | No Connection |

***Figure 4. 44 PLCC Pinout***




* Analog Power & GND
AVEE = -5.2V
AGND = 0V

***Figure 5. 44 PLCC Package***




All dimensions nominal in inches

***Performance Specifications***

| Parameter | Min | Typ | Max | Units | Condition |
|---|---|---|---|---|---|
| Nominal VCO Center Frequency | | 622.08 | | MHz | Given REFCLK = SERCLK ÷ 4, 12 or SERCLK ÷ 32 per SEL <2:0> settings |
| Clock Synthesis Output Jitter | | | | | In CSU mode, given : |
| OC-3/STS-3 | | .005 | .01<br>64 | UI(rms)<br>ps (rms) | • 56ps rms jitter on REFCLK in 12 KHz to 1 MHz band |
| OC-12/STS-12 [1] | | .015 | .03<br>48 | UI(rms)<br>ps (rms) | • 14.1 ps rms jitter on REFCLK in 12 KHz to 1 MHz band |
| Clock Recovery Output Jitter | | | .01 | UI(rms) | rms jitter, in lock |
| Reference Clock Frequency Tolerance [2,3] | | | | | Required to meet SONET output frequency specification |
| Clock Synthesis | -20 | | 20 | ppm | |
| Clock Recovery | -100 | | 100 | ppm | |
| OC-3/STS-3<br>OC-12/STS-12 | | | | | |
| Capture Range | | ±200 | | ppm | With respect to fixed reference frequency |
| Lock Range | | +8,-12 | | % | |
| Clock Output Duty Cycle | 45 | | 55 | % | Minimum transition density of 20% |
| Acquisition Lock Time [3]<br>OC-3/STS-3<br>OC-12/STS-12 | | | 64<br>16 | µsec | With device already powered up and valid REFCLK. |
| Reference Clock Input Duty Cycle | 30 | | 70 | % of period | |
| Reference Clock Rise & Fall Times | | | 2.0 | ns | 10% to 90% of amplitude |
| ECL Output Rise & Fall Times | | | 850 | ps | 10% to 90%, 50Ω to -2V equivalent load, 5 pf cap |

1. These specs can be achieved with either a 51.84 MHz or a 155.52 MHz Reference Clock.
2. Noise on REFCLK should be less than 14.1 ps rms in a jitter frequency band from 12 KHz to 1 MHz.
3. Specifications based on design values. Not tested.

***Table 1. Mode Select***

| SEL2 | SEL1 | SEL0 | SERCLKO | REFCKOUT | REFCKIN |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 622.08 MHz | 51.84 MHz | 51.84 MHz |
| 0 | 0 | 1 | 622.08 MHz | 19.44 MHz | 19.44 MHz |
| 0 | 1 | 0 | 622.08 MHz | 19.44 MHz | 19.44 MHz |
| 0 | 1 | 1 | 622.08 MHz | — | 155.52 MHz |
| 1 | 0 | 0 | 155.52 MHz | 51.84 MHz | 51.84 MHz |
| 1 | 0 | 1 | 155.52 MHz | 19.44 MHz | 19.44 MHz |

### *Absolute Maximum Ratings*

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Case Temperature under Bias | -55 | | 125 | °C |
| Junction Temperature under Bias | -55 | | 150 | °C |
| Storage Temperature | -65 | | 150 | °C |
| Voltage on VCC with Respect to GND | -0.5 | | 7.0 | V |
| Voltage on VEE with Respect to GND | -8.0 | | 0.5 | V |
| Voltage on Any TTL Input Pin | -0.5 | | +5.5 | V |
| Voltage on Any ECL Input Pin | -3.0 | | 0.0 | V |
| TTL Output Sink Current | | | 20 | mA |
| TTL Output Source Current | | | 10 | mA |
| High Speed ECL Output Source Current | | | 50 | mA |
| Static Discharge Voltage | | 500 | | V |

### *Recommended Operating Conditions*

| Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Ambient Temperature under Bias (industrial) | | -40 | | 85 | °C |
| Ambient Temperature under Bias (commercial) | | 0 | | 70 | °C |
| Junction Temperature under Bias | | -10 | | 130 | °C |
| Voltage on VCC with Respect to GND | | 4.75 | 5.0 | 5.25 | V |
| Voltage on VEE with Respect to GND | | -4.2 | -4.5/-5.2 | -5.46 | V |
| Voltage on Any TTL Input Pin | | 0.0 | | VCC | V |
| Voltage on Any ECL Input Pin | | -2.0 | | 0 | V |
| TTL/CMOS Output Sink Current | | | | 8 | mA |
| TTL/CMOS Output Source Current | | | | 1 | mA |
| ECL Output Source Current (50Ω to -2V) | | | 14 | 25 | mA |
| Supply Current | ICC | | 10 | 17 | mA |
| | IEE | | 170 | 210 | mA |

$V_{EE}$(min) = -4.2V for Ambient Temperature ≥ 0˚C, -4.5V for Ambient Temperature <0˚C.

### *TTL Input/Output DC Characteristics*[1]

($T_A$ = -40°C to +85°C, $V_{CC}$ = 5 V ±5%, $V_{EE}$ = -4.5 V ±7% or -5.2 ± 5%)

| Symbol | Parameter | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IL}$[2] | Input LOW Voltage | Guaranteed Input LOW Voltage for all inputs | | 0.8 | Volts |
| $V_{IH}$[2] | Input HIGH Voltage | Guaranteed Input HIGH Voltage for all inputs | 2.0 | | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.5V | -400.0 | | uA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = 2.7V | | 50.0 | uA |
| $I_I$ | Input HIGH Current at Max VCC | $V_{CC}$ = MAX, $V_{IN}$ = 5.25V | | 1.0 | mA |
| $I_{OS}$ | Output Short Circuit Current | $V_{CC}$ = MAX, $V_{OUT}$ = 0.5V | -100.0 | -25.0 | mA |
| $V_{IK}$ | Input Clamp Diode Voltage | $V_{CC}$ = MIN, $I_{IN}$ = -18.0mA | -1.2 | | Volts |
| $V_{OL}$ | TTL Output LOW Voltage | $V_{CC}$ = MIN, $I_{OL}$ = 8mA | | 0.5 | Volts |
| $V_{OH}$ | TTL Output HIGH Voltage | $V_{CC}$ = MIN, $I_{OH}$ = -1.0mA | 2.4 | | Volts |

1. These conditions will be met with an airflow of 400 LFPM.
2. These input levels provide a zero–noise immunity and should only be tested in a static, noise-free environment.

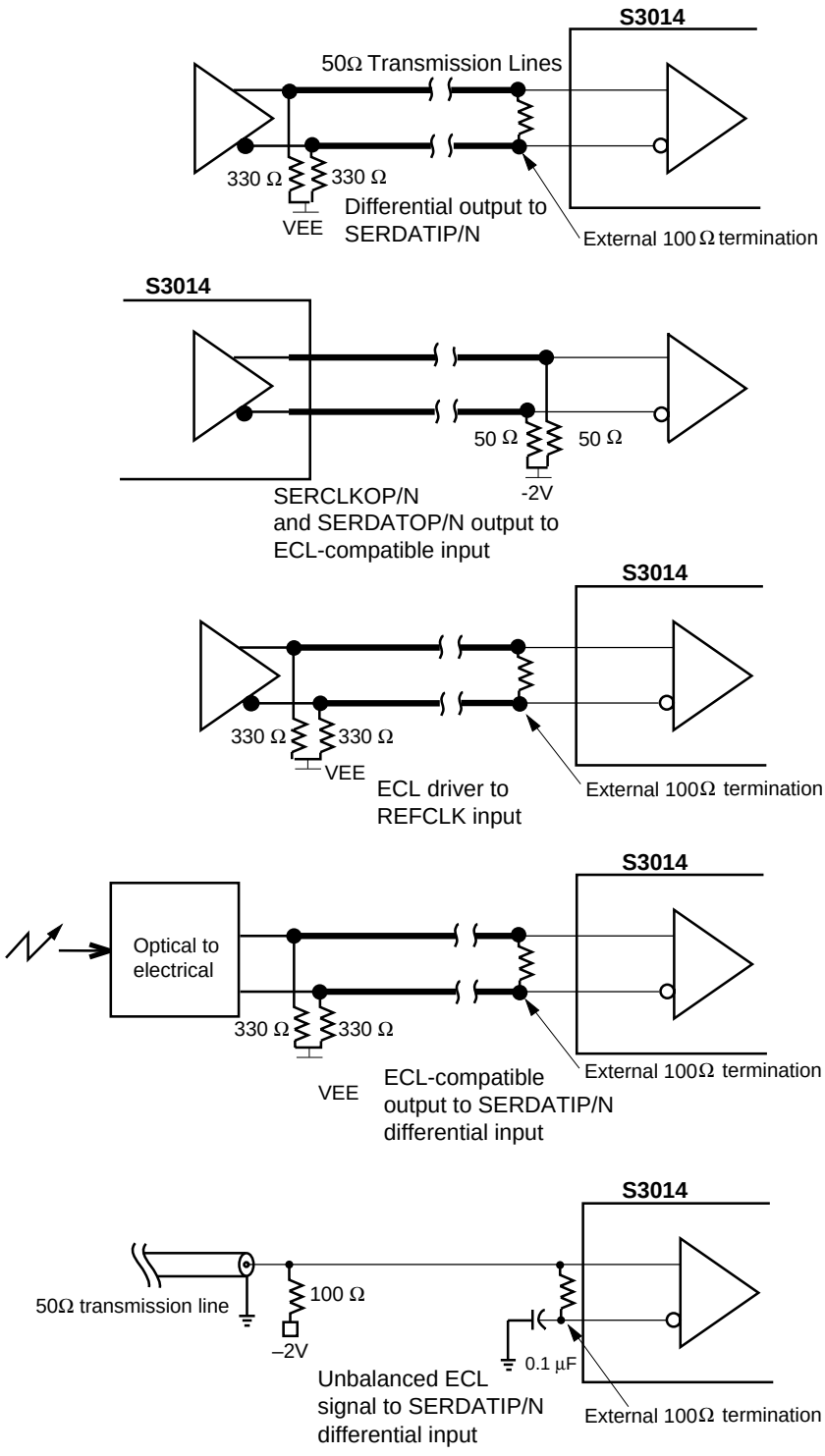
### *ECL Input/Output DC Characteristics*[3]

($T_A$ = -40°C to +85°C, $V_{CC}$ = 5 V ±5%, $V_{EE}$ = -4.5 V ±7% or -5.2 ± 5%)

| Symbol | Parameter | Test Conditions | Signal Name | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$[1] | Input LOW Voltage | Guaranteed Input LOW Voltage for all single ended inputs | | -2.00 | -1.47 | Volts |
| $V_{IH}$[1] | Input HIGH Voltage | Guaranteed Input HIGH Voltage for all single ended inputs | | -1.18 | -0.80 | Volts |
| $V_{IL}$[2] | Input LOW Voltage | Guaranteed Input LOW Voltage for all differential inputs | | -2.00 | -0.70 | Volts |
| $V_{IH}$[2] | Input HIGH Voltage | Guaranteed Input HIGH Voltage for all differential inputs | | -1.75 | -0.45 | Volts |
| $V_{ID}$[2,4] | Input DIFF Voltage | Guaranteed Input DIFF Voltage for all differential inputs | | 0.25 | 1.40 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{EE}$ = MAX, $V_{IL}$ = -1.95V | LOS | -0.50 | 20.00 | uA |
| | | $V_{EE}$ = MAX, $V_{DIFF}$ = 0.5V | SERDATIP,SERDATIN, REFCLKP, REFCLKN | -1.0 | 20.00 | uA |
| $I_{IH}$ | Input HIGH Current | $V_{EE}$ = MAX, $V_{IH}$ = -0.80V | LOS | -0.50 | 20.00 | uA |
| | | $V_{EE}$ = MAX, $V_{DIFF}$ = 0.5V | SERDATIP,SERDATIN, REFCLKP, REFCLKN | -1.0 | 20.00 | uA |
| $V_{OL}$ | Output LOW Voltage | 50Ω to -2V termination | | -2.00 | -1.50 | Volts |
| $V_{OH}$ | Output HIGH Voltage | 50Ω to -2V termination | | -1.11 | -0.62 | Volts |

1. Single Ended Inputs
2. Differential ECL Inputs
3. These conditions will be met with an airflow of 400 LFPM.
4. When not used, tie the negative differential input to ground (OV), and tie the positive differential input to -2.0V.

***Figure 6. Differential ECL Input and Output Applications***



***Ordering Information***

| GRADE | PART | PACKAGE | SPEED GRADE |
|---|---|---|---|
| S-commercial/<br>Industrial | 3014 | A-44 PLCC (com only)<br>D-44 PLCC TEP | 1 – 155 Mbit/s<br>6 – 622 Mbit/s |

| X | XXXX | X | - | X |
|---|---|---|---|---|
| Grade | Part number | Package | | Speed Grade |

ISO 9001 CERTIFIED

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