19-4134; Rev 6; 8/11

EVALUATION KIT AVAILABLE

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

MAX9979

## General Description

The MAX9979 fully integrated, high-performance, dual-channel pin electronics integrates multiple automatic test equipment (ATE) functions into a single IC, including driver/comparator/load (DCL), parametric measurement unit (PMU), and built-in (16-bit) level-setting digital-to-analog converters (DACs). The device is ideal for memory and SOC tester applications. Each channel includes a four-level pin driver, window comparator, differential comparator, dynamic clamps, a versatile PMU, an active load, a high-voltage (VHH) programmable level, and 14 independent level-setting DACs. The MAX9979 features programmable cable-droop compensation for the driver output and for the comparator input, adjustable driver output resistance that allows optimal performance over typical data-path transmission-line variations, slew-rate adjustment, and a programmable high-voltage driver output.

The MAX9979 driver features a wide 8V (-1.5V to +6.5V) high-speed operating voltage range and a VHH programmable range of up to +13V. Operation modes include high-impedance, active-termination (3rd-level drive) and VHH (4th-level drive) modes. The device is highly linear even at low voltage swings. The driver provides high-speed differential control inputs compatible with most high-speed logic families. The window comparators provide extremely low timing variation over changes in slew rate, pulse width, and overdrive voltage. In high-impedance mode, the MAX9979 features dynamic clamps that dampen high-speed device-under-test (DUT) waveforms. The 20mA active load facilitates fast contact testing when used in conjunction with the comparators, and functions as a pullup/pulldown for open-drain/collector DUT outputs. The PMU offers five current ranges from ±2µA to ±50mA and can force and measure current or voltage. An SPI™-compatible serial interface configures the MAX9979.

The MAX9979 is available in a small footprint, 68-pin (10mm x 10mm x 1mm) TQFN-EP-IDP package with exposed pad on the top for easy heat removal. Power dissipation is 1.2W per channel (typ) over the full operating voltage range with the active load disabled. The MAX9979 operates over an internal die temperature range of +40°C to +100°C and provides a temperature monitor output.

## Applications

Memory ATE Testers

SOC ATE Testers

## Features

- **High Speed: 1.1Gbps at $1V_{P-P}$**
- **Extremely Low Power Dissipation: 1.2W/Channel (Active Load Disabled)**
- **Wide Voltage Range: -1.5V to +6.5V and Up to 13V VHH**
- **Wide Voltage Swing Range: $50mV_{P-P}$ to $13V_{P-P}$**
- **Low-Leak Mode: 10nA max**
- **Integrated Termination-on-the-Fly (3rd-Level Drive)**
- **Integrated VHH High Voltage (4th-Level Drive)**
- **Integrated Voltage Clamps**
- **Integrated 20mA Active Load**
- **Integrated Per-Pin PMU**
- **Integrated Level-Setting CALDACs**
- **Programmable Cable-Droop Compensation for Both Driver Output and Comparator Input**
- **Programmable Driver Output Impedance**
- **Four Slew-Rate Settings for Driver Output**
- **Analog Measure Bus**
- **Very Low Timing Dispersion**
- **Minimal External Component Count**
- **SPI-Compatible Serial Control Interface**
- **68-Pin Thermally Enhanced TQFN Package with Top-Side Heat Removal**

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX9979KCTK+ | 0°C to +70°C | 68 TQFN-EP-IDP* |

*+Denotes a lead(Pb)-free/RoHS-compliant package.*

**EP-IDP = Exposed pad, inverted die pad.*

***Pin Configuration and Typical Operating Circuit appear at end of data sheet.***

*SPI is a trademark of Motorola, Inc.*

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

## ABSOLUTE MAXIMUM RATINGS

$V_{CC}$ to GND .....-0.3V to +11V
$V_{EE}$ to GND.....-5.5V to +0.3V
$V_{CC}$ to $V_{EE}$ .....-0.3V to +16.5V
$V_{DD}$ to DGND .....-0.3V to +5.2V
$V_{HHP}$ to GND .....-0.3V to +19V
DGND to GND .....±0.3V
CTV_, BV_ to GND.....-0.3V to +5V
DATA_, NDATA_, RCV_,
NRCV_ to GND.....($V_{EE}$ - 0.3V) to ($V_{BV\_}$ + 0.3V)
CH_, NCH_, CL_, NCL_ to GND.....-1.5V to ($V_{CTV\_}$ + 0.3V)
Current into CH_, NCH_, CL_, NCL_ .....±35mA
DATA_ to NDATA_, RCV_ to NRCV_ .....±1V
DUT_, PMU-F, PMU-S, SENSE_ to GND
(non-VHH mode) .....($V_{EE}$ - 0.3V) to ($V_{CC}$ + 0.3V)
DUT_, PMU-F, PMU-S, SENSE_ to GND
(VHH mode).....-3.5V to +13.5V
SCLK, DIN, $\overline{CS}$, $\overline{RST}$, $\overline{LOAD}$ to GND.....-0.3V to ($V_{DD}$ + 0.3V)
$\overline{LLEAKP\_}$, $\overline{HIZMEASP\_}$, $\overline{ENVHHP\_}$, DUTHI_,
DUTLO_, to GND.....-0.3V to ($V_{DD}$ + 0.3V)
TEMP to GND .....0 to $V_{CC}$
MEAS_ to GND.....($V_{EE}$ - 0.3V) to ($V_{CC}$ + 0.3V)
REF to GND.....-0.3V to (2.6V + $V_{DGS}$)
Current into SCLK, DIN, $\overline{CS}$, $\overline{RST}$, $\overline{LOAD}$ .....±30mA
Current into $\overline{LLEAKP\_}$, $\overline{HIZMEASP\_}$, $\overline{ENVHHP\_}$,
DUTHI_, DUTLO_ .....±30mA
PMU-F Continuous Current.....±35mA
PMU-F Peak Current.....±70mA
PMU-S Continuous Current .....±1mA
PMU-S Peak Current.....±20mA
DGS to GND .....±0.3V
DUT_, SENSE_ Short-Circuit
Duration to $V_{CC}$, $V_{EE}$ .....Continuous
Power Dissipation ($T_A$ = +70°C)*
MAX9979KCTK (derate 125mW/°C above +70°C).....10W
Storage Temperature Range .....-65°C to +150°C
Maximum Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

**Dissipation wattage values are based on still air with no heatsink. Actual maximum power dissipation is a function of heat extraction technique and may be substantially higher.*

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## PACKAGE THERMAL CHARACTERISTICS**

TQFN
Junction-to-Case Thermal Resistance ($\theta_{JA}$).....8.0°C/W
Junction-to-Ambient Thermal Resistance ($\theta_{JC}$).....0.3°C/W

***Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to* ***www.maxim-ic.com/thermal-tutorial****.*

## ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0V, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{CTV\_}$ = 1.4V, $V_{BV\_}$ = 4V, $V_{DGS}$ = $V_{GND}$ = 0V, $V_{CHV\_}$ = $V_{IVMAX\_}$ = 2V, $V_{CLV\_}$ = $V_{IVMIN\_}$ = 1V, $V_{COM\_}$ = 2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{IN\_}$ = 2.5V, $V_{VIOS}$ = 0V, $V_{IIOS}$ = 2.5V, $V_{CLAMPHI\_}$ = 5V, $V_{CLAMPLO\_}$ = 0V, $V_{HH\_}$ = 10V, CDRP = 0b001, RO = 0b1000, HYST = 0b000, $Z_{LOAD}$ = 50Ω, $T_J$ = +70°C to an accuracy of ±15°C, unless otherwise noted. All temperature coefficients are measured at $T_J$ = +40°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DRIVER** | | | | | | |
| **DC CHARACTERISTICS ($R_L$ ≥ 10MΩ, unless otherwise noted; includes DAC error)** | | | | | | |
| Output-Voltage Range | $V_{DHV}$ | $V_{DLV\_}$ = -1.5V, $V_{DTV\_}$ = 1.5V | -1.45 to +6.50 | | | V |
| | $V_{DLV}$ | $V_{DHV\_}$ = 6.5V, $V_{DTV\_}$ = 1.5V | -1.50 to +6.45 | | | |
| | $V_{DTV}$ | $V_{DHV\_}$ = 6.5V, $V_{DLV\_}$ = -1.5V (Note 2) | -1.50 | | +6.50 | |
| Output Offset Voltage | $V_{DHV}$ | $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = -1.5V, $V_{DTV\_}$ = 1.5V | | | ±5 | mV |
| | $V_{DLV}$ | $V_{DLV\_}$ = 0V, $V_{DHV\_}$ = 6.5V, $V_{DTV\_}$ = 1.5V | | | ±5 | |
| | $V_{DTV}$ | $V_{DTV\_}$ = 1.5V, $V_{DHV\_}$ = 6.5V, $V_{DLV\_}$ = -1.5V | | | ±5 | |
| Output-Voltage Temperature Coefficient (Notes 3, 4) | | DHV_, DLV_, DTV_ | | ±75 | ±500 | µV/°C |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0V, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{CTV\_}$ = 1.4V, $V_{BV\_}$ = 4V, $V_{DGS}$ = $V_{GND}$ = 0V, $V_{CHV\_}$ = $V_{IVMAX\_}$ = 2V, $V_{CLV\_}$ = $V_{IVMIN\_}$ = 1V, $V_{COM\_}$ = 2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{IN\_}$ = 2.5V, $V_{VIOS}$ = 0V, $V_{IIOS}$ = 2.5V, $V_{CLAMPHI\_}$ = 5V, $V_{CLAMPLO\_}$ = 0V, $V_{HH\_}$ = 10V, CDRP = 0b001, RO = 0b1000, HYST = 0b000, $Z_{LOAD}$ = 50Ω, $T_J$ = +70°C to an accuracy of ±15°C, unless otherwise noted. All temperature coefficients are measured at $T_J$ = +40°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Gain | $A_{DHV\_}$ | $V_{DLV\_}$ = -1.5V, $V_{DTV\_}$ = 1.5V, $V_{DHV\_}$ = 0V and 4.5V | | 0.998 | 1 | 1.002 | V/V |
| | $A_{DLV}$ | $V_{DHV\_}$ = 6.5V, $V_{DTV\_}$ = 1.5V, $V_{DLV\_}$ = 0V and 4.5V | | 0.998 | 1 | 1.002 | |
| | $A_{DTV}$ | $V_{DHV\_}$ = 6.5V, $V_{DLV\_}$ = -1.5V, $V_{DTV\_}$ = 0V and 4.5V | | 0.998 | 1 | 1.002 | |
| Linearity Error | | 0 to 3V relative to calibration points at 0 and 3V | $V_{DLV\_}$ = -1.5V, $V_{DTV\_}$ = 1.5V, $V_{DHV\_}$ = 0V, 0.75V, 1.5V, 2.25V, 3V | | | ±2 | mV |
| | | | $V_{DHV\_}$ = 6.5V, $V_{DTV\_}$ = 1.5V, $V_{DLV\_}$ = 0V, 0.75V, 1.5V, 2.25V, 3V | | | ±2 | |
| | | | $V_{DLV\_}$ = -1.5V, $V_{DHV\_}$ = 6.5V, $V_{DTV\_}$ = 0V, 0.75V, 1.5V, 2.25V, 3V | | | ±2 | |
| | | -1V to 6V relative to calibration points at 0 and 3V | $V_{DLV\_}$ = -1.5V, $V_{DTV\_}$ = 1.5V, $V_{DHV\_}$ = -1V and 6V | | | ±4.5 | |
| | | | $V_{DHV\_}$ = 6.5V, $V_{DTV\_}$ = 1.5V, $V_{DLV\_}$ = -1V and 6V | | | ±4.5 | |
| | | | $V_{DLV\_}$ = -1.5V, $V_{DHV\_}$ = 6.5V, $V_{DTV\_}$ = -1V and 6V | | | ±4.5 | |
| | | Full range relative to calibration points at 0 and 3V | $V_{DLV\_}$ = -1.5V, $V_{DTV\_}$ = 1.5V, $V_{DHV\_}$ = -1.25V and 6.5V | | | ±6 | |
| | | | $V_{DHV\_}$ = 6.5V, $V_{DTV\_}$ = 1.5V, $V_{DLV\_}$ = -1.5V and 6.25V | | | ±6 | |
| | | | $V_{DLV\_}$ = -1.5V, $V_{DHV\_}$ = 6.5V, $V_{DTV\_}$ = -1.5V and 6.5V | | | ±6 | |

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0V, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{CTV\_}$ = 1.4V, $V_{BV\_}$ = 4V, $V_{DGS}$ = $V_{GND}$ = 0V, $V_{CHV\_}$ = $V_{IVMAX\_}$ = 2V, $V_{CLV\_}$ = $V_{IVMIN\_}$ = 1V, $V_{COM\_}$ = 2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{IN\_}$ = 2.5V, $V_{VIOS}$ = 0V, $V_{IIOS}$ = 2.5V, $V_{CLAMPHI\_}$ = 5V, $V_{CLAMPLO\_}$ = 0V, $V_{HH\_}$ = 10V, CDRP = 0b001, RO = 0b1000, HYST = 0b000, $Z_{LOAD}$ = 50Ω, $T_J$ = +70°C to an accuracy of ±15°C, unless otherwise noted. All temperature coefficients are measured at $T_J$ = +40°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Crosstalk | | DHV_ to DLV_ | $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, $V_{DHV\_}$ = 0.2V and 6.5V | | | ±7 | mV |
| | | DLV_ to DHV_ | $V_{DHV\_}$ = 5V, $V_{DTV\_}$ = 1.5V, $V_{DLV\_}$ = -1.5 and 4.8V | | | ±7 | |
| | | DTV_ to DLV_ and DHV_ | $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = -1.5V and 6.5V | | | ±2 | |
| | | DHV_ to DTV_ | $V_{DTV\_}$ = 1.5V, $V_{DLV\_}$ = 0V, $V_{DHV\_}$ = 1.6V and 3V | | | ±3 | |
| | | DLV_ to DTV_ | $V_{DTV\_}$ = 1.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0 and 1.4V | | | ±3 | |
| Term Voltage | | Dependence on DATA_ | $V_{DTV\_}$ = 1.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, DATA_ = 0 and 1 | | | ±2 | mV |
| DC Power-Supply Rejection (Note 5) | | DHV_ | $V_{DHV\_}$ = 3V | 40 | | | dB |
| | | DLV_ | $V_{DLV\_}$ = 0V | 40 | | | |
| | | DTV_ | $V_{DTV\_}$ = 1.5V | 40 | | | |
| DC Drive Current Limit | | $V_{DHV\_}$ = 6.5V, $V_{DLV\_}$ = -1.5V | DATA_ = 1, $V_{DUT\_}$ = -1.5V | +60 | | +110 | mA |
| | | | DATA_ = 0, $V_{DUT\_}$ = 6.5V | -110 | | -60 | |
| DC Output Resistance | | (Note 6) | | 48 | 50 | 52 | Ω |
| DC Output Resistance Variation (Note 7) | | DATA_ = 1, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, $I_{DUT\_}$ = 1mA, 8mA, 15mA, 40mA | | | 1 | 2 | Ω |
| | | DATA_ = 0, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, $I_{DUT\_}$ = -1mA, -8mA, -15mA, -40mA | | | 1 | 2 | |
| Adjustable Output Resistance Range | | $R_O$ = 0xF vs. $R_O$ = 0x8 and $R_O$ = 0x0 vs. $R_O$ = 0x8, resolution of 0.36Ω (Note 6) | | | ±2.5 | | Ω |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0V, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{CTV\_}$ = 1.4V, $V_{BV\_}$ = 4V, $V_{DGS}$ = $V_{GND}$ = 0V, $V_{CHV\_}$ = $V_{IVMAX\_}$ = 2V, $V_{CLV\_}$ = $V_{IVMIN\_}$ = 1V, $V_{COM\_}$ = 2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{IN\_}$ = 2.5V, $V_{VIOS}$ = 0V, $V_{IIOS}$ = 2.5V, $V_{CLAMPHI\_}$ = 5V, $V_{CLAMPLO\_}$ = 0V, $V_{HH\_}$ = 10V, CDRP = 0b001, RO = 0b1000, HYST = 0b000, $Z_{LOAD}$ = 50Ω, $T_J$ = +70°C to an accuracy of ±15°C, unless otherwise noted. All temperature coefficients are measured at $T_J$ = +40°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **AC CHARACTERISTICS ($R_{DUT\_}$ = 50Ω to Ground) (Note 8)** | | | | | | |
| Dynamic Drive Current | | (Note 9) | | ±130 | | mA |
| Drive-Mode Overshoot | | Cable-droop compensation off, $V_{DLV\_}$ = 0V, $V_{DHV\_}$ = 0.1V | | 30 | | mV |
| | | Cable-droop compensation off, $V_{DLV\_}$ = 0V, $V_{DHV\_}$ = 1V | | 40 | | |
| | | Cable-droop compensation off, $V_{DLV\_}$ = 0V, $V_{DHV\_}$ = 3V | | 50 | | |
| | | Cable-droop compensation off, $V_{DLV\_}$ = 0V, $V_{DHV\_}$ = 5V | | 50 | | |
| Cable-Droop Compensation | | $V_{DLV\_}$ = 0V, $V_{DHV\_}$ = 3V, CDRP_ = 0b000 | | 0 | | % |
| | | $V_{DLV\_}$ = 0V, $V_{DHV\_}$ = 3V, CDRP_ = 0b111 | | 10 | | |
| Termination-Mode Overshoot | | Cable-droop compensation off (Note 10) | | 0 | | mV |
| Settling Time (Notes 4, 11) | | To within 100mV, $V_{DHV\_}$ = 5V, $V_{DLV\_}$ = 0V | | 0.25 | 1 | ns |
| | | To within 50mV, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V | | 0.25 | 1 | |
| | | To within 50mV, $V_{DHV\_}$ = 0.5V, $V_{DLV\_}$ = 0V | | 0.25 | 1 | |
| **TIMING CHARACTERISTICS (Notes 8, 12)** | | | | | | |
| Propagation Delay | | Data to output, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V (Note 13) | 1 | 1.9 | 4 | ns |
| | | Drive to term, term to drive (Notes 4, 14) | 1.7 | 2.7 | 3.7 | |
| | | Drive to high impedance, high impedance to drive, $V_{DHV\_}$ = 1V, $V_{DLV\_}$ = -1V (Notes 4, 15) | 1.4 | 2.4 | 3.4 | |
| Propagation-Delay Match | | $t_{LH}$ vs. $t_{HL}$ (Note 4) | | ±40 | ±80 | ps |
| | | Drivers within package, same edge | | ±40 | | |
| | | Drive to high impedance vs. high impedance to drive, $V_{DHV\_}$ = 1V, $V_{DLV\_}$ = -1V (Note 16) | | ±0.5 | | ns |
| | | High impedance vs. data | | ±0.5 | | |
| | | Drive to term vs. term to drive, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V (Note 17) | | ±0.3 | | |
| | | Terminate vs. data | | ±0.8 | | |
| Propagation-Delay Channel Match | | Differential mode, $V_{DHV\_}$ = 1V, $V_{DLV\_}$ = 0V, channel 1 inverted, DIFFERENTIAL0 = 1, INVERT1 = 1 | | ±40 | | ps |

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0V, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{CTV\_}$ = 1.4V, $V_{BV\_}$ = 4V, $V_{DGS}$ = $V_{GND}$ = 0V, $V_{CHV\_}$ = $V_{IVMAX\_}$ = 2V, $V_{CLV\_}$ = $V_{IVMIN\_}$ = 1V, $V_{COM\_}$ = 2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{IN\_}$ = 2.5V, $V_{VIOS}$ = 0V, $V_{IIOS}$ = 2.5V, $V_{CLAMPHI\_}$ = 5V, $V_{CLAMPLO\_}$ = 0V, $V_{HH\_}$ = 10V, CDRP = 0b001, RO = 0b1000, HYST = 0b000, $Z_{LOAD}$ = 50Ω, $T_J$ = +70°C to an accuracy of ±15°C, unless otherwise noted. All temperature coefficients are measured at $T_J$ = +40°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Propagation-Delay Temperature Coefficient | | $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V (Note 4) | | | 3 | 5 | ps/°C |
| Propagation-Delay Change | | Change vs. pulse width (Note 18) | $V_{DHV\_}$ = 1V, $V_{DLV\_}$ = 0V, 1ns to 24ns pulse width (Note 4) | | ±25 | ±60 | ps |
| | | | $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, 1ns to 24ns pulse width (Note 4) | | ±35 | ±60 | |
| | | | $V_{DHV\_}$ = 5V, $V_{DLV\_}$ = 0V, 1.5ns to 23.5ns pulse width | | ±100 | | |
| | | Peak-to-peak change vs. common mode, $V_{DHV\_}$ - $V_{DLV\_}$ = 1V, $V_{DHV\_}$ = 0 to 6V, using a DC-blocking capacitor (Note 4) | | | 50 | 60 | |
| Rise-and-Fall Time | | 0.2$V_{P-P}$ programmed, $V_{DHV\_}$ = 0.2V, $V_{DLV\_}$ = 0V, 20% to 80% | | | 275 | | ps |
| | | 1$V_{P-P}$ programmed, $V_{DHV\_}$ = 1V, $V_{DLV\_}$ = 0V, 10% to 90% | | 330 | 450 | 550 | |
| | | 3$V_{P-P}$ programmed, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, 10% to 90%, trim condition | | 500 | 650 | 800 | |
| | | 5$V_{P-P}$ programmed, $V_{DHV\_}$ = 5V, $V_{DLV\_}$ = 0V, 10% to 90% (Note 4) | | 800 | 1000 | 1200 | |
| Rise-and-Fall Time Matching | | 0.2$V_{P-P}$ programmed, $V_{DHV\_}$ = 0.2V, $V_{DLV\_}$ = 0V, 20% to 80% | | | ±40 | | ps |
| | | 1$V_{P-P}$ programmed, $V_{DHV\_}$ = 1V, $V_{DLV\_}$ = 0V, 10% to 90% | | | ±50 | ±130 | |
| | | 3$V_{P-P}$ programmed, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, 10% to 90% | | | ±50 | ±200 | |
| | | 5$V_{P-P}$ programmed, $V_{DHV\_}$ = 5V, $V_{DLV\_}$ = 0V, 10% to 90% | | | ±50 | | |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0V, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{CTV\_}$ = 1.4V, $V_{BV\_}$ = 4V, $V_{DGS}$ = $V_{GND}$ = 0V, $V_{CHV\_}$ = $V_{IVMAX\_}$ = 2V, $V_{CLV\_}$ = $V_{IVMIN\_}$ = 1V, $V_{COM\_}$ = 2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{IN\_}$ = 2.5V, $V_{VIOS}$ = 0V, $V_{IIOS}$ = 2.5V, $V_{CLAMPHI\_}$ = 5V, $V_{CLAMPLO\_}$ = 0V, $V_{HH\_}$ = 10V, CDRP = 0b001, RO = 0b1000, HYST = 0b000, $Z_{LOAD}$ = 50Ω, $T_J$ = +70°C to an accuracy of ±15°C, unless otherwise noted. All temperature coefficients are measured at $T_J$ = +40°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Slew Rate | | Relative to SC1 = SC0 = 0 | SC1 = 0, SC0 = 1, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, 20% to 80% | | 75 | | % |
| | | | SC1 = 1, SC0 = 0, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, 20% to 80% | | 50 | | |
| | | | SC1 = 1, SC0 = 1, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, 20% to 80% | | 25 | | |
| Minimum Pulse Width | | Positive or negative | $0.2V_{P-P}$ programmed, $V_{DHV\_}$ = 0.2V, $V_{DLV\_}$ = 0V (Note 19) | | 800 | | ps |
| | | | $1V_{P-P}$ programmed, $V_{DHV\_}$ = 1V, $V_{DLV\_}$ = 0V (Note 19) | | 950 | | |
| | | | $3V_{P-P}$ programmed, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V (Notes 4, 19) | | 1000 | 1250 | |
| | | | $5V_{P-P}$ programmed, $V_{DHV\_}$ = 5V, $V_{DLV\_}$ = 0V (Note 19) | | 1300 | | |
| Data Rate | | To 95%$_{P-P}$ (Note 20) | $0.2V_{P-P}$ programmed, $V_{DHV\_}$ = 0.2V, $V_{DLV\_}$ = 0V | | 1100 | | Mbps |
| | | | $1V_{P-P}$ programmed, $V_{DHV\_}$ = 1V, $V_{DLV\_}$ = 0V | | 900 | | |
| | | | $3V_{P-P}$ programmed, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V | | 800 | | |
| | | | $5V_{P-P}$ programmed, $V_{DHV\_}$ = 5V, $V_{DLV\_}$ = 0V | | 680 | | |
| | | To 90%$_{P-P}$ (Note 21) | $0.2V_{P-P}$ programmed, $V_{DHV\_}$ = 0.2V, $V_{DLV\_}$ = 0V | | 1200 | | |
| | | | $1V_{P-P}$ programmed, $V_{DHV\_}$ = 1V, $V_{DLV\_}$ = 0V | | 1100 | | |
| | | | $3V_{P-P}$ programmed, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V | | 900 | | |
| | | | $5V_{P-P}$ programmed, $V_{DHV\_}$ = 5V, $V_{DLV\_}$ = 0V | | 720 | | |

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0V, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{CTV\_}$ = 1.4V, $V_{BV\_}$ = 4V, $V_{DGS}$ = $V_{GND}$ = 0V, $V_{CHV\_}$ = $V_{IVMAX\_}$ = 2V, $V_{CLV\_}$ = $V_{IVMIN\_}$ = 1V, $V_{COM\_}$ = 2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{IN\_}$ = 2.5V, $V_{VIOS}$ = 0V, $V_{IIOS}$ = 2.5V, $V_{CLAMPHI\_}$ = 5V, $V_{CLAMPLO\_}$ = 0V, $V_{HH\_}$ = 10V, CDRP = 0b001, RO = 0b1000, HYST = 0b000, $Z_{LOAD}$ = 50Ω, $T_J$ = +70°C to an accuracy of ±15°C, unless otherwise noted. All temperature coefficients are measured at $T_J$ = +40°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Rise-and-Fall Time | | Drive to term, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, measured 10% to 90% of waveform | 300 | 500 | 1000 | ps |
| | | Term to drive, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, measured 10% to 90% of waveform | 300 | 600 | 850 | |
| **HIGH-SPEED COMPARATORS** | | | | | | |
| **DC CHARACTERISTICS** | | | | | | |
| Input-Voltage Range | | (Notes 2, 22) | -1.5 | | +6.5 | V |
| Differential Input Voltage | | $V_{DUT\_}$ - $V_{CHV\_}$, $V_{DUT\_}$ - $V_{CLV\_}$ (Note 23) | | | ±8 | V |
| Input Offset Voltage | | $V_{DUT\_}$ = 1.5V | | ±1 | ±5 | mV |
| Input-Voltage Temperature Coefficient | | (Notes 4, 24) | | ±50 | ±175 | µV°C |
| Common-Mode Rejection Ratio | CMRR | $V_{DUT\_}$ = -1.5V, 6.5V (Note 25) | 50 | 55 | | dB |
| Linearity Error (Note 26) | | 0 to 3V, $V_{DUT\_}$ = 0V, 1.5V, 3V | | ±1 | ±5 | mV |
| | | Full range, $V_{DUT\_}$ = -1.5V, 0V, 1.5V, 3V, 6.5V | | ±1 | ±10 | |
| Power-Supply Rejection Ratio | PSRR | $V_{DUT\_}$ = -1.5 and 6.5V (Notes 5, 27) | 50 | 66 | | dB |
| Hysteresis | | **HYST0** / **HYST1** / **HYST2** | | | | mV |
| | | 0 / 0 / 0 | | 0 | | |
| | | 0 / 0 / 1 | | 2 | | |
| | | 0 / 1 / 0 | | 4 | | |
| | | 0 / 1 / 1 | | 6 | | |
| | | 1 / 0 / 0 | | 8 | | |
| | | 1 / 0 / 1 | | 10 | | |
| | | 1 / 1 / 0 | | 12 | | |
| | | 1 / 1 / 1 | | 15 | | |
| **AC CHARACTERISTICS (Notes 4, 28, 29, 30)** | | | | | | |
| Minimum Pulse Width | | (Note 31) | | 0.50 | 0.65 | ns |
| Propagation Delay | | | 0.5 | 0.9 | 1.5 | ns |
| Propagation-Delay Temperature Coefficient | | | | 1.7 | | ps/°C |
| Propagation-Delay Match | | High/low vs. low/high, absolute value of delta for each comparator | | ±10 | ±25 | ps |
| Propagation-Delay Dispersion vs. Common-Mode Input | | -1.4V to +6.4V (Note 32) | | 40 | 55 | $ps_{P-P}$ |
| Propagation-Delay Dispersion vs. Duty Cycle | | 0.6ns to 24.4ns pulse width, relative to 5ns pulse width | | ±25 | ±40 | ps |
| Propagation-Delay Dispersion vs. Slew Rate | | 1V/ns to 6V/ns, relative to 2V/ns (Note 33) | | ±30 | ±55 | ps |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0V, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{CTV\_}$ = 1.4V, $V_{BV\_}$ = 4V, $V_{DGS}$ = $V_{GND}$ = 0V, $V_{CHV\_}$ = $V_{IVMAX\_}$ = 2V, $V_{CLV\_}$ = $V_{IVMIN\_}$ = 1V, $V_{COM\_}$ = 2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{IN\_}$ = 2.5V, $V_{VIOS}$ = 0V, $V_{IIOS}$ = 2.5V, $V_{CLAMPHI\_}$ = 5V, $V_{CLAMPLO\_}$ = 0V, $V_{HH\_}$ = 10V, CDRP = 0b001, RO = 0b1000, HYST = 0b000, $Z_{LOAD}$ = 50Ω, $T_J$ = +70°C to an accuracy of ±15°C, unless otherwise noted. All temperature coefficients are measured at $T_J$ = +40°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Equivalent 20–80 Bandwidth | | $V_{DTV\_}$ = 0.5V, driver terminated (Note 34) | | 1000 | 1500 | | MHz |
| | | Driver high impedance | | | 700 | | |
| Cable-Droop Compensation, Peaking | | 1V swing, rise/fall time = 500ps, DRV terminated | CDRP = 0b000 | | 0 | | % |
| | | | CDRP = 0b111 | | 10 | | |
| **LOGIC OUTPUTS (CH_, NCH_, CL_, NCL_ collector output, $R_L$ = 50Ω internal pullup to CTV)** | | | | | | | |
| Termination Voltage | CTV_ | | | 0 | | 3.5 | V |
| Output High Current | | | | | 0 | | mA |
| Output Low Current | | | | | 16 | | mA |
| Output-Voltage Compliance | | Set by $I_{OUT\_}$, $R_{TERM\_}$ and $V_{CTV}$ | | -0.5 | | CTV_ | V |
| Differential Rise Time | | 20% to 80% (Note 4) | | | 200 | 400 | ps |
| Differential Fall Time | | 20% to 80% (Note 4) | | | 200 | 400 | ps |
| Termination Resistor Value | | CTV_ to CH_, NCH_, CL_, NCL_ | | 48 | | 52 | Ω |
| Output High Voltage | $V_{OH}$ | With output resistors, $R_{TERM}$ to $V_{CTV}$ (Note 56) | | CTV_ - 0.1 | CTV_ - 0.02 | CTV_ | V |
| Output Low Voltage | $V_{OL}$ | With output resistors, $R_{TERM}$ to $V_{CTV}$ (Note 56) | | CTV_ - 0.55 | CTV_ - 0.4 | CTV_ - 0.35 | V |
| Output-Voltage Swing | | With output resistors, 50Ω nominal trim (Note 56) | | 350 | 400 | 450 | mV |
| **DYNAMIC CLAMPS** | | | | | | | |
| CPHV_ Functional Clamp Range | | $I_{DUT\_}$ = -1mA, $V_{CPLV\_}$ = -1.5V (Note 2) | | -0.3 | | +6.5 | V |
| CPLV_ Functional Clamp Range | | $I_{DUT\_}$ = 1mA, $V_{CPHV\_}$ = 6.5V (Note 2) | | -1.5 | | +5.3 | V |
| CPHV_ Maximum Programmable Voltage | | $I_{DUT\_}$ = 0mA (Note 23) | | 7.2 | 7.5 | | V |
| CPLV_ Minimum Programmable Voltage | | $I_{DUT\_}$ = 0mA (Note 23) | | | -2.5 | -2.2 | V |
| Offset Voltage | | $I_{DUT\_}$ = -1mA, $V_{CPHV\_}$ = 1.5V, $V_{CPLV\_}$ = -1.5V | | | | ±10 | mV |
| | | $I_{DUT\_}$ = 1mA, $V_{CPLV\_}$ = 1.5V, $V_{CPHV\_}$ = 6.5V | | | | ±10 | |
| Offset-Voltage Temperature Coefficient | | $V_{CPHV\_}$ = $V_{CPLV\_}$ = 1.5V | | | 0.5 | | mV/°C |
| Power-Supply Rejection Ratio | | $I_{DUT\_}$ = -1mA, $V_{CPHV\_}$ = 1.5V, $V_{CPLV\_}$ = -1.5V (Note 5) | | 40 | | | dB |
| | | $I_{DUT\_}$ = +1mA, $V_{CPLV\_}$ = 1.5V, $V_{CPHV\_}$ = 6.5V (Note 5) | | 40 | | | |
| High Clamp Voltage Gain | | $V_{CPHV\_}$ = -0.3V, 6.5V | | 0.998 | | 1.002 | V/V |
| Low Clamp Voltage Gain | | $V_{CPLV\_}$ = -1.5V, 5.3V | | 0.998 | | 1.002 | V/V |
| Voltage-Gain Temperature Coefficient | | | | | 100 | | ppm/°C |

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0V, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{CTV\_}$ = 1.4V, $V_{BV\_}$ = 4V, $V_{DGS}$ = $V_{GND}$ = 0V, $V_{CHV\_}$ = $V_{IVMAX\_}$ = 2V, $V_{CLV\_}$ = $V_{IVMIN\_}$ = 1V, $V_{COM\_}$ = 2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{IN\_}$ = 2.5V, $V_{VIOS}$ = 0V, $V_{IIOS}$ = 2.5V, $V_{CLAMPHI\_}$ = 5V, $V_{CLAMPLO\_}$ = 0V, $V_{HH\_}$ = 10V, CDRP = 0b001, RO = 0b1000, HYST = 0b000, $Z_{LOAD}$ = 50Ω, $T_J$ = +70°C to an accuracy of ±15°C, unless otherwise noted. All temperature coefficients are measured at $T_J$ = +40°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Linearity | | $I_{DUT\_}$ = -1mA, $V_{CPHV\_}$ = -0.3V, 1.5V, 3.25V, 5V, 6.5V | | | ±30 | mV |
| | | $I_{DUT\_}$ = 1mA, $V_{CPLV\_}$ = -1.5V, 0.5V, 2.25V, 4V, 5.3V | | | ±30 | |
| Static Output Current | | $V_{CPHV\_}$ = 0V, $V_{CPLV\_}$ = -1.5V, $R_L$ = 0Ω to 6.5V | -120 | | -60 | mA |
| | | $V_{CPLV\_}$ = 5V, $V_{CPHV\_}$ = 6.5V, $R_L$ = 0Ω to -1.5V | 60 | | 120 | |
| High Clamp Resistance | | $V_{CPHV\_}$ = 0V, $V_{CPLV\_}$ = -1.5V, $I_{DUT\_}$ = -5mA and -15mA | 48 | | 55 | Ω |
| Low Clamp Resistance | | $V_{CPHV\_}$ = 6.5V, $V_{CPLV\_}$ = 0V, $I_{DUT\_}$ = 5mA and 15mA | 48 | | 55 | Ω |
| High Clamp-Resistance Variation | | $I_{DUT\_}$ = -20mA and -30mA, $V_{CPHV\_}$ = 2.5V, $V_{CPLV\_}$ = -1.5V (Note 35) | | ±5 | | Ω |
| Low Clamp-Resistance Variation | | $I_{DUT\_}$ = 20mA and 30mA, $V_{CPLV\_}$ = 2.5V, $V_{CPHV\_}$ = 6.5V (Note 35) | | ±5 | | Ω |
| Overshoot and Undershoot | | (Note 36) | | 700 | | mV |
| **PARAMETRIC MEASUREMENT UNIT (PMU)** | | | | | | |
| **DC ELECTRICAL CHARACTERISTICS** | | | | | | |
| **FORCE VOLTAGE ($R_L$ ≥ 10MΩ, $V_{IN\_}$ = 2.5V, unless otherwise noted)** | | | | | | |
| Force-Voltage Output Range (Note 2) | $V_{IN}$ | $I_{DUT\_}$ = 0mA | -1.5 | | +6.5 | V |
| | | $I_{DUT\_}$ = +FSR/2, range A | -1.5 | | +4.5 | |
| | | $I_{DUT\_}$ = +FSR/2, ranges B–E | -1.5 | | +6.1 | |
| | | $I_{DUT\_}$ = -FSR/2, range A | 1.1 | | 6.5 | |
| | | $I_{DUT\_}$ = -FSR/2, ranges B–E | -1.1 | | +6.5 | |
| Force-Voltage Offset Error | | $I_{DUT\_}$ = 0mA | -5 | | +5 | mV |
| Force-Voltage PSRR | | (Note 5) | -5 | | +5 | mV/V |
| Force-Voltage Load Regulation | | $I_{DUT\_}$ = +FSR/2 to -FSR/2 using SENSE_ input | | ±200 | | µV |
| Force-Voltage Offset Temperature Coefficient | | (Note 37) | | ±50 | | µV/°C |
| Force-Voltage Gain Error | | $V_{IN}$ = -1.5V to +6.5V, nominal gain = +1 | -0.1 | | +0.1 | % |
| Force-Voltage Gain Temperature Coefficient | | | | ±10 | | ppm/°C |
| Force-Voltage Linearity Error | | $V_{IN}$ = -1.5V, 0.5V, 2.5V, 4.5V, 6.5V (Notes 38, 39) | -0.02 | | +0.02 | %FSR |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0V, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{CTV\_}$ = 1.4V, $V_{BV\_}$ = 4V, $V_{DGS}$ = $V_{GND}$ = 0V, $V_{CHV\_}$ = $V_{IVMAX\_}$ = 2V, $V_{CLV\_}$ = $V_{IVMIN\_}$ = 1V, $V_{COM\_}$ = 2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{IN\_}$ = 2.5V, $V_{VIOS}$ = 0V, $V_{IIOS}$ = 2.5V, $V_{CLAMPHI\_}$ = 5V, $V_{CLAMPLO\_}$ = 0V, $V_{HH\_}$ = 10V, CDRP = 0b001, RO = 0b1000, HYST = 0b000, $Z_{LOAD}$ = 50Ω, $T_J$ = +70°C to an accuracy of ±15°C, unless otherwise noted. All temperature coefficients are measured at $T_J$ = +40°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Force-Voltage Range Switching Glitch | | From any two adjacent ranges, $C_{DUT\_}$ = 100pF, $I_{DUT\_}$ = (±0.25 x FSR) of lower current range (Note 4) | | | 0.3 | V |
| **MEASURE CURRENT (Measured at MEAS_ in FIMI mode, $V_{IN\_}$ = $V_{IIOS}$ = $V_{DUT\_}$ = 2.5V)** | | | | | | |
| Measure-Current Offset | $I_{MOS}$ | (Note 38) | -1 | | +1 | %FSR |
| Measure-Current PSRR | | $I_{DUT\_}$ = 0mA (Note 5) | -0.05 | | +0.05 | %FSR/V |
| Measure-Current Offset Temperature Coefficient | | | | ±20 | | ppmFSR/°C |
| Measure-Current Gain Error | $I_{MGE}$ | Ranges A, B, C | -1.0 | | +1.0 | % |
| | | Ranges D, E | -1.1 | | +1.1 | |
| Measure-Current Gain Temperature Coefficient | | Ranges B–E | | ±20 | | ppm/°C |
| | | Range A | | +100 | | |
| Measure-Current Linearity Error (Note 38) | $I_{MLER}$ | Ranges B–E, $I_{DUT\_}$ = -FSR/2, -FSR/4, 0, FSR/4, FSR/2 relative to end points | -0.02 | | +0.02 | %FSR |
| | | Range A, $I_{DUT\_}$ = -30mA, -15mA, 0, 15mA, 30mA, relative to end points | -0.03 | | +0.03 | |
| | | Range A, $I_{DUT\_}$ = -FSR/2, -FSR/4, 0, FSR/4, FSR/2 relative to end points | -0.06 | | +0.06 | |
| +FSR Measure Output Voltage | | $V_{IIOSMIN}$ = 2V (Note 40) | | 6 | | V |
| | | $V_{IIOSMAX}$ = 4V (Note 40) | | 8 | | |
| -FSR Measure Output Voltage | | $V_{IIOSMIN}$ = 2V (Note 40) | | -2 | | V |
| | | $V_{IIOSMAX}$ = 4V (Note 40) | | 0 | | |
| Rejection of Output Measure Error Due to Common-Mode Sense Voltage | $CMVR_{LER}$ | $I_{DUT\_}$ = 0mA, $V_{IN\_}$ = -1.5V to +6.5V, percent FSR change at MEAS_ per volt change at DUT_ | | | 0.003 | %FSR/V |
| Measure-Current Range (Note 2) | | Range E, R_E = 500kΩ | -2 | | +2 | µA |
| | | Range D, R_D = 50kΩ | -20 | | +20 | |
| | | Range C, R_C = 5kΩ | -200 | | +200 | |
| | | Range B, R_B = 500Ω | -2 | | +2 | mA |
| | | Range A, R_A = 20Ω (Note 41) | -50 | | +50 | |
| **FORCE CURRENT ($V_{DUT\_}$ = $V_{IN\_}$ = $V_{IIOS}$ = 2.5V, unless otherwise noted)** | | | | | | |
| Input-Voltage Range For Setting Force Current to +FSR/2 | | $V_{IIOSMIN}$ = 2V | | 6 | | V |
| | | $V_{IIOSMAX}$ = 3.5V | | 7.5 | | |
| Input-Voltage Range For Setting Force Current to -FSR/2 | | $V_{IIOSMIN}$ = 2V | | -2 | | V |
| | | $V_{IIOSMAX}$ = 3.5V | | -0.5 | | |
| Current-Sense Amplifier Offset Voltage Input | | Relative to $V_{DGS}$ | 2.0 | 2.5 | 3.5 | V |

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0V, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{CTV\_}$ = 1.4V, $V_{BV\_}$ = 4V, $V_{DGS}$ = $V_{GND}$ = 0V, $V_{CHV\_}$ = $V_{IVMAX\_}$ = 2V, $V_{CLV\_}$ = $V_{IVMIN\_}$ = 1V, $V_{COM\_}$ = 2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{IN\_}$ = 2.5V, $V_{VIOS}$ = 0V, $V_{IIOS}$ = 2.5V, $V_{CLAMPHI\_}$ = 5V, $V_{CLAMPLO\_}$ = 0V, $V_{HH\_}$ = 10V, CDRP = 0b001, RO = 0b1000, HYST = 0b000, $Z_{LOAD}$ = 50Ω, $T_J$ = +70°C to an accuracy of ±15°C, unless otherwise noted. All temperature coefficients are measured at $T_J$ = +40°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Force-Current Offset | | (Note 38) | -0.1 | | +0.1 | %FSR |
| Force-Current Offset PSRR | | (Note 5) | -0.2 | | +0.2 | %FSR/V |
| Force-Current Offset-Temperature Coefficient | | (Note 37) | | ±20 | | ppmFSR/°C |
| Force-Current Gain Error | | $V_{IN\_}$ = -1.5V and 6.5V | -0.1 | | +0.1 | % |
| Force-Current Gain-Temperature Coefficient | | Ranges B–E | | ±20 | | ppm/°C |
| | | Range A | | -100 | | |
| Force-Current Linearity Error (Notes 38, 39) | | Ranges B–E, $V_{IN\_}$ = -1.5V, 0.5V, 2.5V, 4.5V, 6.5V relative to end points of $I_{DUT\_}$ | -0.025 | | +0.025 | %FSR |
| | | Range A, IDUT_ ±30mA, VIN_ = 0V, 1V, 1.3V, 2.5V, 3.7V, 4.9V relative to end points of $I_{DUT\_}$ | -0.03 | | +0.03 | |
| | | Range A, $V_{IN\_}$ = -1.5V, 0.5V, 2.5V, 4.5V, 6.5V relative to end points of $I_{DUT\_}$ | -0.06 | | +0.06 | |
| Rejection of Output Error Due to Common-Mode DUT_ Voltage | | Percent of FSR change of the force current per volt change in DUT_, $V_{DUT\_}$ = -1.5V to 6.5V | | | 0.007 | %FSR/V |
| Force-Current Range (Note 2) | | Range E, R_E = 500kΩ | -2 | | +2 | µA |
| | | Range D, R_D = 50kΩ | -20 | | +20 | |
| | | Range C, R_C = 5kΩ | -200 | | +200 | |
| | | Range B, R_B = 500Ω | -2 | | +2 | mA |
| | | Range A, R_A = 20 , (Note 41) | -50 | | +50 | |
| **MEASURE VOLTAGE (Measured at MEAS_ in FVMV mode, $V_{VIOS}$ = 0, $V_{DUT\_}$ = $V_{IN\_}$ = $V_{IIOS}$ = 2.5V)** | | | | | | |
| Measure-Voltage Offset | | | -25 | | +25 | mV |
| Measure-Voltage PSRR | | (Note 5) | -5 | | +5 | mV/V |
| Measure-Voltage Offset Temperature Coefficient | | | | ±100 | | µV/°C |
| Measure-Voltage Gain Error | | $V_{DUT\_}$ = -1.5V and 6.5V, nominal gain = +1 | -1 | | +1 | % |
| Measure-Voltage Gain-Temperature Coefficient | | | | ±10 | | ppm/°C |
| Measure-Voltage Linearity Error | | $V_{IN\_}$ = -1.5V, 0.5V, 2.5V, 4.5V, 6.5V relative to end points. (Note 38) | -0.02 | | +0.02 | %FSR |
| Measure Output Voltage (Note 42) | | For $V_{DUT\_}$ = 6.5V, measure voltage input range = -1.5V to 6.5V, $V_{VIOS}$ offsets the range at MEAS_ | | 6.5 + $V_{VIOS}$ | | V |
| | | For $V_{DUT\_}$ = -1.5V | | -1.5 + $V_{VIOS}$ | | |
| Voltage Sense Amp Offset Voltage Input | $V_{IOS}$ | Relative to DUT ground (Note 42) | 0 | | 1.5 | V |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0V, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{CTV\_}$ = 1.4V, $V_{BV\_}$ = 4V, $V_{DGS}$ = $V_{GND}$ = 0V, $V_{CHV\_}$ = $V_{IVMAX\_}$ = 2V, $V_{CLV\_}$ = $V_{IVMIN\_}$ = 1V, $V_{COM\_}$ = 2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{IN\_}$ = 2.5V, $V_{VIOS}$ = 0V, $V_{IIOS}$ = 2.5V, $V_{CLAMPHI\_}$ = 5V, $V_{CLAMPLO\_}$ = 0V, $V_{HH\_}$ = 10V, CDRP = 0b001, RO = 0b1000, HYST = 0b000, $Z_{LOAD}$ = 50Ω, $T_J$ = +70°C to an accuracy of ±15°C, unless otherwise noted. All temperature coefficients are measured at $T_J$ = +40°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **FORCE OUTPUT** | | | | | | |
| Short-Circuit Current Limit in FV Mode | | Range A, $V_{IN\_}$ = -1.5V, $V_{DUT\_}$ = 6.5V, CLENABLE = 0 | -100 | | -55 | mA |
| | | Range B, $V_{IN\_}$ = -1.5V, $V_{DUT\_}$ = 6.5V, CLENABLE = 0 | -8 | | -3 | |
| | | Range A, $V_{IN\_}$ = 6.5V, $V_{DUT\_}$ = -1.5V, CLENABLE = 0 | 55 | | 100 | |
| | | Range B, $V_{IN\_}$ = 6.5V, $V_{DUT\_}$ = -1.5V, CLENABLE = 0 | 3 | | 8 | |
| Force-to-Sense Resistor | $R_{FS}$ | (Note 4) | | 10 | | k |
| **SENSE INPUT** | | | | | | |
| Input-Voltage Range | | All modes except $V_{HHP}$ driver mode | -1.5 | | +6.5 | V |
| | | VHH_ driver-mode compliance, SENSE open (Note 43) | -1.5 | | +13.0 | |
| Input Bias Current | | $V_{SENSE\_}$ = -1.5V and 6.5V, sense input enabled | -5 | | +5 | nA |
| **COMPARATOR INPUTS ($V_{IN\_}$ = $V_{IIOS}$ = 2.5V, HYSTEN = 0, unless otherwise noted)** | | | | | | |
| Input-Voltage Range | | Maximum at $V_{IIOS}$ = 3.4V, MI mode | | +7.4 | | V |
| | | Minimum at $V_{IIOS}$ = 2V, MI mode | | -2.2 | | |
| FIMV Offset Voltage | | $V_{DUT\_}$ = 2.5V (Note 44) | -5 | | +5 | mV |
| FVMI Offset Current | | IVMAX_ = IVMIN_ = 2.5V (Note 44) | -0.1 | | +0.1 | %FSR |
| Hysteresis | | HYSTEN = 1, functionally tested in MV mode | | ±25 | ±50 | mV |
| **VOLTAGE CLAMPS (FI mode, CLENABLE_ = 1)** | | | | | | |
| Clamp Voltage Range | | (Note 45) | -1.5 | | +6.5 | V |
| Linear FI DUT_ Range | | FI loop not influenced when $V_{DUT\_}$ 0.5V from voltage clamps | $V_{CLAMPLO\_}$ + 0.5 | | $V_{CLAMPHI\_}$ - 0.5 | V |
| Clamp Voltage Accuracy | | $V_{CLAMPHI\_}$ = $V_{CLAMPLO\_}$ = -1.5V, 0V, 1.5V, 2.5V, 4V, 5V, 6.5V | -20 | | +20 | mV |
| **CURRENT CLAMPS (FV mode, CLENABLE_ = 1)** | | | | | | |
| Input Control Voltage Range | $V_{CLAMPHI\_MAX}$ | Clamp current = $I_{CLAMPHI\_}$ = ($V_{CLAMPHI\_}$ - $V_{IIOS}$)/$R_{RANGE}$ (sourcing) | | $V_{IIOS}$ + 1.3V | | V |
| | $V_{CLAMPLO\_MIN}$ | Clamp current = $I_{CLAMPLOI\_}$ = ($V_{CLAMPLO\_}$ - $V_{IIOS}$)/ $R_{RANGE}$ (sinking) | | $V_{IIOS}$ - 1.3V | | |

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0V, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{CTV\_}$ = 1.4V, $V_{BV\_}$ = 4V, $V_{DGS}$ = $V_{GND}$ = 0V, $V_{CHV\_}$ = $V_{IVMAX\_}$ = 2V, $V_{CLV\_}$ = $V_{IVMIN\_}$ = 1V, $V_{COM\_}$ = 2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{IN\_}$ = 2.5V, $V_{VIOS}$ = 0V, $V_{IIOS}$ = 2.5V, $V_{CLAMPHI\_}$ = 5V, $V_{CLAMPLO\_}$ = 0V, $V_{HH\_}$ = 10V, CDRP = 0b001, RO = 0b1000, HYST = 0b000, $Z_{LOAD}$ = 50Ω, $T_J$ = +70°C to an accuracy of ±15°C, unless otherwise noted. All temperature coefficients are measured at $T_J$ = +40°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Clamp Current Range (Note 45) | | Range E, R_E = 500kΩ | | -2.2 | | +2.2 | µA |
| | | Range D, R_D = 50kΩ | | -22 | | +22 | |
| | | Range C, R_C = 5kΩ | | -220 | | +220 | |
| | | Range B, R_B = 500Ω | | -2.2 | | +2.2 | mA |
| | | Range A, R_A = 20Ω | | -55 | | +55 | |
| Linear FV $I_{DUT\_}$ Range | | FV loop not influenced when $I_{DUT\_}$ ≥ 10% FSR from current clamps | | $I_{CLAMPLO\_}$ + 10%FSR | | $I_{CLAMPHI\_}$ - 10%FSR | A |
| Clamp Current Accuracy | | $\|I_{CLAMPHI\_}\|$ = $\|I_{CLAMPLO\_}\|$ = 0, (0.25 x FSR), (0.50 x FSR) and (0.55 x FSR), calibrated at 0 and (0.50 x FSR) | | -0.5 | | +0.5 | %FSR |
| **COMPARATOR OUTPUTS (Note 46)** | | | | | | | |
| Output High Voltage | | $R_{PULLUP}$ = 1kΩ to $V_{DD}$ | | $V_{DD}$ - 0.2 | | | V |
| Output Low Voltage | | $R_{PULLUP}$ = 1kΩ to $V_{DD}$ | | | | 0.4 | V |
| High-Impedance State Leakage Current | | | | | ±1 | | µA |
| High-Impedance State Output Capacitance | | | | | 6 | | pF |
| **AC ELECTRICAL CHARACTERISTICS ($V_{VIOS}$ = 0V, $V_{IIOS}$ = 2.5V, $C_{DUT\_}$ = $C_{MEAS\_}$ = 100pF, $R_{DUT\_}$ = 4 x $R_{RANGE}$ to 2.5V, unless otherwise noted; setting times are to 0.1%FSR)** | | | | | | | |
| **FORCE VOLTAGE** | | | | | | | |
| Settling Time | | $V_{IN\_}$ = -1.5V, 6.5V | Range E, R_E = 500kΩ | | 140 | | µs |
| | | | Range D, R_D = 50kΩ | | 30 | | |
| | | | Range C, R_C = 5kΩ | | 20 | 30 | |
| | | | Range B, R_B = 500Ω | | 20 | | |
| | | $V_{IN\_}$ = -1V to +6.5V | Range A, R_A = 20Ω , $R_{DUT\_}$ = 200Ω to 2.5V (Note 41) | | 20 | | |
| Maximum Stable Load Capacitance | | | | | 2500 | | pF |
| **FORCE VOLTAGE/MEASURE CURRENT** | | | | | | | |
| Settling Time | | Range E, R_E = 500kΩ | | | 300 | | µs |
| | | Range D, R_D = 50kΩ | | | 40 | | |
| | | Range C, R_C = 5kΩ | | | 20 | 35 | |
| | | Range B, R_B = 500Ω | | | 20 | | |
| | | Range A, R_A = 20Ω , $R_{DUT\_}$ = 200Ω to 2.5V (Note 41) | | | 20 | | |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0V, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{CTV\_}$ = 1.4V, $V_{BV\_}$ = 4V, $V_{DGS}$ = $V_{GND}$ = 0V, $V_{CHV\_}$ = $V_{IVMAX\_}$ = 2V, $V_{CLV\_}$ = $V_{IVMIN\_}$ = 1V, $V_{COM\_}$ = 2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{IN\_}$ = 2.5V, $V_{VIOS}$ = 0V, $V_{IIOS}$ = 2.5V, $V_{CLAMPHI\_}$ = 5V, $V_{CLAMPLO\_}$ = 0V, $V_{HH\_}$ = 10V, CDRP = 0b001, RO = 0b1000, HYST = 0b000, $Z_{LOAD}$ = 50Ω, $T_J$ = +70°C to an accuracy of ±15°C, unless otherwise noted. All temperature coefficients are measured at $T_J$ = +40°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Range-Change Switching | | In addition to force-voltage and measure-current settling times, range A to range B (Note 47) | | | 20 | | µs |
| **FORCE CURRENT (Measured at MEAS_ in FIMI Mode)** | | | | | | | |
| Settling Time | | $V_{IN\_}$ = -1.5V, +6.5V | Range E, R_E = 500kΩ | | 500 | | µs |
| | | | Range D, R_D = 50kΩ | | 100 | | |
| | | | Range C, R_C = 5kΩ | | 25 | 35 | |
| | | | Range B, R_B = 500Ω | | 20 | | |
| | | $V_{IN\_}$ = -1.1V to +4.1V | Range A, R_A = 20Ω $R_{DUT\_}$ = 200Ω to 2.5V (Note 41) | | 20 | | |
| **FORCE CURRENT/MEASURE VOLTAGE (Note 48)** | | | | | | | |
| Settling Time | | Range E, R_E = 500kΩ | | | 1900 | | µs |
| | | Range D, R_D = 50kΩ | | | 200 | | |
| | | Range C, R_C = 5kΩ | | | 30 | 40 | |
| | | Range B, R_B = 500Ω | | | 20 | | |
| | | Range A, R_A = 20Ω, $R_{DUT\_}$ = 200Ω to 2.5V (Note 41) | | | 20 | | |
| Range-Change Switching | | In addition to force-current/measure-voltage settling times, range A to range B. (Note 47) | | | 20 | | µs |
| **SENSE INPUT TO MEASURE OUTPUT PATH (Note 49)** | | | | | | | |
| Propagation Delay | | Measured at 90% of output, SENSE input slew rate ≤ 2V/µs | | | 0.07 | | µs |
| **MEASURE OUTPUT** | | | | | | | |
| High-Impedance Leakage Current | | $V_{MEAS\_}$ = -1.5V, 2.5V, 6.5V | | -10 | | +10 | nA |
| HIZMEASP_ True to High-Impedance Time | | $R_{MEAS\_}$ = 5kΩ to GND, $V_{SENSE}$ = 2.5V, measured from the 50% point of $\overline{HIZMEASP\_}$ to 90% of output | | | 80 | | ns |
| $\overline{HIZMEASP\_}$ False to Active Time | | $R_{MEAS\_}$ = 5kΩ to GND, $V_{SENSE}$ = 2.5V, measured from the 50% point of $\overline{HIZMEASP\_}$ to 10% of output | | | 40 | | ns |
| Maximum Stable Load Capacitance | | | | | 1000 | | pF |
| **FORCE OUTPUT** | | | | | | | |
| $\overline{LLEAKP\_}$ True to Low-Leak Time | | $V_{IN\_}$ = 1V, $R_{DUT\_}$ = $R_{RANGE\_}$ to GND, FVMI mode, measured from the 50% point of $\overline{LLEAKP\_}$ to 90% of output | | | 0.3 | | µs |

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0V, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{CTV\_}$ = 1.4V, $V_{BV\_}$ = 4V, $V_{DGS}$ = $V_{GND}$ = 0V, $V_{CHV\_}$ = $V_{IVMAX\_}$ = 2V, $V_{CLV\_}$ = $V_{IVMIN\_}$ = 1V, $V_{COM\_}$ = 2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{IN\_}$ = 2.5V, $V_{VIOS}$ = 0V, $V_{IIOS}$ = 2.5V, $V_{CLAMPHI\_}$ = 5V, $V_{CLAMPLO\_}$ = 0V, $V_{HH\_}$ = 10V, CDRP = 0b001, RO = 0b1000, HYST = 0b000, $Z_{LOAD}$ = 50Ω, $T_J$ = +70°C to an accuracy of ±15°C, unless otherwise noted. All temperature coefficients are measured at $T_J$ = +40°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $\overline{\text{LLEAKP\_}}$ False to Active Time | | $V_{IN\_}$ = 1V, $R_{DUT\_}$ = $R_{RANGE\_}$ to GND, FVMI mode, measured from the 50% point of $\overline{\text{LLEAKP\_}}$ to 10% of output | | | 0.3 | | µs |
| **COMPARATORS ($C_{CMP\_}$ = 20PF, $R_{\overline{PULLUP}}$ = 1kΩ to $V_{DD}$)** | | | | | | | |
| Rise Time | | 20% to 80% | | | 35 | | ns |
| Fall Time | | 80% to 20% | | | 1.5 | | ns |
| Disable True to High Impedance | | Measured from the 50% point of $\overline{CS}$ (or $\overline{LOAD}$) to 10% of the output | | | 25 | | ns |
| Disable False to Active | | Measured from the 50% point of $\overline{CS}$ (or $\overline{LOAD}$) to 90% of the output | | | 20 | | ns |
| **ACTIVE LOAD** | | | | | | | |
| **DC CHARACTERISTICS ($V_{VCOM\_}$ = 2.5V, $V_{DHV\_}$ = $V_{DLV\_}$ = 6V, unless otherwise noted)** | | | | | | | |
| VCOM_ Voltage Range | VCOM_ | | | -1.5 | | +6.5 | V |
| VCOM_ Offset Voltage | | $I_{DUT\_}$ = 0mA | | | | ±5 | mV |
| Differential Voltage Range | | $V_{DUT\_}$ - $V_{VCOM\_}$ | | -8 | | +8 | V |
| Offset Voltage-Temperature Coefficient | | | | | 100 | | µV/°C |
| VCOM_ Voltage Gain | | $V_{VCOM\_}$ = 0, 4.5V | | 0.998 | 1 | 1.002 | V/V |
| VCOM_ Voltage-Gain Temperature Coefficient | | | | | -10 | | ppm/°C |
| VCOM_ Linearity Error | | $V_{VCOM\_}$ = -1.5V, 0V, 1.5V, 3V, 4.5V, 6.5V relative to end points | | | ±3 | ±15 | mV |
| VCOM_ Output-Voltage Power-Supply Rejection Ratio | | (Note 5) | | 40 | | | dB |
| Sink or Source Output Resistance | | $V_{DUT\_}$ = 3V, 6.5V with $V_{VCOM\_}$ = -1.5V or $V_{DUT\_}$ = -1.5V, 2V with $V_{VCOM\_}$ = 6.5V | $I_{SOURCE}$ = $I_{SINK}$ = 20mA | 30 | | | kΩ |
| | | | $I_{SOURCE}$ = $I_{SINK}$ = 1mA | 250 | | | |
| Linear Region Output Resistance | | $I_{DUT\_}$ = ±10mA | | | 12 | 18 | Ω |
| Dead-Band | | $I_{SOURCE\_}$ = $I_{SINK\_}$ = 10mA, 80% commutation | | | 400 | | mV |
| | | 95% $I_{SOURCE\_}$ to 95% $I_{SINK\_}$, $I_{SOURCE}$ = $I_{SINK}$ = 20mA | | | 700 | 900 | |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0V, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{CTV\_}$ = 1.4V, $V_{BV\_}$ = 4V, $V_{DGS}$ = $V_{GND}$ = 0V, $V_{CHV\_}$ = $V_{IVMAX\_}$ = 2V, $V_{CLV\_}$ = $V_{IVMIN\_}$ = 1V, $V_{COM\_}$ = 2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{IN\_}$ = 2.5V, $V_{VIOS}$ = 0V, $V_{IIOS}$ = 2.5V, $V_{CLAMPHI\_}$ = 5V, $V_{CLAMPLO\_}$ = 0V, $V_{HH\_}$ = 10V, CDRP = 0b001, RO = 0b1000, HYST = 0b000, $Z_{LOAD}$ = 50Ω, $T_J$ = +70°C to an accuracy of ±15°C, unless otherwise noted. All temperature coefficients are measured at $T_J$ = +40°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **SOURCE CURRENT ($V_{DUT\_}$ = -1V, $V_{VCOM\_}$ = 6V, $V_{VLDL\_}$ = 0V, $V_{VLDH\_}$ = 6V, unless otherwise noted)** | | | | | | |
| Source Current Output Range | | $V_{VLDH\_}$ = 0 to 6V (Note 2) | 0 | | 20 | mA |
| Source Current Offset | | $V_{VLDH\_}$ = 300mV (1mA) | -20 | | +20 | µA |
| Source Current Programming Gain | | $V_{VLDH\_}$ = 0.3V, 5.4V (1mA, 18mA) | 3.326 | 3.333 | 3.340 | mA/V |
| Source Current Temperature Coefficient | | | | -10 | | µA/°C |
| Source Current Power-Supply Rejection Ratio | | (Note 5) | | | ±60 | µA/V |
| Source Current Linearity | | $V_{VLDH\_}$ = 0V, 0.1V, 0.3V, 1.5V, 3V, 5.4V, 6V, relative to 0.3V and 5.4V | | | ±80 | µA |
| **SINK CURRENT ($V_{DUT\_}$ = 6V, $V_{VCOM\_}$ = -1V, $V_{VLDL\_}$ = 6V, $V_{VLDH\_}$ = 0V, unless otherwise noted)** | | | | | | |
| Sink Current Output Range | | $V_{VLDL\_}$ = 0 to 6V (Note 2) | 0 | | 20 | mA |
| Sink Current Offset | | $V_{VLDL\_}$ = 300mV (1mA) | -20 | | +20 | µA |
| Sink Current Programming Gain | | $V_{VLDL\_}$ = 0.3V, 5.4V (1mA, 18mA) | 3.326 | 3.333 | 3.340 | mA/V |
| Sink Current Temperature Coefficient | | | | 10 | | µA/°C |
| Sink Current Power-Supply Rejection Ratio | PSRR | (Note 5) | | | ±60 | µA/V |
| Sink Current Linearity | | $V_{VLDL\_}$ = 0V, 0.1V, 0.3V, 1.5V, 3V, 5.4V, 6V, relative to 0.3V and 5.4V | | | ±80 | µA |
| **AC CHARACTERISTICS ($Z_L$ = 50Ω to GND, $V_{VLDH\_}$ = $V_{VLDL\_}$ = 6V, TMSEL_ = LDDIS_ = LDCAL_ = 0)** | | | | | | |
| Transition Time to/from Inhibit via RCV/NRCV | $t_{EN}$ | Measured from 50% crossing of RCV/NRVC to 10% level of output waveform; $V_{VCOM\_}$ = -1.5V and 1.5V | | 2 | | ns |
| Spike During Enable/Disable Transition | | $V_{VCOM\_}$ = 0V (Note 4) | | 200 | 300 | mV |
| **TEMPERATURE MONITOR** | | | | | | |
| Nominal Voltage | | $T_J$ = +70°C, $R_L$ ≥ 10MΩ | | 3.43 | | V |
| Temperature Coefficient | | | | 10 | | mV/°C |
| Output Resistance | | | | 15 | | kΩ |
| **DIGITAL I/O** | | | | | | |
| **DIFFERENTIAL CONTROL INPUTS (DATA_, NDATA_, RCV_, NRCV_)** | | | | | | |
| Input High Voltage | | | -1.6 | | +3.5 | V |
| Input Low Voltage | | | -2.0 | | +3.1 | V |
| Differential Input Voltage | | | ±0.15 | | ±1.0 | V |

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0V, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{CTV\_}$ = 1.4V, $V_{BV\_}$ = 4V, $V_{DGS}$ = $V_{GND}$ = 0V, $V_{CHV\_}$ = $V_{IVMAX\_}$ = 2V, $V_{CLV\_}$ = $V_{IVMIN\_}$ = 1V, $V_{COM\_}$ = 2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{IN\_}$ = 2.5V, $V_{VIOS}$ = 0V, $V_{IIOS}$ = 2.5V, $V_{CLAMPHI\_}$ = 5V, $V_{CLAMPLO\_}$ = 0V, $V_{HH\_}$ = 10V, CDRP = 0b001, RO = 0b1000, HYST = 0b000, $Z_{LOAD}$ = 50Ω, $T_J$ = +70°C to an accuracy of ±15°C, unless otherwise noted. All temperature coefficients are measured at $T_J$ = +40°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Differential Termination Resistance | | Between RCV and NRCV, DATA, and NDATA, tested at $I_{RCV\_/NRCV\_}$ = ±4mA (Note 50) | 96 | | 104 | Ω |
| **SINGLE-ENDED CONTROL INPUTS ($\overline{CS}$, SCLK, DIN, $\overline{RST}$, $\overline{LOAD}$, $\overline{ENVHHP\_}$, $\overline{LLEAKP\_}$, $\overline{HIZMEASP\_}$)** | | | | | | |
| Input High | | | 2/3 x $V_{DD}$ | | $V_{DD}$ | V |
| Input Low | | | -0.1 | | 1/3 x $V_{DD}$ | V |
| Input Bias Current | | | -25 | | +25 | µA |
| **SINGLE-ENDED OUTPUT (DOUT)** | | | | | | |
| Output High | | $I_{OH}$ = 25µA | $V_{DD}$ - 0.15 | | | V |
| Output Low | | $I_{OL}$ = -25µA | | | DGND + 0.15 | V |
| **SERIAL PORT TIMING** | | | | | | |
| SCLK Frequency | f | | | | 50 | MHz |
| SCLK Pulse-Width High | $t_{CH}$ | | 8 | | | ns |
| SCLK Pulse-Width Low | $t_{CL}$ | | 8 | | | ns |
| $\overline{CS}$ Low to SCLK High Setup | $t_{CSS0}$ | | 3.5 | | | ns |
| SCLK High to $\overline{CS}$ Low Hold | $t_{CSH0}$ | | 3.5 | | | ns |
| $\overline{CS}$ High to SCLK High Setup | $t_{CSS1}$ | | 3.5 | | | ns |
| SCLK High to $\overline{CS}$ High Hold | $t_{CSH1}$ | | 3.5 | | | ns |
| DIN to SCLK High Setup | $t_{DS}$ | | 3.5 | | | ns |
| DIN to SCLK High Hold | $t_{DH}$ | | 3.5 | | | ns |
| $\overline{CS}$ High Pulse Width | $t_{CSWH}$ | | 40 | | | ns |
| $\overline{LOAD}$ Low Pulse Width | $t_{LDW}$ | | 20 | | | ns |
| $\overline{RST}$ Low Pulse Width | $t_{RST}$ | | 20 | | | ns |
| $\overline{CS}$ High to $\overline{LOAD}$ Low Hold Time | $t_{CSHLD}$ | | 20 | | | ns |
| SCLK to DOUT Delay | $t_{DO}$ | | | | 40 | ns |
| **COMMON FUNCTIONS** | | | | | | |
| Operating Voltage Range | | (Note 2) | -1.5 | | +13.0 | V |
| DUT_ High-Impedance Leakage | | $V_{DUT\_}$ = 0V, 1.5V, 3V | -2 | | +2 | µA |
| | | $V_{CLV\_}$ = $V_{CHV\_}$ = 6.5V, $V_{DUT\_}$ = -1.5V | -5 | | +5 | |
| | | $V_{CLV\_}$ = $V_{CHV\_}$ = -1.5V, $V_{DUT\_}$ = 6.5V | -5 | | +5 | |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0V, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{CTV\_}$ = 1.4V, $V_{BV\_}$ = 4V, $V_{DGS}$ = $V_{GND}$ = 0V, $V_{CHV\_}$ = $V_{IVMAX\_}$ = 2V, $V_{CLV\_}$ = $V_{IVMIN\_}$ = 1V, $V_{COM\_}$ = 2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{IN\_}$ = 2.5V, $V_{VIOS}$ = 0V, $V_{IIOS}$ = 2.5V, $V_{CLAMPHI\_}$ = 5V, $V_{CLAMPLO\_}$ = 0V, $V_{HH\_}$ = 10V, CDRP = 0b001, RO = 0b1000, HYST = 0b000, $Z_{LOAD}$ = 50Ω, $T_J$ = +70°C to an accuracy of ±15°C, unless otherwise noted. All temperature coefficients are measured at $T_J$ = +40°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| DUT_ Low-Leak Mode Leakage | | $V_{DUT\_}$ = 0V, 1.5V, 3V, $T_J$ < +90°C | -10 | | +10 | nA |
| | | $V_{CLV\_}$ = $V_{CHV\_}$ = 6.5V, $V_{DUT\_}$ = -1.5V, $T_J$ < +90°C | -10 | | +10 | |
| | | $V_{CLV\_}$ = $V_{CHV\_}$ = -1.5V, $V_{DUT\_}$ = 6.5V, $T_J$ < +90°C | -10 | | +10 | |
| DUT_ Combined Capacitance | | Driver in terminate mode (Note 4) | | 3.4 | 4.3 | pF |
| | | Driver in high impedance, PMU in high impedance | | 8 | | |
| Low-Leakage Enable Time | | $\overline{LLEAKP\_}$ low to DUT_ = low leak | | 20 | | µs |
| Low-Leakage Disable Time | | $\overline{LLEAKP\_}$ high to normal operation | | 20 | | µs |
| **POWER SUPPLY** | | | | | | |
| Positive Supply Voltage | $V_{CC}$ | | 9.5 | 9.75 | 10.5 | V |
| Negative Supply Voltage | $V_{EE}$ | | -5.2 | -4.75 | -4.5 | V |
| Logic Supply Voltage | $V_{DD}$ | | 2.7 | 3.3 | 5.0 | V |
| $V_{HHP}$ Supply Voltage | $V_{HHP}$ | | 17 | 17.5 | 18 | V |
| Positive Supply Current | $I_{CC}$ | (Note 51) | | 120 | 135 | mA |
| Negative Supply Current | $I_{EE}$ | (Note 51) | | 245 | 260 | mA |
| Logic Supply Current | $I_{DD}$ | (Note 51) | | 4.5 | 7 | mA |
| $V_{HHP}$ Supply Current | $I_H$ | (Note 51) | | 1.5 | 2.0 | mA |
| | | VHH mode, no load | | 45 | 50 | |
| Power Dissipation per Channel | | Includes CTV power at $V_{CTV1}$ = $V_{CTV2}$ = 1.4V (Note 51) | | 1.2 | 1.35 | W |
| **ANALOG INPUTS** | | | | | | |
| **DUT GROUND SENSE** | | | | | | |
| Input Range | $V_{DGS}$ | Relative to AGND (Note 52) | -150 | | +150 | mV |
| Input Bias Current | | $V_{DGS}$ = 0V | -10 | | +10 | µA |
| Gain | | DHV_, DLV_, DTV_, CPHV_, CPLV_, VHH_ | 0.985 | 0.990 | 1.005 | V/V |
| | | All other levels and MEAS_ output | 0.995 | 1.000 | 1.005 | |
| **2.5V REFERENCE** | | | | | | |
| Nominal Voltage | $V_{REF}$ | (Notes 53, 54) | | 2.5 | | V |
| Input Bias Current | | | -2 | | +2 | µA |
| **ANALOG BUS ($V_{DUT\_}$ = -1.5V to +6.5V, PMU-F = PMU-S = -1.5V to +6.5V, unless otherwise noted)** | | | | | | |
| PMU-F Switch | | $I_{SWITCH}$ = ±2.5mA, $V_{DUT\_}$ = -1.25V, 2.50V, 6.25V | | | 100 | Ω |
| PMU-S Switch | | $I_{SWITCH}$ = ±100µA, $V_{DUT\_}$ = -1.25V, 2.50V, 6.25V | | | 2.5 | kΩ |

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0V, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{CTV\_}$ = 1.4V, $V_{BV\_}$ = 4V, $V_{DGS}$ = $V_{GND}$ = 0V, $V_{CHV\_}$ = $V_{IVMAX\_}$ = 2V, $V_{CLV\_}$ = $V_{IVMIN\_}$ = 1V, $V_{COM\_}$ = 2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{IN\_}$ = 2.5V, $V_{VIOS}$ = 0V, $V_{IIOS}$ = 2.5V, $V_{CLAMPHI\_}$ = 5V, $V_{CLAMPLO\_}$ = 0V, $V_{HH\_}$ = 10V, CDRP = 0b001, RO = 0b1000, HYST = 0b000, $Z_{LOAD}$ = 50Ω, $T_J$ = +70°C to an accuracy of ±15°C, unless otherwise noted. All temperature coefficients are measured at $T_J$ = +40°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| PMU-S Switch | | $I_{SWITCH}$ = ±10µA, $V_{DUT\_}$ = 6.5V to 13V, $V_{PMU-F}$ = $V_{PMU-S}$ = 6.5V to 13V for $V_{HH}$ level calibration | | | 5 | kΩ |
| PMU-F Path Current | | | | | ±30 | mA |
| PMU-F, PMU-S On-Leakage | | F and S Independent, other channel switches off | -10 | ±5 | +10 | nA |
| PMU-F, PMU-S Off-Leakage | | | -10 | ±1 | +10 | nA |
| **DIFFERENTIAL COMPARATOR (DIFFERENTIAL_ = 1)** | | | | | | |
| **DC CHARACTERISTICS ($V_{CLV\_}$ = $V_{CHV\_}$ = 0V, unless otherwise noted)** | | | | | | |
| Input-Voltage Range | $V_{DUT0}$, $V_{DUT1}$ | (Notes 22, 55) | -1.5 | | +6.5 | V |
| Differential Threshold Voltage Range | CLV, CHV | Levels may be safely programmed beyond this range | -1 | | +1 | V |
| Differential Input Voltage | | (Notes 22, 23) | -8 | | +8 | V |
| Offset Error | | $V_{DUT\_}$ = 0V | -5 | | +5 | mV |
| Gain | | $V_{DUTn}$ = 0V, $V_{DUTm}$ = -1V, 1V | 0.998 | 1 | 1.002 | V/V |
| Linearity Error Relative to Straight Line from -1V to +1V | | $V_{DUTn}$ = 0V, $V_{DUTm}$ = -1V, -0.5V, 0, 0.5V, 1V | -5 | | +5 | mV |
| Hysteresis | | **HYST0 / HYST1 / HYST2** | | | | mV |
| | | 0 / 0 / 0 | | 0 | | |
| | | 0 / 0 / 1 | | 2 | | |
| | | 0 / 1 / 0 | | 4 | | |
| | | 0 / 1 / 1 | | 6 | | |
| | | 1 / 0 / 0 | | 8 | | |
| | | 1 / 0 / 1 | | 10 | | |
| | | 1 / 1 / 0 | | 12 | | |
| | | 1 / 1 / 1 | | 15 | | |
| Offset Temperature Coefficient | | $V_{DUTn}$ = 0V and $V_{DUTm}$ = -1V, 1V (Note 4) | -150 | | +150 | µV/°C |
| DC Power-Supply Rejection Ratio | | $V_{DUT\_}$ = 1.5V (Note 27) | 50 | 66 | | dB |
| Common-Mode Rejection Ratio | CMRR | $V_{DUT\_}$ = -1.5V and 6.5V, $V_{CLV\_}$ = $V_{CHV\_}$ = 0V (Note 25) | 50 | 55 | | dB |
| **AC CHARACTERISTICS ($V_{CHV\_}$ = $V_{CLV\_}$ = 0V, driver terminated, unless otherwise noted) (Note 4)** | | | | | | |
| Minimum Pulse Width | | (Note 31) | | 0.5 | 0.65 | ns |
| Propagation Delay | | | 0.5 | 1 | 1.5 | ns |
| Propagation-Delay Match H/L vs. L/H, Individual Comparator | | | -25 | | +25 | ps |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0V, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{CTV\_}$ = 1.4V, $V_{BV\_}$ = 4V, $V_{DGS}$ = $V_{GND}$ = 0V, $V_{CHV\_}$ = $V_{IVMAX\_}$ = 2V, $V_{CLV\_}$ = $V_{IVMIN\_}$ = 1V, $V_{COM\_}$ = 2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{IN\_}$ = 2.5V, $V_{VIOS}$ = 0V, $V_{IIOS}$ = 2.5V, $V_{CLAMPHI\_}$ = 5V, $V_{CLAMPLO\_}$ = 0V, $V_{HH\_}$ = 10V, CDRP = 0b001, RO = 0b1000, HYST = 0b000, $Z_{LOAD}$ = 50Ω, $T_J$ = +70°C to an accuracy of ±15°C, unless otherwise noted. All temperature coefficients are measured at $T_J$ = +40°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Change in Propagation Delay vs. Duty Cycle | | 500mV swing, 250mV overdrive, 2ns to 23ns pulse width, relative to PW = 12.5ns | | -45 | | +45 | ps |
| Propagation Delay vs. Common-Mode Voltage | | $V_{SWING}$ = 200mV, 100mV overdrive, common-mode voltage = -1.4V to +6.4V (Note 32) | | | | 70 | $ps_{P-P}$ |
| Propagation-Delay Temperature Coefficient | | | | | ±3 | | ps/°C |
| Propagation Delay vs. Slew Rate | | 1V/ns to 6V/ns, relative to 2V/ns | | | | ±50 | ps |
| Cable-Droop Compensation | | 1V swing, rise/fall time = 500ps | CDRP = 0b000 | | 0 | | % |
| | | | CDRP = 0b111 | | 10 | | |
| **DRIVER VHH** | | | | | | | |
| **DC CHARACTERISTICS** | | | | | | | |
| Output-Voltage Range | VHH | | | 0 | | 13 | V |
| DC Output Current | | VHH_ = 13V, $I_{DUT\_}$ = 10mA, $V_{DUT\_}$ > 12.25V | | +10 | | | mA |
| | | VHH_ = 0V, $I_{DUT\_}$ = -10mA, $V_{DUT\_}$ < 0.75V | | | | -10 | |
| Current Limit | | VHH_ = 13V, $V_{DUT\_}$ = 0V and VHH_ = 0V, $V_{DUT\_}$ = 13V | | ±11 | | ±25 | mA |
| Offset Voltage | | VHH_ = 8V | | | | ±30 | mV |
| Gain | | VHH_ = 8V, 12V | | 0.998 | 1 | 1.002 | V/V |
| Linearity Relative to 8V, 12V | | VHH_ = 7V, 8V, 10V, 12V, 13V | | | | ±10 | mV |
| Linearity Relative to 2V, 12V | | VHH_ = 0, 2V, 4V, 8V 12V, 13V | | | | ±30 | mV |
| Output Resistance | | $I_{DUT\_}$ = ±2mA, VHH_ = 1V | | | | 75 | Ω |
| Output-Voltage Temperature Coefficient | | VHH_ = 7V to 13V (Note 4) | | | ±75 | ±500 | µV/°C |
| **AC CHARACTERISTICS ($R_L$ ≥ 10MΩ, $C_{DUT\_}$ = 100pF)** | | | | | | | |
| VHH Rise/Fall Times | | $V_{DHV\_}$ = 3V, VHH_ = 13V, 10% to 90% | | | | 170 | ns |
| VHH Overshoot (Note 4) | | $V_{DHV\_}$ = 3V to VHH_ = 13V rise | | | | 150 | mV |
| | | VHH_ = 13V to $V_{DHV\_}$ = 3V fall | | | | 200 | |
| **LEVEL DACs** | | | | | | | |
| Settling Time | | Full-scale transition to within 5mV | | | 20 | | µs |
| Differential Nonlinearity | | $I_{SOURCE}$ (VLDH_), $I_{SINK}$ (VLDL_) | | | | ±3.5 | µA |
| | | VHH_, IIOS | | | | ±2 | mV |
| | | All other levels | | | | ±1 | mV |

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0V, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{CTV\_}$ = 1.4V, $V_{BV\_}$ = 4V, $V_{DGS}$ = $V_{GND}$ = 0V, $V_{CHV\_}$ = $V_{IVMAX\_}$ = 2V, $V_{CLV\_}$ = $V_{IVMIN\_}$ = 1V, $V_{COM\_}$ = 2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{IN\_}$ = 2.5V, $V_{VIOS}$ = 0V, $V_{IIOS}$ = 2.5V, $V_{CLAMPHI\_}$ = 5V, $V_{CLAMPLO\_}$ = 0V, $V_{HH\_}$ = 10V, CDRP = 0b001, RO = 0b1000, HYST = 0b000, $Z_{LOAD}$ = 50Ω, $T_J$ = +70°C to an accuracy of ±15°C, unless otherwise noted. All temperature coefficients are measured at $T_J$ = +40°C to +100°C, unless otherwise noted.) (Note 1)

**Note 1:** Unless otherwise specified, all minimum and maximum specifications are production tested. All other specification test limits are guaranteed by design. All tests are performed at nominal supply voltages and after gain and offset calibration, unless otherwise specified.

**Note 2:** Guaranteed by the associated linearity test.

**Note 3:** Change in offset at any voltage over the operating range. Specification includes both gain and offset temperature effects. Limits have been simulated over the entire operating range and verified at worst-case conditions ($V_{DHV\_}$ - $V_{DLV\_}$ > 200mV).

**Note 4:** Guaranteed by design and characterization.

**Note 5:** $V_{CC}$ and $V_{EE}$ independently varied over their full range.

**Note 6:** DATA_ = 1V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, $I_{OUT}$ = ±30mA. Different values within the range of 48Ω to 52Ω are available by custom trimming (contact factory).

**Note 7:** Resistance measurements are made using ±2.5mA current changes in the loading instrument about the noted value. Absolute value of the difference in measured resistance at the specified points, tested separately for each current polarity.

**Note 8:** Rise time, unless otherwise specified for the differential inputs DATA_ and RCV_, is 250ps (10% to 90%) at 40MHz. (These conditions are for bench characterization. Final test conditions may differ from bench.)

**Note 9:** ±8V step into AC-coupled 10Ω load. Current supplied for a minimum of 10ns. Guaranteed by design to be greater than or equal to DC drive current.

**Note 10:** $V_{DTV\_}$ = 1.5V, $R_S$ = 50Ω. External signal driven into a transmission line to produce a 0 to 3V edge at the comparator input with a 600ps rise time (10% to 90%). Measurement point is at the comparator input.

**Note 11:** Measured between the 90% point of the driver output (relative to its final value) and the waveform settling to within the specified limit.

**Note 12:** Propagation delays are measured from the crossing point of the differential input signals to the 50% point of expected output swing.

**Note 13:** Average of two measurements for propagation-delay match, $t_{LH}$ vs. $t_{HL}$.

**Note 14:** Four measurements are made: DHV_ to high impedance, DLV_ to high impedance, high impedance to DHV_, and high impedance to DLV_. The worst of the four measurements is reported.

**Note 15:** Average of four measurements of propagation-delay match, drive to high impedance vs. high impedance to drive. Measured from the crossing point of RCV/NRCV to the 50% point of the output waveform.

**Note 16:** Average of four measurements for propagation-delay match, drive to term vs. term to drive. Measured from the crossing point of RCV/NRCV to the 50% point of the output waveform.

**Note 17:** Four measurements are made: DHV_ to DTV_, DLV_ to DTV_, DTV_ to DHV_, and DTV_ to DLV_. The worst-case difference is reported.

**Note 18:** Propagation-delay change is reported with respect to a 5ns pulse width.

**Note 19:** At this pulse width, the output reaches at least 95% of its nominal (DC) amplitude. The pulse width is measured at DATA_ and NDATA_.

**Note 20:** Maximum data rate in transitions/second. A waveform that reaches at least 95% of its programmed amplitude may be generated at half of this frequency.

**Note 21:** Maximum data rate in transitions/second. A waveform that reaches at least 90% of its programmed amplitude may be generated at half of this frequency.

**Note 22:** The comparators tolerate the $V_{HH}$ produced by the driver; however, the specifications only apply to the -1.5V to +6.5V input range.

**Note 23:** This specification is implicitly tested, by meeting the high-impedance leakage specification.

**Note 24:** Change in offset at any voltage over operating range. Includes both gain (CMRR) and offset temperature effects.

**Note 25:** Change in offset voltage over the input range.

**Note 26:** Relative to straight line between 0 and 3V.

**Note 27:** Change in offset voltage with power supplies independently varied over their full range. Both high and low comparators are tested.

**Note 28:** All propagation delays measured from $V_{DUT\_}$ crossing calibrated CHV_/CLV_ threshold to crossing point of differential outputs.

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0V, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{CTV\_}$ = 1.4V, $V_{BV\_}$ = 4V, $V_{DGS}$ = $V_{GND}$ = 0V, $V_{CHV\_}$ = $V_{IVMAX\_}$ = 2V, $V_{CLV\_}$ = $V_{IVMIN\_}$ = 1V, $V_{COM\_}$ = 2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{IN\_}$ = 2.5V, $V_{VIOS}$ = 0V, $V_{IIOS}$ = 2.5V, $V_{CLAMPHI\_}$ = 5V, $V_{CLAMPLO\_}$ = 0V, $V_{HH\_}$ = 10V, CDRP = 0b001, RO = 0b1000, HYST = 0b000, $Z_{LOAD}$ = 50Ω, $T_J$ = +70°C to an accuracy of ±15°C, unless otherwise noted. All temperature coefficients are measured at $T_J$ = +40°C to +100°C, unless otherwise noted.) (Note 1)

**Note 29:** All delay specifications are measured with DUT_ (comparator input) as the reference.

**Note 30:** 40MHz, 0 to 1V input to comparator, reference = 0.5V, 50% duty cycle, 250ps rise/fall time, $Z_S$ = 50Ω, driver in term mode with $V_{DTV\_}$ = 0V, and hysteresis disabled, unless otherwise specified.

**Note 31:** At this pulse width, the output reaches at least 90% of its nominal peak-to-peak swing. The pulse width is measured at the crossing points of the differential outputs. 250ps rise/fall time at DUT_. Timing dispersion specifications are not guaranteed.

**Note 32:** $V_{DUT\_}$ = 200mVP-P, rise/fall time = 150ps, overdrive = 100mV, $V_{DTV\_}$ = $V_{CM}$. Valid for common-mode ranges where the signal does not exceed the operating range. Specification is worst case (slowest–fastest) over the specified range.

**Note 33:** For any input slew rate up to 6V/ns, no unusual behavior should be exhibited (i.e., glitching, changing polarity, etc.).

**Note 34:** Input to comparator is 40MHz at 0 to 1V, 50% duty cycle, 250ps 10% to 90% rise time. EQ bandwidth = 0.22/($t_{TCMP}$^2 + $t_{TINPUT}$^2)^(1/2) where $t_{TINPUT}$ and $t_{TCMP}$ are the 20% to 80% transition time of the comparator input and reconstructed output.

**Note 35:** Resistance measurements are made using ±2.5mA current changes in the loading instrument. Value reported is the absolute value of the difference in measured resistance over the specified range, tested separately for each current polarity.

**Note 36:** Stimulus is 0 to 3V, 2.5V/ns square wave from far end of 3ns transmission line with $R_S$ = 25Ω, clamps set to 0 and 3V.

**Note 37:** Change in offset over the entire operating range. Includes both gain and offset temperature effects.

**Note 38:** Interpretation of errors are expressed in terms of %FSR (percent of full-scale range) as a percentage of the end-point-to-end-point range (i.e., for the ±2mA range, the full-scale range = 4mA and a 1% error = 40µA).

**Note 39:** With clamps enabled, the linear DUT_ current range for force voltage is defined by the clamp-current-range specification, and the linear DUT_ voltage range for force current is defined by the linear FI $V_{DUT\_}$ range specification.

**Note 40:** For currents greater than +FSR/2, $V_{MEAS}$ is greater than $V_{IIOS}$ + 4V and for currents less than -FSR/2, $V_{MEAS}$ is less than $V_{IIOS}$ - 4V.

**Note 41:** This current is supplied by the driver.

**Note 42:** $V_{VIOS}$ may be programmed to greater than 1.5V to a maximum value of 2.5V; however, the maximum valid $V_{DUT\_}$ value must be reduced below 6.5V, as the maximum MEAS output is limited to 8V. Because $V_{MEAS\_}$ = $V_{DUT\_}$ + $V_{VIOS}$, then $V_{DUT\_MAX}$ = 8V - $V_{VIOS}$ when $V_{VIOS}$ > 1.5V.

**Note 43:** Guaranteed by driver VHH_ and DLV_ linearity tests.

**Note 44:** IVMAX and IVMIN do not have separate calibration registers for MI and MV modes. Specifications apply with calibration for each mode.

**Note 45:** Guaranteed by the associated accuracy test.

**Note 46:** The digital interface is compatible with 2.7V ≤ $V_{DD}$ ≤ 5V CMOS logic.

**Note 47:** See the *Typical Operating Characteristics* section.

**Note 48:** FIMV settling times are a function of $C_{DUT\_}$ and $R_{RANGE}$. Increased DUT_ capacitance will increase settling time.

**Note 49:** The propagation delay time is guaranteed only over the force-voltage output range. Propagation delay is measured by holding $V_{SENSE\_}$ steady and transitioning IVMAX_ or IVMIN_.

**Note 50:** Default configuration has internal 100Ω resistors between DATA and NDATA, RCV and NRCV. Resistor terminations from DATA, NDATA, RCV, and NRCV to a separate pin are available by special request.

**Note 51:** At nominal supply voltages. Total current for dual device. $R_L$ ≥ 10MΩ.

**Note 52:** Increasing DGS beyond 0V requires a proportional increase in the minimum supply levels. Specified ranges for all DAC output levels are defined with respect to DGS.

**Note 53:** The error of the external 2.5V reference impacts the accuracy of the DAC levels; a 1% error in the 2.5V reference will translate to a 1% error in the DAC level gain. Use a precision voltage reference, such as the MAX6225.

**Note 54:** Generate the 2.5V external reference with respect to DGS (DUT ground sense).

**Note 55:** Guaranteed by associated CMRR_ test.

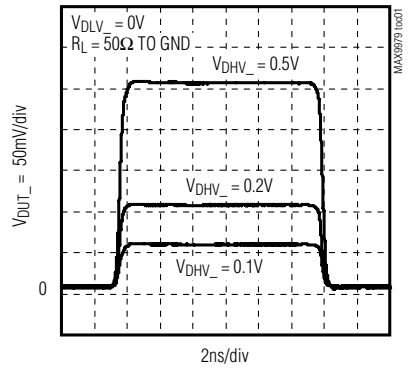
**Note 56:** The comparator outputs are normally source side-terminated with 50Ω on-die to CTV_ and at the receive side of the transmission path. The comparator outputs are tested with the 50Ω on-die source resistors only with limits relative to CTV_ twice the values indicated.

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

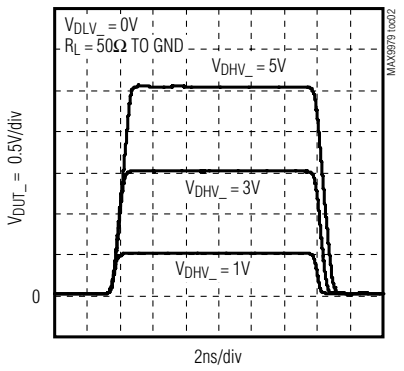
## Typical Operating Characteristics

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $R_T$ = 50Ω ll 1pF, $C_L$ = 100pF, CTV_ = 1.4V, $T_J$ = +70°C, unless otherwise specified. All temperature coefficients are measured at $T_J$ = +40°C to +100°C.)

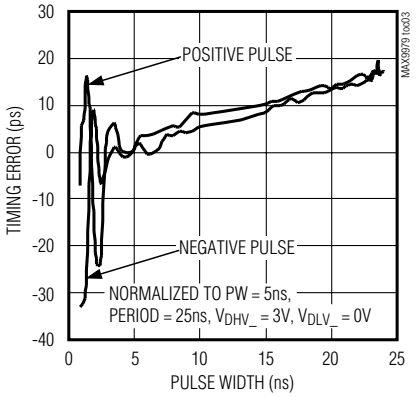
**DRIVER SMALL-SIGNAL RESPONSE**



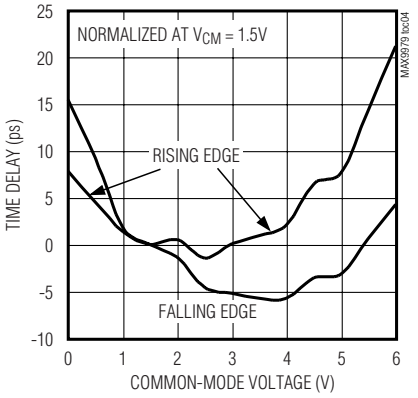

**DRIVER LARGE-SIGNAL RESPONSE**



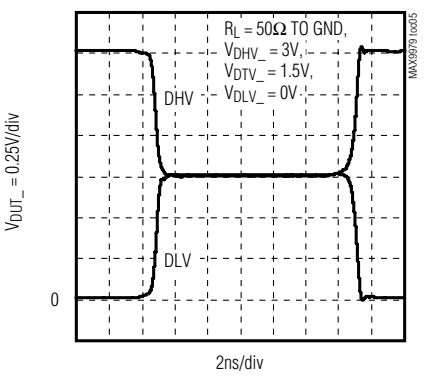

**DRIVER TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH**



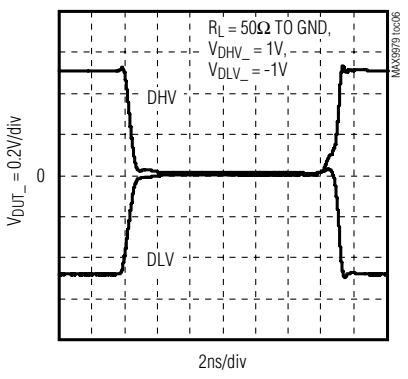

**DRIVER TIME DELAY vs. COMMON-MODE VOLTAGE**



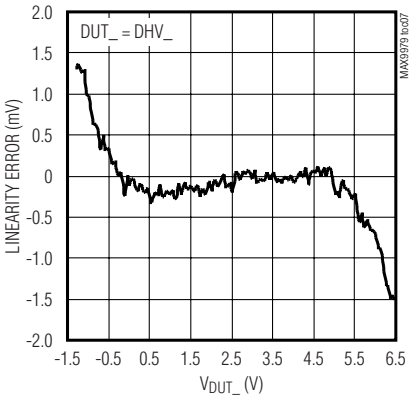

**DRIVER-TO-TERM TRANSITION**



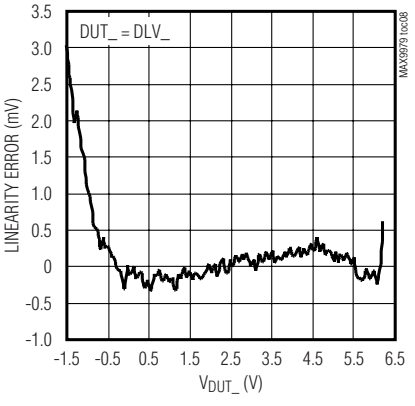

**DRIVER TO HIGH-IMPEDANCE TRANSITION**




**DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE**



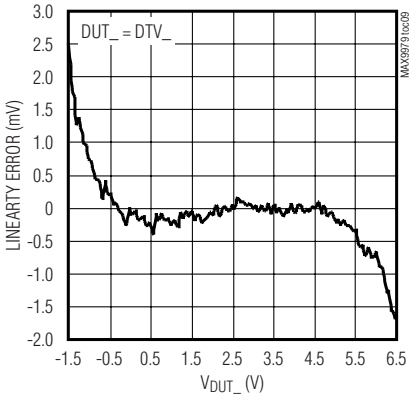

**DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE**



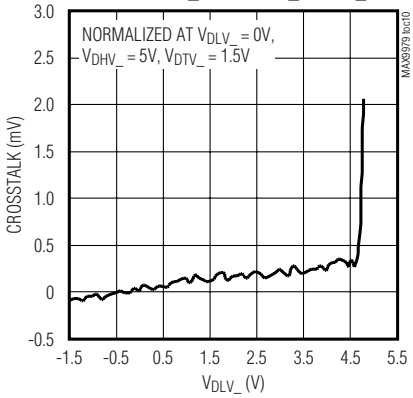
## Typical Operating Characteristics (continued)

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $R_T$ = 50Ω ll 1pF, $C_L$ = 100pF, CTV_ = 1.4V, $T_J$ = +70°C, unless otherwise specified. All temperature coefficients are measured at $T_J$ = +40°C to +100°C.)

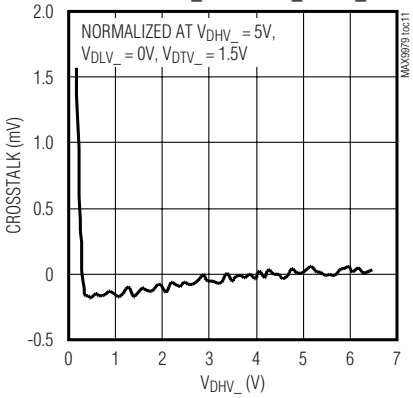
**DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE**



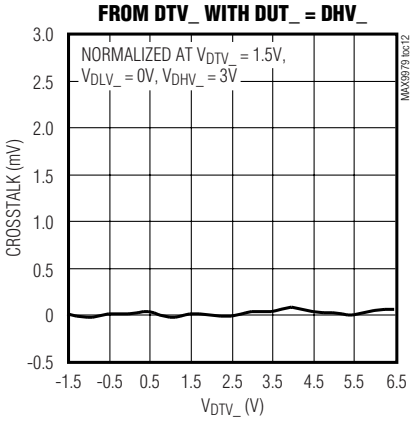

**CROSSTALK TO DUT_ FROM DLV_ WITH DUT_ = DHV_**



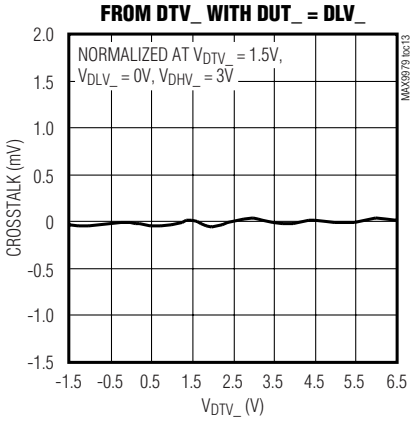

**CROSSTALK TO DUT_ FROM DHV_ WITH DUT_ = DLV_**



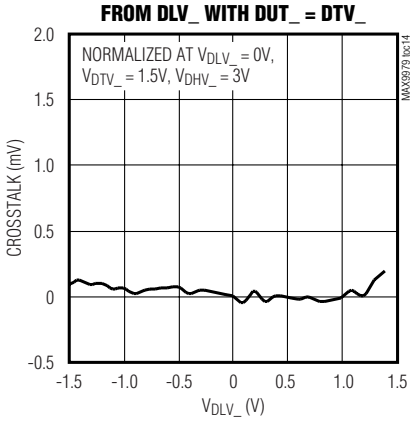

**CROSSTALK TO DUT_ FROM DTV_ WITH DUT_ = DHV_**



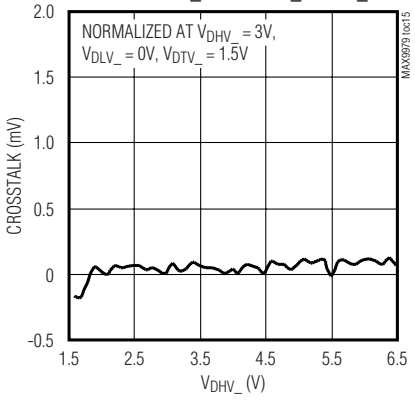

**CROSSTALK TO DUT_ FROM DTV_ WITH DUT_ = DLV_**



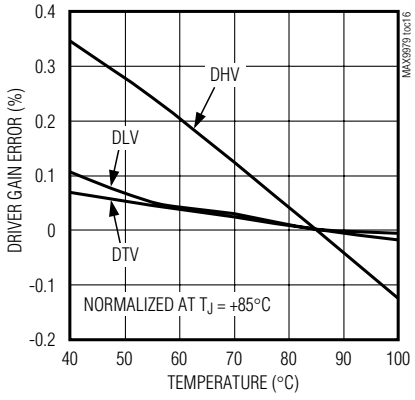

**CROSSTALK TO DUT_ FROM DLV_ WITH DUT_ = DTV_**




**CROSSTALK TO DUT_ FROM DHV_ WITH DUT_ = DTV_**




**DRIVER GAIN ERROR vs. TEMPERATURE**



# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

## Typical Operating Characteristics (continued)

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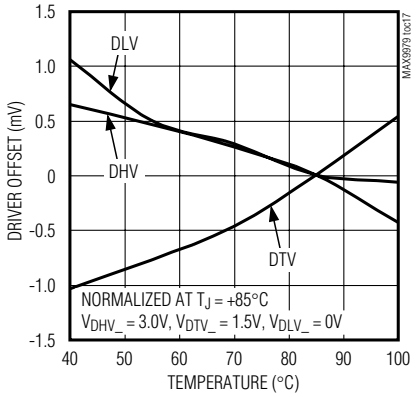
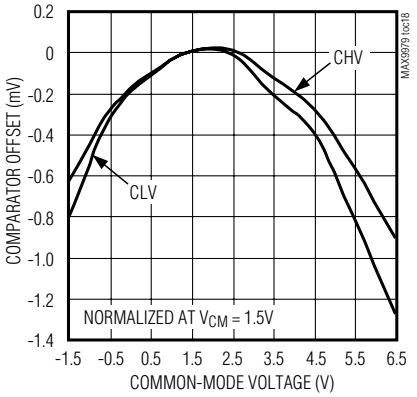
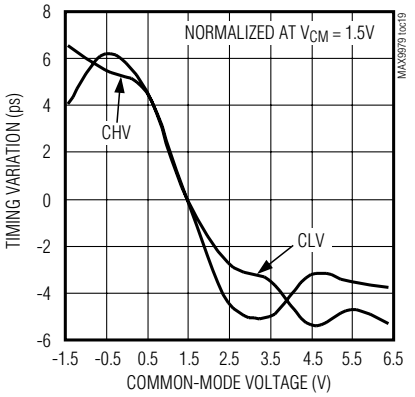
**DRIVER OFFSET vs. TEMPERATURE**



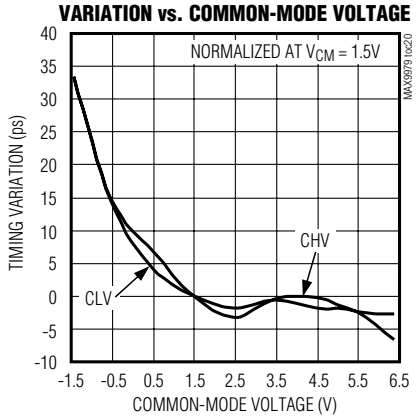

**COMPARATOR OFFSET vs. COMMON-MODE VOLTAGE**



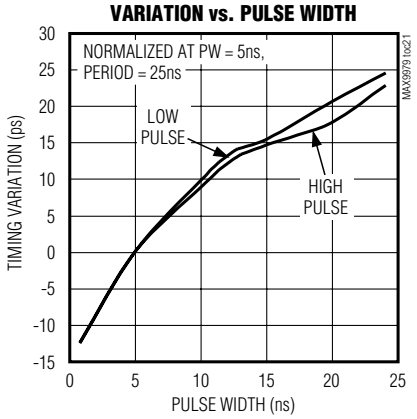

**COMPARATOR RISING-EDGE TIMING VARIATION vs. COMMON-MODE VOLTAGE**



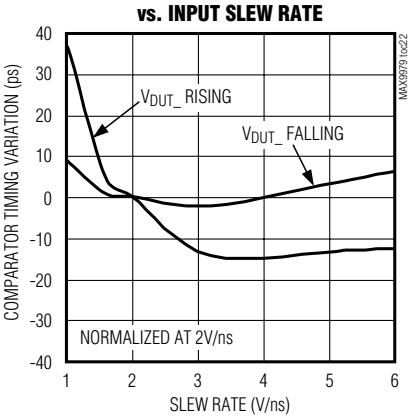

**COMPARATOR FALLING-EDGE TIMING VARIATION vs. COMMON-MODE VOLTAGE**



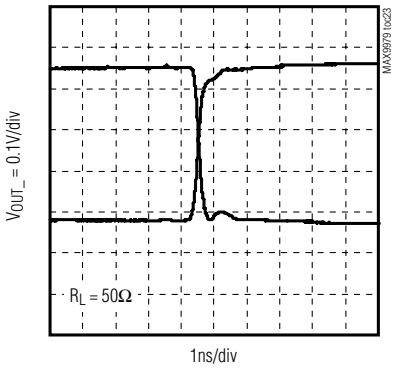

**COMPARATOR TRAILING-EDGE TIMING VARIATION vs. PULSE WIDTH**



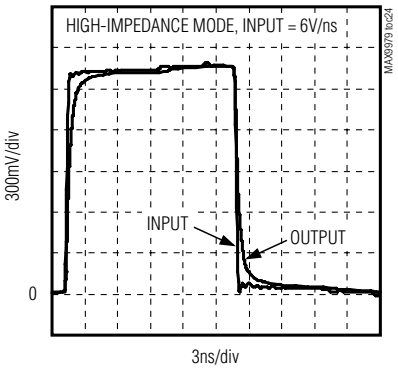

**COMPARATOR TIMING VARIATION vs. INPUT SLEW RATE**




**COMPARATOR DIFFERENTIAL OUTPUT RESPONSE**




**COMPARATOR RESPONSE TO HIGH SLEW-RATE INPUT**



## Typical Operating Characteristics (continued)

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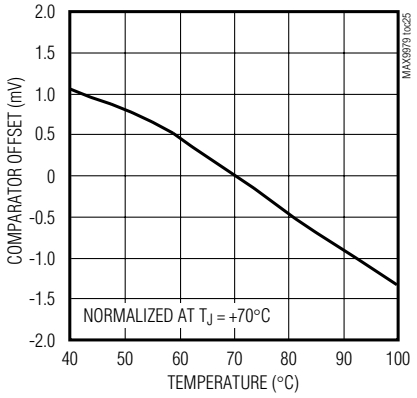
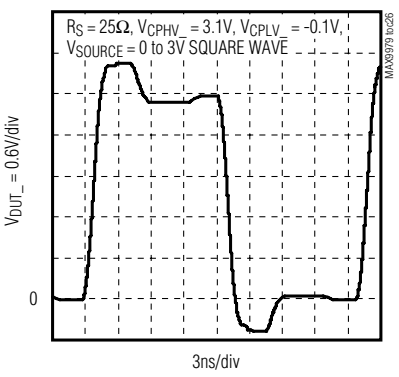
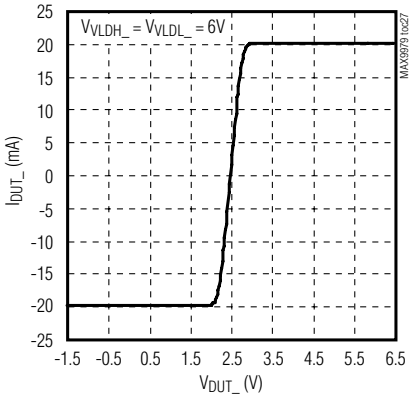
**COMPARATOR OFFSET vs. TEMPERATURE**



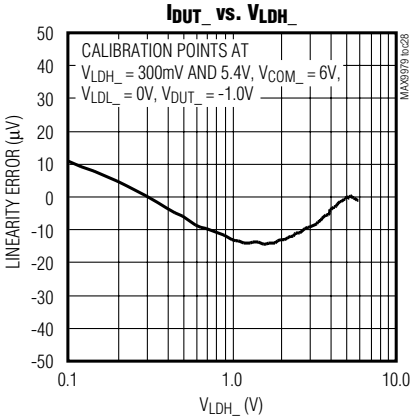

**CLAMP RESPONSE AT SOURCE**



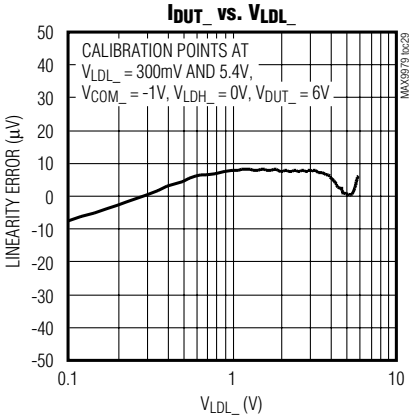

**ACTIVE LOAD CURRENT vs. VOLTAGE**



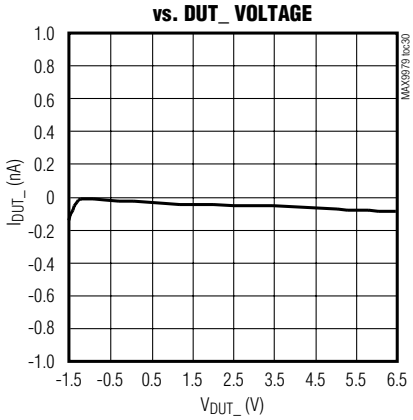

**ACTIVE-LOAD LINEARITY ERROR IDUT_ vs. VLDH_**



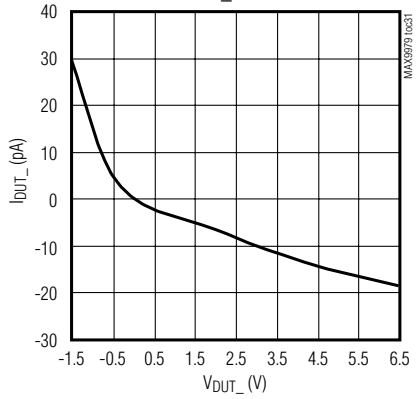

**ACTIVE LOAD LINEARITY ERROR IDUT_ vs. VLDL_**



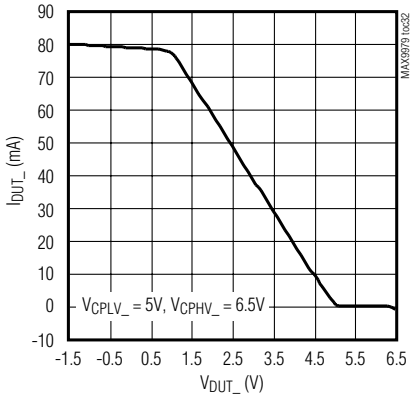

**HIGH-IMPEDANCE LEAKAGE CURRENT vs. DUT_ VOLTAGE**




**LOW-LEAKAGE CURRENT vs. DUT_ VOLTAGE**




**HIGH-IMPEDANCE CLAMP CURRENT vs. DIFFERENCE VOLTAGE**



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## Typical Operating Characteristics (continued)

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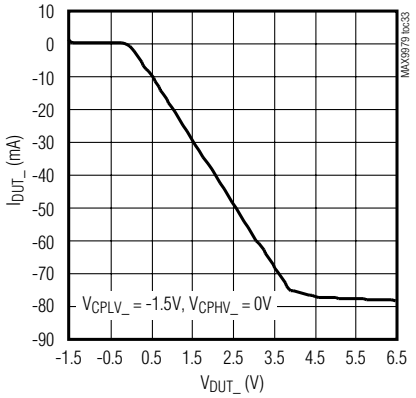
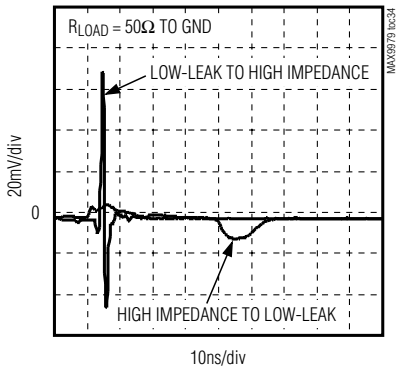
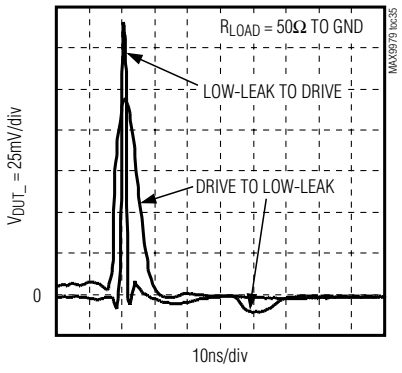
**HIGH-IMPEDANCE CLAMP CURRENT vs. DIFFERENCE VOLTAGE**



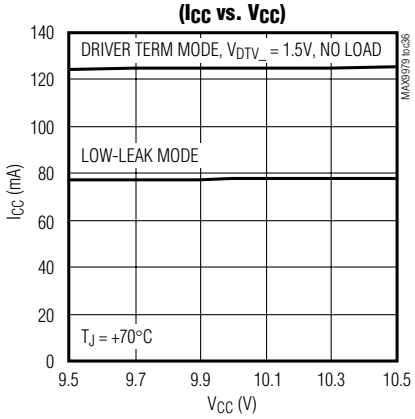

**HIGH IMPEDANCE TO LOW-LEAK TRANSITION**



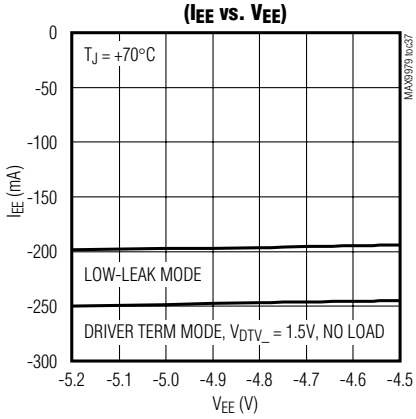

**DRIVE TO LOW-LEAK TRANSITION**



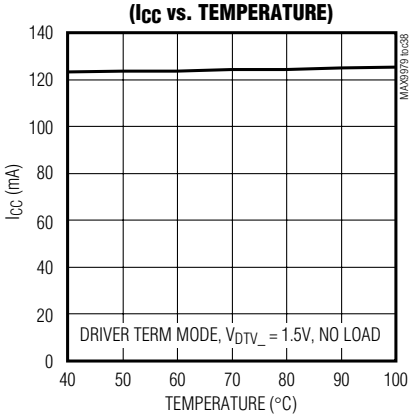

**SUPPLY CURRENT ($I_{CC}$ vs. $V_{CC}$)**



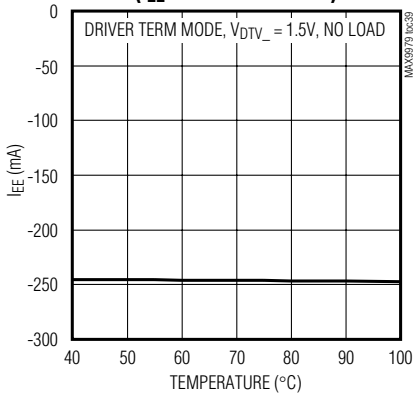

**SUPPLY CURRENT ($I_{EE}$ vs. $V_{EE}$)**



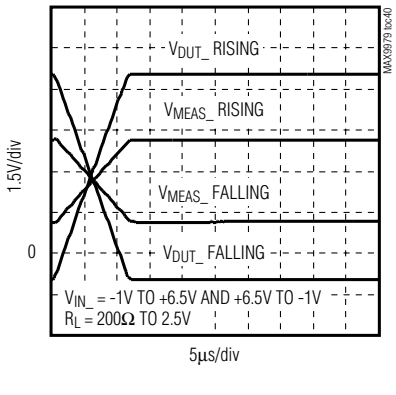

**SUPPLY CURRENT ($I_{CC}$ vs. TEMPERATURE)**




**SUPPLY CURRENT ($I_{EE}$ vs. TEMPERATURE)**




**TRANSIENT RESPONSE FVMI RANGE A**



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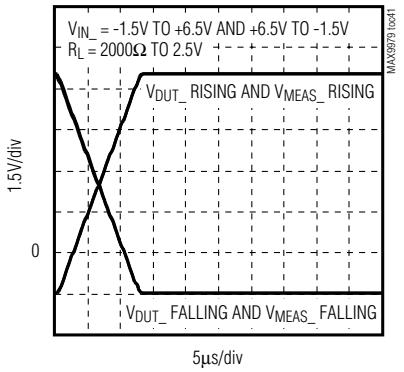
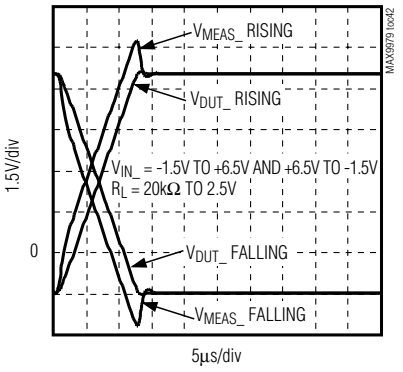
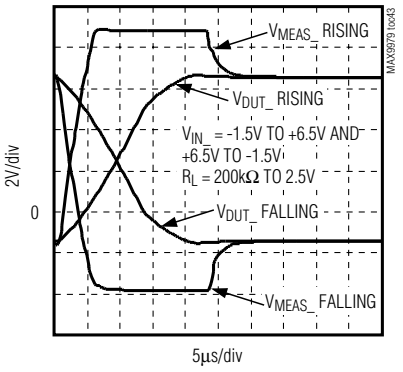
**TRANSIENT RESPONSE FVMI RANGE B**



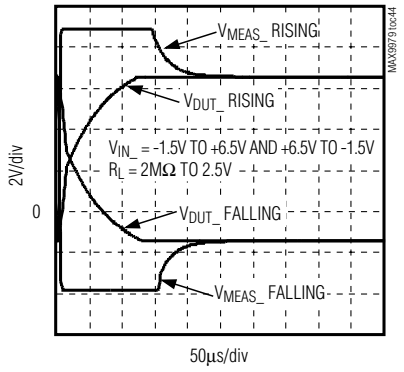

**TRANSIENT RESPONSE FVMI RANGE C**



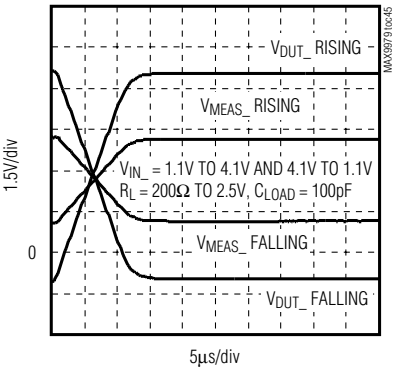

**TRANSIENT RESPONSE FVMI RANGE D**



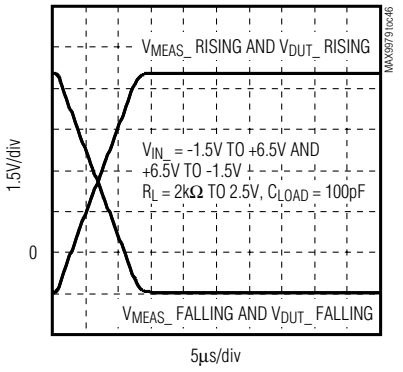

**TRANSIENT RESPONSE FVMI RANGE E**



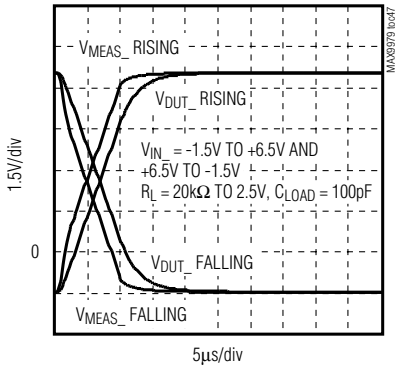

**TRANSIENT RESPONSE FIMI RANGE A**



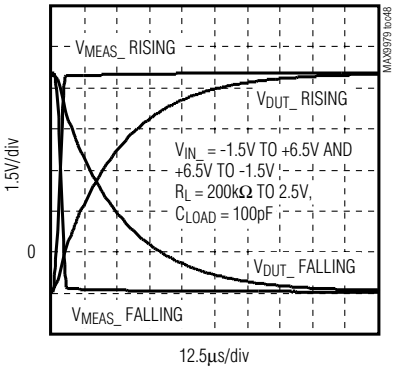

**TRANSIENT RESPONSE FIMI RANGE B**




**TRANSIENT RESPONSE FIMI RANGE C**




**TRANSIENT RESPONSE FIMI RANGE D**

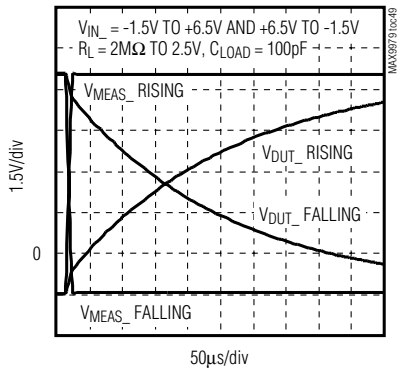


# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

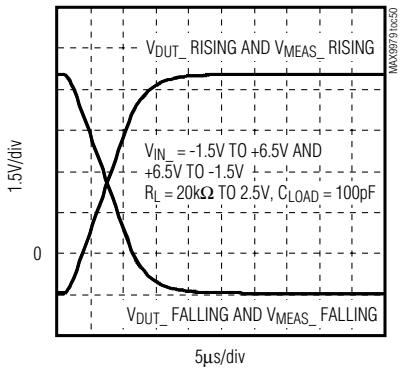
## Typical Operating Characteristics (continued)

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $R_T$ = 50Ω ll 1pF, $C_L$ = 100pF, CTV_ = 1.4V, $T_J$ = +70°C, unless otherwise specified. All temperature coefficients are measured at $T_J$ = +40°C to +100°C.)

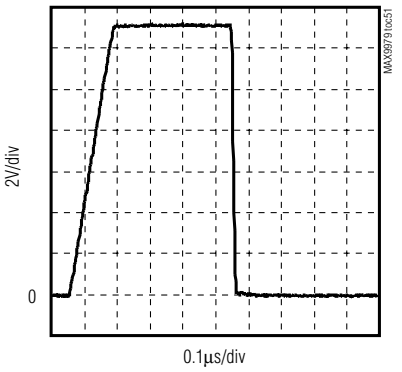
**TRANSIENT RESPONSE FIMI RANGE E**



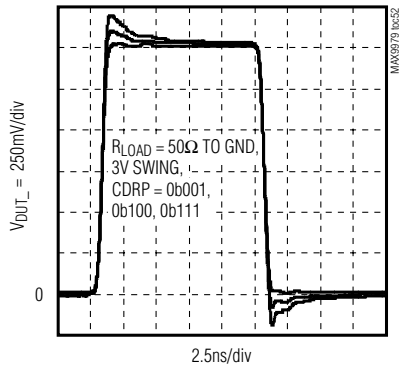

**TRANSIENT RESPONSE FIMV RANGE C**



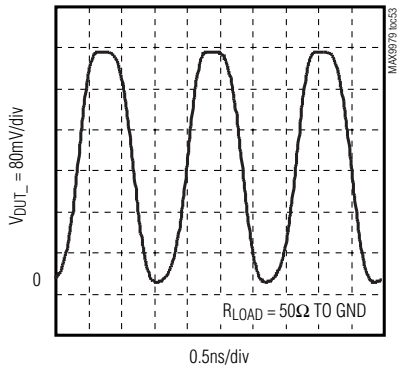

**TRANSIENT RESPONSE VHH**



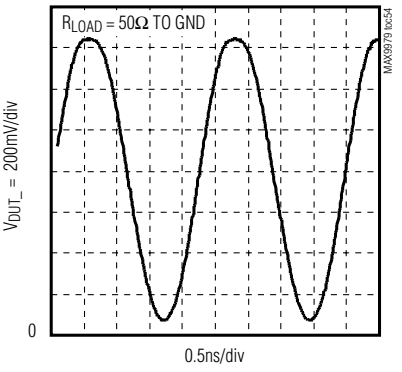

**DRIVER CABLE-DROOP COMPENSATION**



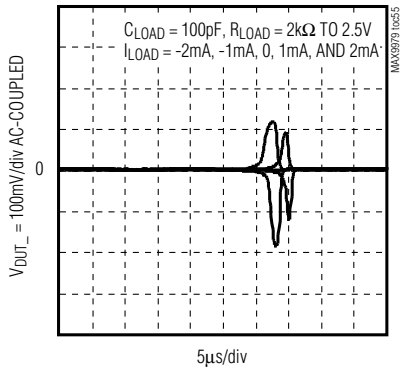

**DRIVER 1.2Gbps TOGGLE RATE, 1V**



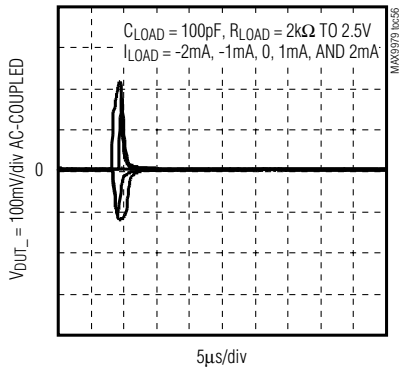

**DRIVER 900Mbps TOGGLE RATE, 3V**




**PMU RANGE CHANGE A TO B**



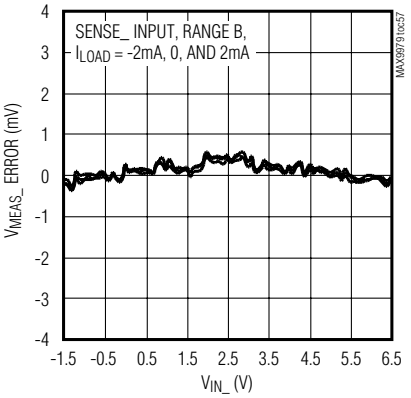

**PMU RANGE CHANGE B TO A**



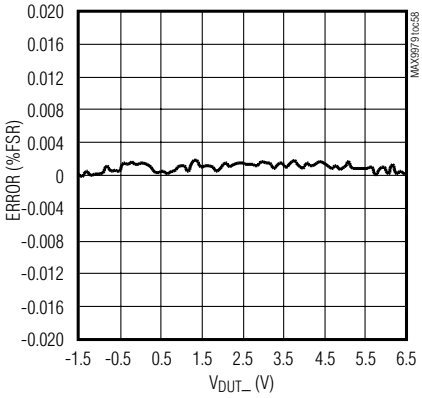
## Typical Operating Characteristics (continued)

($V_{CC}$ = 9.75V, $V_{EE}$ = -4.75V, $V_{DD}$ = 3.3V, $V_{HHP}$ = 17.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $R_T$ = 50Ω ll 1pF, $C_L$ = 100pF, CTV_ = 1.4V, $T_J$ = +70°C, unless otherwise specified. All temperature coefficients are measured at $T_J$ = +40°C to +100°C.)

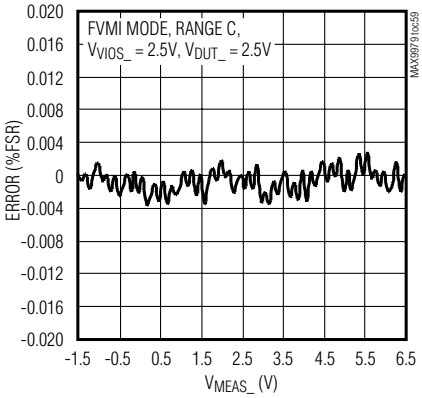
**PMU FV LINEARITY**



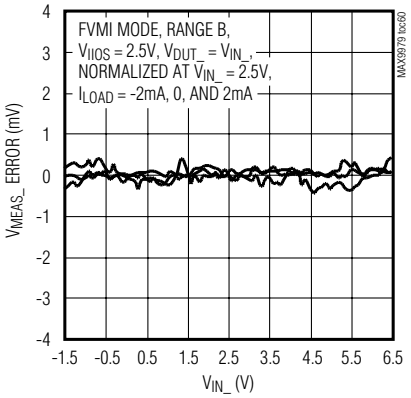

**PMU MV LINEARITY**



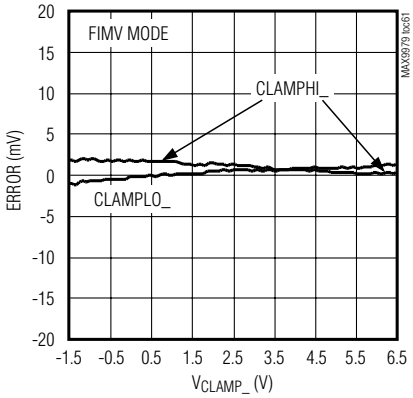

**PMU MI LINEARITY**



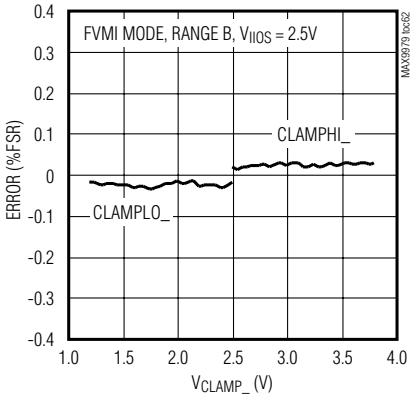

**PMU MI COMMON-MODE RESPONSE**




**PMU VOLTAGE CLAMP ACCURACY**




**PMU CURRENT CLAMP ACCURACY**



# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

## Pin Description

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | MEAS0 | Channel 0 Measure Output |
| 2 | DUTHI0 | Channel 0 PMU High Comparator Output |
| 3 | DUTLO0 | Channel 0 PMU Low Comparator Output |
| 4 | REF | DAC Reference Input |
| 5 | DGS | DUT Ground Sense Input |
| 6, 35, 51 | GND | Analog Ground |
| 7 | DOUT | Data Output. Serial-interface data output. |
| 8 | DGND | Digital Ground |
| 9 | $\overline{CS}$ | Chip-Select Input |
| 10 | SCLK | Serial-Clock Input |
| 11 | DIN | Data Input. Serial-interface data input. |
| 12 | $V_{DD}$ | Digital Power Supply |
| 13 | $\overline{LOAD}$ | Load Input. Serial-interface asynchronous load control. |
| 14 | $\overline{RST}$ | Reset Input. Serial-interface reset. |
| 15 | DUTLO1 | Channel 1 PMU Low Comparator Output |
| 16 | DUTHI1 | Channel 1 PMU High Comparator Output |
| 17 | MEAS1 | Channel 1 Measure Output |
| 18, 37, 40, 46, 49, 68 | $V_{CC}$ | Positive Power Supply |
| 19, 36, 39, 47, 50, 67 | $V_{EE}$ | Negative Power Supply |
| 20 | $\overline{HIZMEASP1}$ | Channel 1 High-Impedance Enable Input for PMU Measure Output |
| 21 | $\overline{LLEAKP1}$ | Channel 1 Low-Leak Enable Input |
| 22 | NRCV1 | Channel 1 Negative Receive Multiplexer Control Input |
| 23 | RCV1 | Channel 1 Positive Receive Multiplexer Control Input |
| 24 | BV1 | Channel 1 Bias Voltage Input |
| 25 | NDATA1 | Channel 1 Negative Data Multiplexer Control Input |
| 26 | DATA1 | Channel 1 Positive Data Multiplexer Control Input |
| 27 | $\overline{ENVHHP1}$ | Channel 1 High-Voltage Mode Enable Input |
| 28 | NCL1 | Channel 1 Negative Low Comparator Output |
| 29 | CL1 | Channel 1 Positive Low Comparator Output |
| 30 | CTV1 | Channel 1 Comparator Termination Voltage |
| 31 | NCH1 | Channel 1 Negative High Comparator Output |
| 32 | CH1 | Channel 1 Positive High Comparator Output |
| 33 | SENSE1 | Channel 1 PMU Sense Input |
| 34, 42, 52 | N.C. | No Connection. Not internally connected. |
| 38 | DUT1 | Channel 1 DUT Connection |

## Pin Description (continued)

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 41 | TEMP | Temperature Output |
| 43 | $V_{HHP}$ | High-Voltage Power Supply |
| 44 | PMU-F | PMU External Force Connection |
| 45 | PMU-S | PMU External Sense Connection |
| 48 | DUT0 | Channel 0 DUT Connection |
| 53 | SENSE0 | Channel 0 PMU Sense Input |
| 54 | CH0 | Channel 0 Positive High Comparator Output |
| 55 | NCH0 | Channel 0 Negative High Comparator Output |
| 56 | CTV0 | Channel 0 Comparator Termination Voltage |
| 57 | CL0 | Channel 0 Positive Low Comparator Output |
| 58 | NCL0 | Channel 0 Negative Low Comparator Output |
| 59 | $\overline{ENVHHP0}$ | Channel 0 High-Voltage Mode Enable Input |
| 60 | DATA0 | Channel 0 Positive Data Multiplexer Control Input |
| 61 | NDATA0 | Channel 0 Negative Data Multiplexer Control Input |
| 62 | BV0 | Channel 0 Bias Voltage Input |
| 63 | RCV0 | Channel 0 Positive Receive Multiplexer Control Input |
| 64 | NRCV0 | Channel 0 Negative Receive Multiplexer Control Input |
| 65 | $\overline{LLEAKP0}$ | Channel 0 Low-Leak Enable Input |
| 66 | $\overline{HIZMEASP0}$ | Channel 0 High-Impedance Enable Input For PMU Measure Output |
| — | EP | Exposed Pad. Internally connected to ground. Connect to a large open copper PCB plane or heatsink to maximize thermal performance. Not intended as an electrical connection point. |

## Detailed Description

The MAX9979 dual-channel pin electronics DCL/PMU integrates multiple pin-electronics functions into a single IC. Each channel includes a four-level pin driver, a window comparator, a differential comparator, dynamic clamps, a versatile PMU, an active load, and 14 independent 16-bit level-setting DACs. Additionally, each channel of the MAX9979 features programmable cable-droop compensation for the driver output and for the comparator input, adjustable driver output resistance, and driver slew-rate adjustment.

The MAX9979 driver features a wide -1.5V to +6.5V high-speed operating range, high-impedance and active-termination (3rd-level drive) modes, and is highly linear even at low voltage swings. The MAX9979 also features a built-in super voltage (VHH) level up to 13V. The driver provides high-speed differential control inputs compatible with most high-speed logic families. The window comparators provide extremely low timing variation over changes in slew rate, pulse width, or overdrive voltage, and have 50Ω source outputs internally terminated to an applied voltage at CTV_. When high-impedance mode is selected, the programmable dynamic clamps provide damping of high-speed DUT waveforms. The 20mA active load facilitates fast contact testing when used in conjunction with the comparators, and functions as a pullup for open-drain/collector DUT outputs. The PMU offers five current ranges from ±2µA to ±50mA and can force and measure current or voltage. Placing the MAX9979 DUT_ output into its very low-leakage state disables the DCL functions and the PMU force function. This feature is convenient for making IDDQ measurements without the need for an output disconnect relay. Low-leakage control is independent for each channel. An SPI-compatible serial interface and external inputs configure the MAX9979.

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

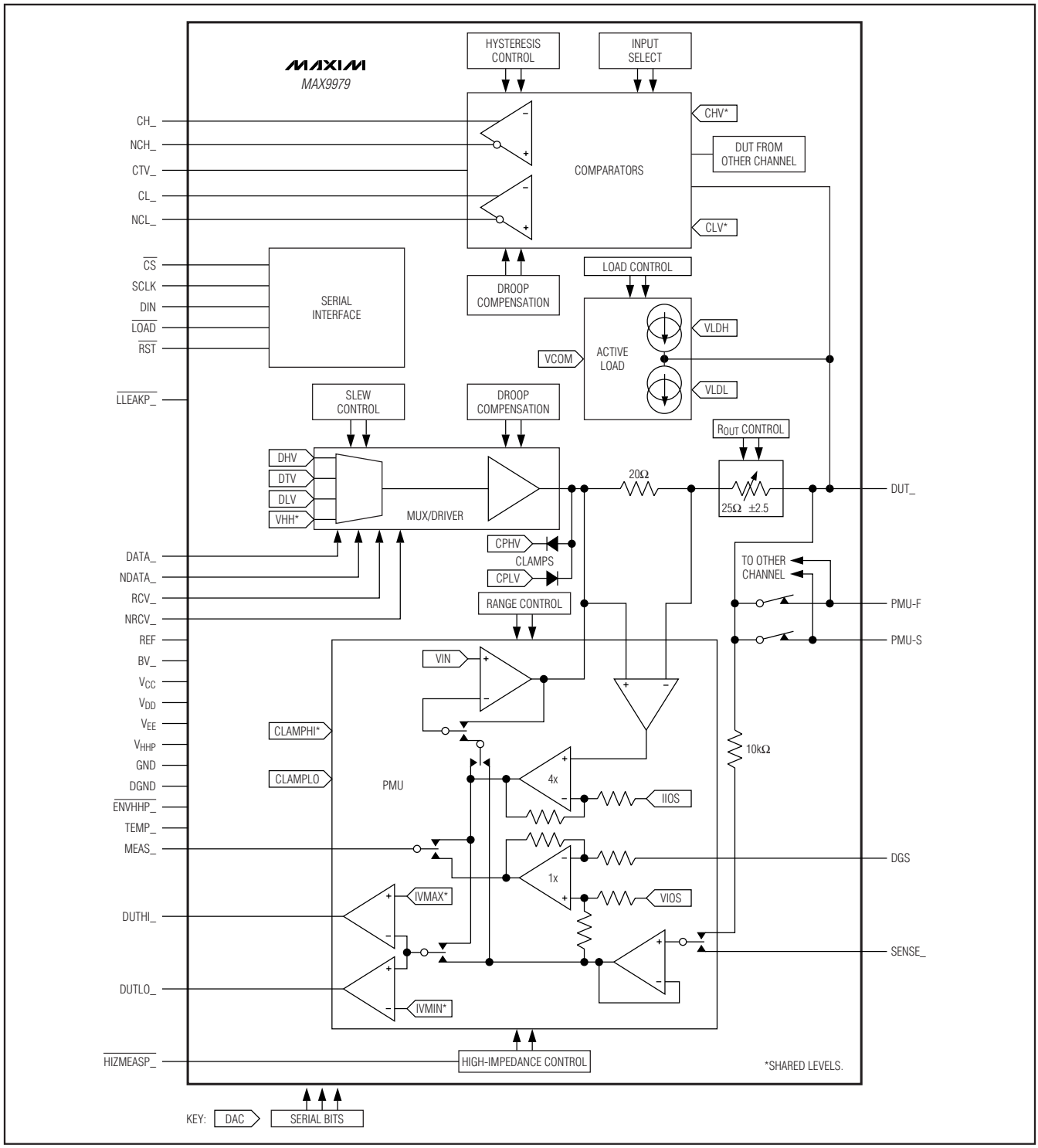



*Figure 1. Simplified Block Diagram. Only one of two channels is shown. The PMU is shown in high range. The single serial interface controls both channels.*

The integration of DCL and PMU functions in the MAX9979 requires defined states to manage the interaction of these resources. The PMU controls supersede those of the DCL, as described below and shown in Table 1. Important details to keep in mind are:

- Normal high-speed DCL operation is intended only when the PMU is in the FNMN state and the DCL is available, as indicated by Note B in Table 1.
- Forcing $\overline{\text{LLEAKP\_}}$ = 0 immediately places the DCL into low-leak mode, and the PMU into its high-impedance state independent of any other programmed control bit or external control inputs. Forcing $\overline{\text{LLEAKP\_}}$ = 1 is required to allow any other mode of operation.
- Forcing $\overline{\text{HIZFORCE\_}}$ = 1 enables the PMU and simultaneously forces the DCL into low-leak mode.
- Additional PMU settings such as the force and measure modes, current range, the measure output, comparators, and the clamp features are controlled as described later in this document.
- The MAX9979 provides calibration modes under which both the DCL and the PMU are simultaneously active. Forcing $\overline{\text{HIZFORCE\_}}$ = 0 ordinarily disables the PMU, however, when LLEAKS_ is not asserted, the FMODE_ and MMODE_ bits select these calibration modes. While in a calibration mode, the DCL states are still selected by the controls normally associated with those functions. When in a calibration mode, the PMU range A is not available. The PMU range defaults to range B if the serial-interface bit RS2_ = 1.

### Driver

The driver uses a high-speed multiplexer to select one of three DAC voltages (DHV_, DLV_, and DTV_), or to select high-impedance mode. Multiplexer switching is controlled by high-speed differential inputs DATA_/NDATA_ and RCV_/NRCV_ and mode-control bit TMSEL_ (see Table 2). The multiplexer output is buffered to drive DUT_. A programmable slew-rate circuit controls the slew rate of the buffer input.

In high-impedance mode, the clamps and comparators remain connected to DUT_, the DUT_ bias current is less than ±2µA, and the node continues to track high-speed signals. In low-leakage mode, the bias current at DUT_ is further reduced to less than ±10nA, yet signal tracking slows.

The nominal driver output resistance is 50Ω and features an adjustment range of ±2.5Ω through the serial interface in 360mΩ increments. Contact the factory for different output resistance values.

**Table 1. MAX9979 Mode Selection**

| MODES | DRIVER | COMPARATOR | LOAD | PMU | FMODE_ | MMODE_ | $\overline{\text{LLEAKP\_}}$ | $\overline{\text{HIZFORCE\_}}$ | NOTE |
|---|---|---|---|---|---|---|---|---|---|
| PMU | Low leak | Low leak | Low leak | FVMI | 0 | 0 | 1 | 1 | — |
| | Low leak | Low leak | Low leak | FVMV | 0 | 1 | 1 | 1 | — |
| | Low leak | Low leak | Low leak | FIMI | 1 | 0 | 1 | 1 | — |
| | Low leak | Low leak | Low leak | FIMV | 1 | 1 | 1 | 1 | — |
| DCL | Low leak | Available | Available | FVMI | 0 | 0 | 1 | 0 | A |
| | Available | Available | Available | FIMV | 0 | 1 | 1 | 0 | A |
| | Available | Available | Available | FNMN | 1 | 0 | 1 | 0 | B |
| | Available | Available | Available | FNMV | 1 | 1 | 1 | 0 | A |
| FNMx | Low leak | Low leak | Low leak | FNMN | X | 0 | 0 | X | — |
| | Low leak | Low leak | Low leak | FNMV | X | 1 | 0 | X | — |

*A = Calibration modes.*

*B = Normal high-speed DCL operation mode.*

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

## Table 2. Driver Control

| SERIAL-INTERFACE BITS | | | DIGITAL INPUTS | | | | DRIVER OUTPUT |
|---|---|---|---|---|---|---|---|
| LLEAKS_ | ENVHHS_ | TMSEL_ | $\overline{\text{LLEAKP\_}}$ | $\overline{\text{ENVHHP\_}}$ | RCV_ | DATA_ | |
| 0 | X* | X | 1 | 1 | 0 | 0 | Drive to DLV |
| 0 | X* | X | 1 | 1 | 0 | 1 | Drive to DHV |
| 0 | 0 | 0 | 1 | 1 | 1 | X | High-impedance receive |
| 0 | 0 | 1 | 1 | 1 | 1 | X | Drive to DTV |
| 0 | 1 | X | 1 | X | 1 | X | Drive to VHH** |
| 0 | 0 | X | 1 | 0 | X | X | Drive to VHH** |
| X | X | X | 0 | X | X | X | Low leak |
| 1 | X | X | X | X | X | X | Low leak |

**Specified DHV, DLV transition times are not altered by the state of ENVHHS_.*

***PMU and active load must be disabled to drive to VHH_ ($\overline{\text{HIZFORCE\_}}$ = 0, FMODE_ = 1, MMODE_ = 0, LDDIS_ = 1).*

## Table 3. Driver Slew Control

| SC1_ | SC0_ | DRIVER SLEW RATE (%) |
|---|---|---|
| 0 | 0 | 100* |
| 0 | 1 | 75 |
| 1 | 0 | 50 |
| 1 | 1 | 25 |

**The power-on-reset and $\overline{\text{RST}}$ default value.*

### Driver Slew Control

A slew-rate circuit controls the slew rate of the buffer input. Select one of four possible slew rates according to Table 3. The speed of the internal multiplexer sets the 100% driver slew rate (see the *Driver Large-Signal Response* graph in the *Typical Operating Characteristics* section). SC1 and SC0 are set to 0 at power-up or when $\overline{\text{RST}}$ is forced low.

### VHH Function

VHH allows DUT_ to drive voltages up to 13V. The VHH_ DAC, which doubles as the PMU's CLAMPHI_ DAC, adjusts from 0 to +13V. Table 2 indicates the control settings required to set DUT_ to VHH_. Table 23 shows the transfer function for the VHH_ DAC.

### Driver Cable-Droop Compensation

The driver incorporates active cable-droop compensation. At high frequencies, transmission-line effects from the DUT_ output, across the tester signal delivery path to the device under test, can degrade the output waveform fidelity, resulting in a highly degraded or unusable signal. The compensation circuit counters this degradation by adding a double time-constant decaying waveform to the nominal output waveform (pre-emphasis). Figure 2 depicts a comparison between a typical driver and the MAX9979, and shows how droop compensation counters signal degradation. Control bits CDRP0, CDRP1, and CDRP2 vary the amplitude of the compensation signal. Table 4 shows the percent compensation as a function of control bit settings. The power-on-reset and $\overline{\text{RST}}$ values for CDRP0, CDRP1, and CDRP2 are 0. The specified default value is CDRP0 = 1 for *Electrical Characteristics* table data.

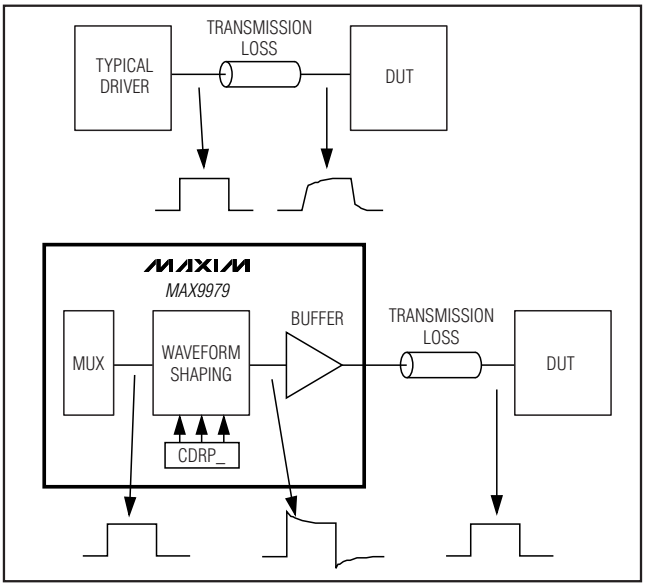



*Figure 2. Cable-Droop Compensation*

## Table 4. Cable-Droop Compensation Control

| SERIAL-INTERFACE BITS | | | DROOP COMPENSATION (%) |
|---|---|---|---|
| CDRP2_ | CDRP1_ | CDRP0_ | |
| 0 | 0 | 0 | 0* |
| 0 | 0 | 1 | 1.5** |
| 0 | 1 | 0 | 3 |
| 0 | 1 | 1 | 4.5 |
| 1 | 0 | 0 | 6 |
| 1 | 0 | 1 | 7.5 |
| 1 | 1 | 0 | 9 |
| 1 | 1 | 1 | 10.5 |

**The power-on-reset and $\overline{RST}$ default value.*

***Specified default value for Electrical Characteristics table data.*

***Adjustable Driver Output Impedance ($\Delta R_O$)***

The MAX9979's nominal 50Ω driver output resistance is adjustable by ±2.5Ω with a 360mΩ resolution. The RO bits in the DCL calibration register set the resistance value. Table 5 presents the output resistance control logic. The output resistance is set to $R_O$ + 0.0Ω (0b1000) at power-up or when $\overline{RST}$ is forced low.

## Table 5. Output Resistance Control

| SERIAL-INTERFACE BITS | | | | DRIVER OUTPUT RESISTANCE (Ω) |
|---|---|---|---|---|
| RO3_ | RO2_ | RO1_ | RO0_ | |
| 0 | 0 | 0 | 0 | $R_O$ - 2.88 |
| 0 | 0 | 0 | 1 | $R_O$ - 2.52 |
| 0 | 0 | 1 | 0 | $R_O$ -2.16 |
| 0 | 0 | 1 | 1 | $R_O$ - 1.80 |
| 0 | 1 | 0 | 0 | $R_O$ - 1.44 |
| 0 | 1 | 0 | 1 | $R_O$ - 1.08 |
| 0 | 1 | 1 | 0 | $R_O$ - 0.72 |
| 0 | 1 | 1 | 1 | $R_O$ - 0.36 |
| 1 | 0 | 0 | 0 | $R_O$ + 0* |
| 1 | 0 | 0 | 1 | $R_O$ + 0.36 |
| 1 | 0 | 1 | 0 | $R_O$ + 0.72 |
| 1 | 0 | 1 | 1 | $R_O$ + 1.08 |
| 1 | 1 | 0 | 0 | $R_O$ + 1.44 |
| 1 | 1 | 0 | 1 | $R_O$ + 1.80 |
| 1 | 1 | 1 | 0 | $R_O$ + 2.16 |
| 1 | 1 | 1 | 1 | $R_O$ + 2.52 |

**Power-on-reset and $\overline{RST}$ default value.*

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

### Driver DATA Invert Mode

The DATA_/NDATA_ signals for a driver channel are internally inverted when the INVERT_ bit in the DCL register is asserted. The INVERT_ bit is set to 0 at power-up or when $\overline{RST}$ is forced low.

### Driver Differential Data Mode

The MAX9979 allows the drivers to be configured for control of both channels from the channel 0 DATA0/NDATA0 inputs. This feature allows the two channels to drive DUT nodes in parallel, providing a 25Ω driver at twice the nominal drive current. Enable this feature by setting the DIFFERENTIAL0 bit in the DCL register. The DIFFERENTIAL0 bit is set to 0 at power-up or when $\overline{RST}$ is forced low.

### Driver Invert + Differential Data Mode

Combining the differential and the invert modes allows the two channels to produce complementary outputs at DUT0 and DUT1 from a single digital data stream at DATA0/NDATA0. The driver block diagram (Figure 3) shows the logic of the differential and inverted modes.

### Bias Voltage Input (BV_)

Apply a voltage to BV_ that is ≥ the $V_{IH}$ voltage used for the DATA_ and RCV_ inputs ($V_{IH}$ (DATA_, RCV_)) < $V_{BV}$ < 3.5V, because there are ESD-protection diodes between BV_ and the high-speed inputs. Failure to do this turns on the protection diodes, degrading the DATA_ and RCV_ signals. Input bias current for BV_ is less than 1µA.

### Driver Voltage Clamps

The voltage clamps (high and low) limit the voltage at DUT_ and suppress reflections when the channel is configured as a high-impedance receiver. The clamps behave as diodes connected to the outputs of high-current buffers (Figure 1). Internal circuitry compensates for the diode drop at 1mA clamp current. Set the clamp voltages using the level-setting DACs (CPHV_ and CPLV_). The clamps are enabled only when the driver is in the high-impedance mode. For transient suppression, set the clamp voltages to approximately the minimum and maximum expected DUT_ voltage range. The optimal clamp voltages are application-specific and must be empirically determined. Set the clamp voltages at least 0.7V outside the expected DUT_ voltage range when not using the clamps. Overvoltage protection then remains active without loading DUT_. Driver clamps are always and only enabled in driver high-impedance mode.

### High-Speed Comparators

The MAX9979 provides two independent high-speed comparators for each channel. Each comparator has one input connected internally to DUT_ and the other input connected to either CHV_ or CLV_ (Figure 4). Cable-droop compensation is present on both channels. Comparator outputs are a logical result of the input conditions.

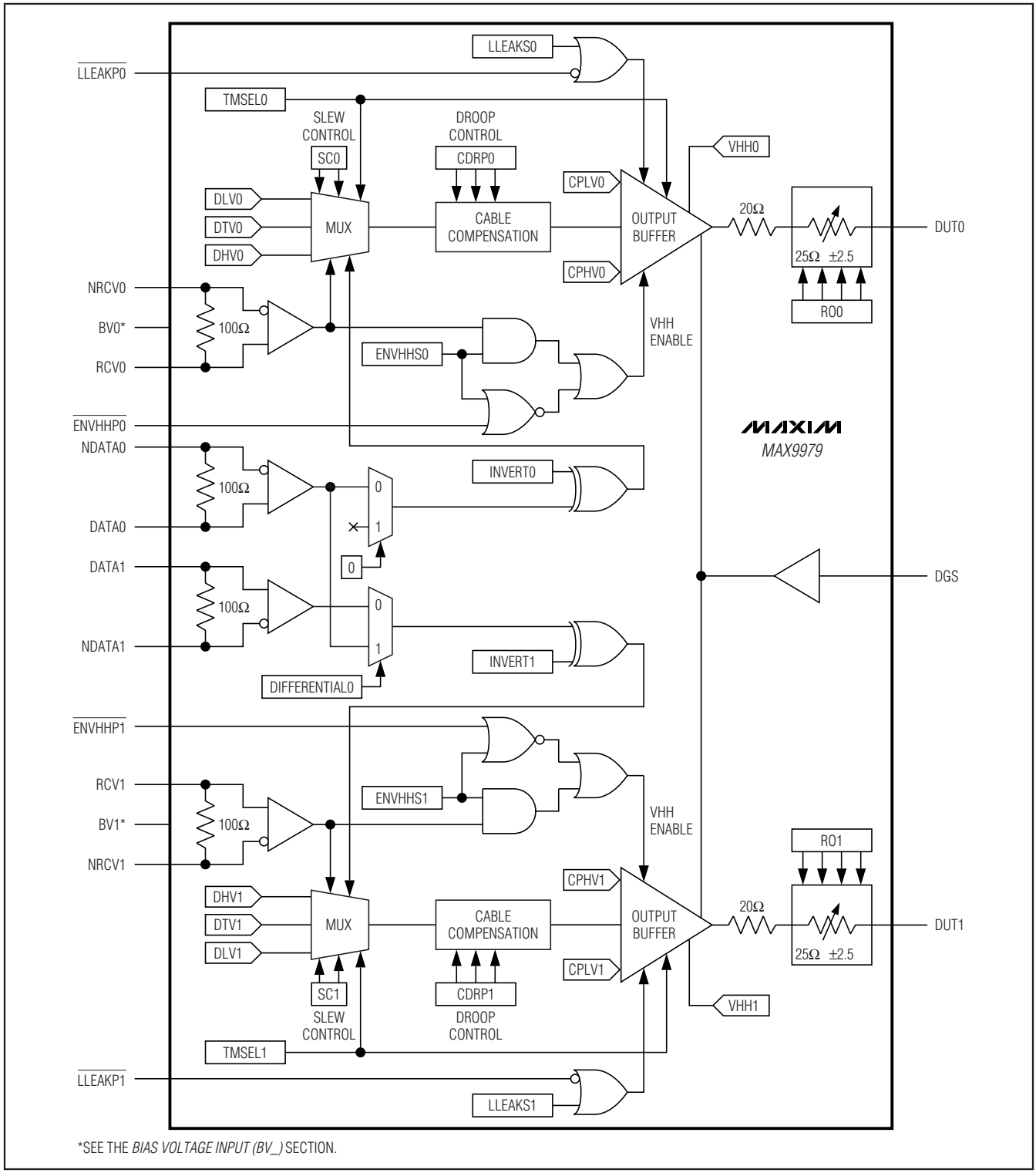
This configuration switches a 16mA current source between the two outputs, and each output has an internal termination resistor connected to CTV_. These resistors are typically 50Ω. Use alternate configurations to terminate different path impedance provided that the absolute maximum ratings are not exceeded. Note that the resistor value also sets the voltage swing. The output provides a nominal 400m$V_{P-P}$ swing with a 50Ω load termination, and a 50Ω source termination. See the *Electrical Characteristics* section titled *High-Speed Comparators, Logic Outputs* for definition of the $V_{OH}$ voltage.

### Single-Ended Window Comparator

Set the DIFFERENTIAL1 bit = 0 in the channel 1 DCL register to enable the high-speed window comparator. DAC voltages CHV_ and CLV_ control the comparator thresholds. Table 6 shows the truth table for the comparators. Figure 4 shows the comparator block diagram.

## Table 6. Single-Ended Window Comparator Truth Table

| CONDITION | | CH_ | CL_ |
|---|---|---|---|
| $V_{DUT\_} < V_{CHV\_}$ | $V_{DUT\_} < V_{CLV\_}$ | 0 | 0 |
| $V_{DUT\_} < V_{CHV\_}$ | $V_{DUT\_} > V_{CLV\_}$ | 0 | 1 |
| $V_{DUT\_} > V_{CHV\_}$ | $V_{DUT\_} < V_{CLV\_}$ | 1 | 0 |
| $V_{DUT\_} > V_{CHV\_}$ | $V_{DUT\_} > V_{CLV\_}$ | 1 | 1 |




*SEE THE *BIAS VOLTAGE INPUT (BV_)* SECTION.

*Figure 3. Driver Block Diagram*

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

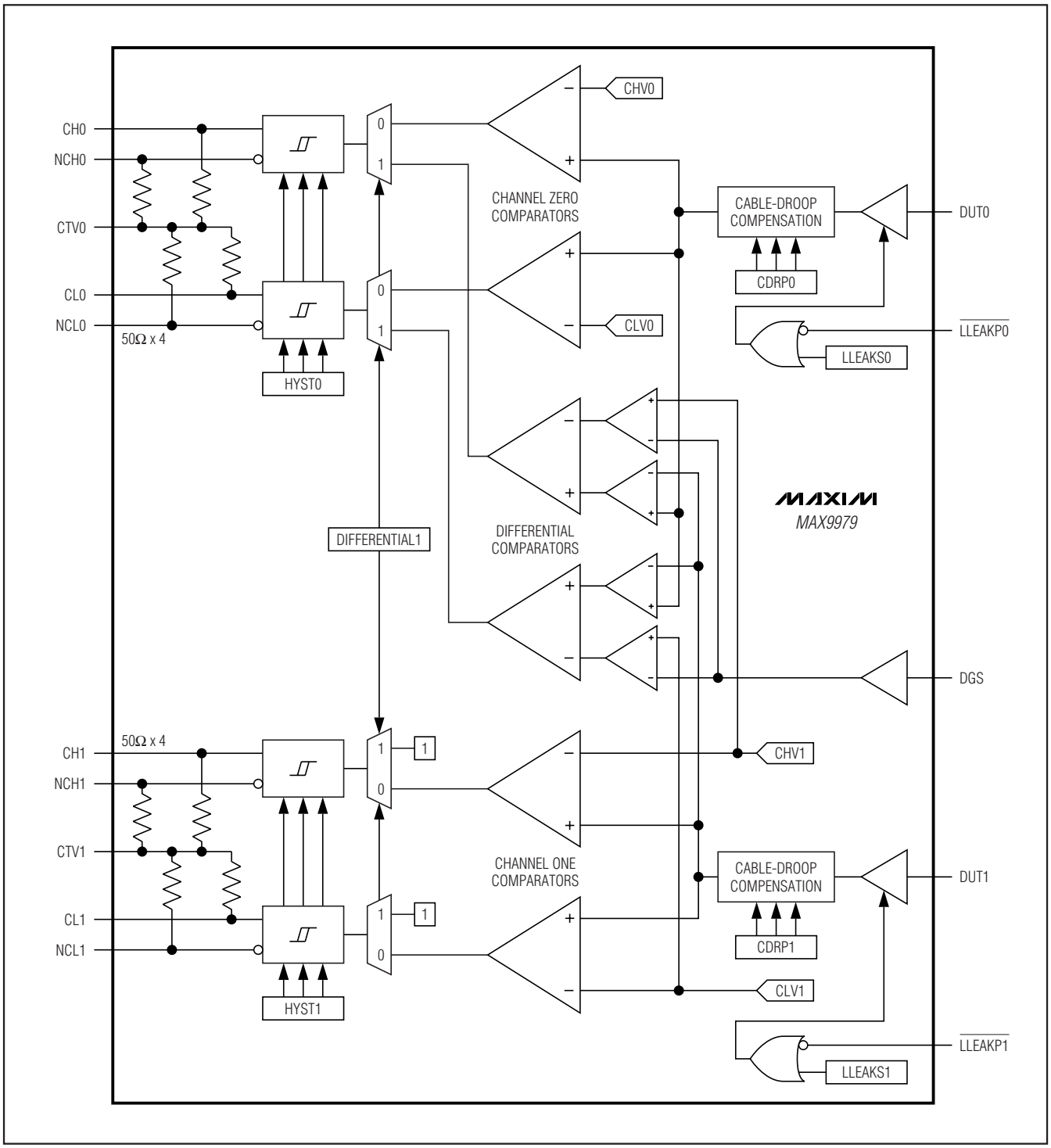



*Figure 4. High-Speed Comparators Block Diagram*

## Table 7. Differential Window Comparator Truth Table

| CONDITION | | CH0 | CL0 |
|---|---|---|---|
| $V_{DUT0} - V_{DUT1} < V_{CHV1} - V_{DGS}$ | $V_{DUT0} - V_{DUT1} < V_{CLV1} - V_{DGS}$ | 0 | 0 |
| $V_{DUT0} - V_{DUT1} < V_{CHV1} - V_{DGS}$ | $V_{DUT0} - V_{DUT1} > V_{CLV1} - V_{DGS}$ | 0 | 1 |
| $V_{DUT0} - V_{DUT1} > V_{CHV1} - V_{DGS}$ | $V_{DUT0} - V_{DUT1} < V_{CLV1} - V_{DGS}$ | 1 | 0 |
| $V_{DUT0} - V_{DUT1} > V_{CHV1} - V_{DGS}$ | $V_{DUT0} - V_{DUT1} > V_{CLV1} - V_{DGS}$ | 1 | 1 |

### *Differential Window Comparator*

Set the DIFFERENTIAL1 bit = 1 in the channel 1 DCL register to enable the high-speed differential window comparator. CHV1 and CLV1 control the differential comparator thresholds. CHV0 and CLV0 are not used when differential comparison is active. The valid voltage range for CHV1 and CLV1 in differential comparison mode is ±1V. Setting levels outside ±1V does not damage the device, but performance is not guaranteed. Differential comparator outputs are multiplexed to the channel 0 comparator outputs. The channel 1 comparator outputs are both forced to a high state. Figure 4 shows the operation of the comparators. Table 7 shows the truth table for the differential comparator. Figure 4 shows the comparator block diagram.

### *Comparator Hysteresis*

The DCL calibration register controls the high-speed comparator hysteresis. The HYST bits of that register select one of eight values (0, 2mV, 4mV, 6mV, 8mV, 10mV, 12mV, or 15mV). Hysteresis control affects both single-ended and differential comparators. The HYST bits are set to 0b000 at power-up or when $\overline{RST}$ is forced low. Table 8 shows the HYST bit functions.

## Table 8. Hysteresis Logic

| SERIAL-INTERFACE BITS | | | COMPARATOR HYSTERESIS (mV) |
|---|---|---|---|
| HYST1_ | HYST1_ | HYST0_ | |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 4 |
| 0 | 1 | 1 | 6 |
| 1 | 0 | 0 | 8 |
| 1 | 0 | 1 | 10 |
| 1 | 1 | 0 | 12 |
| 1 | 1 | 1 | 15 |

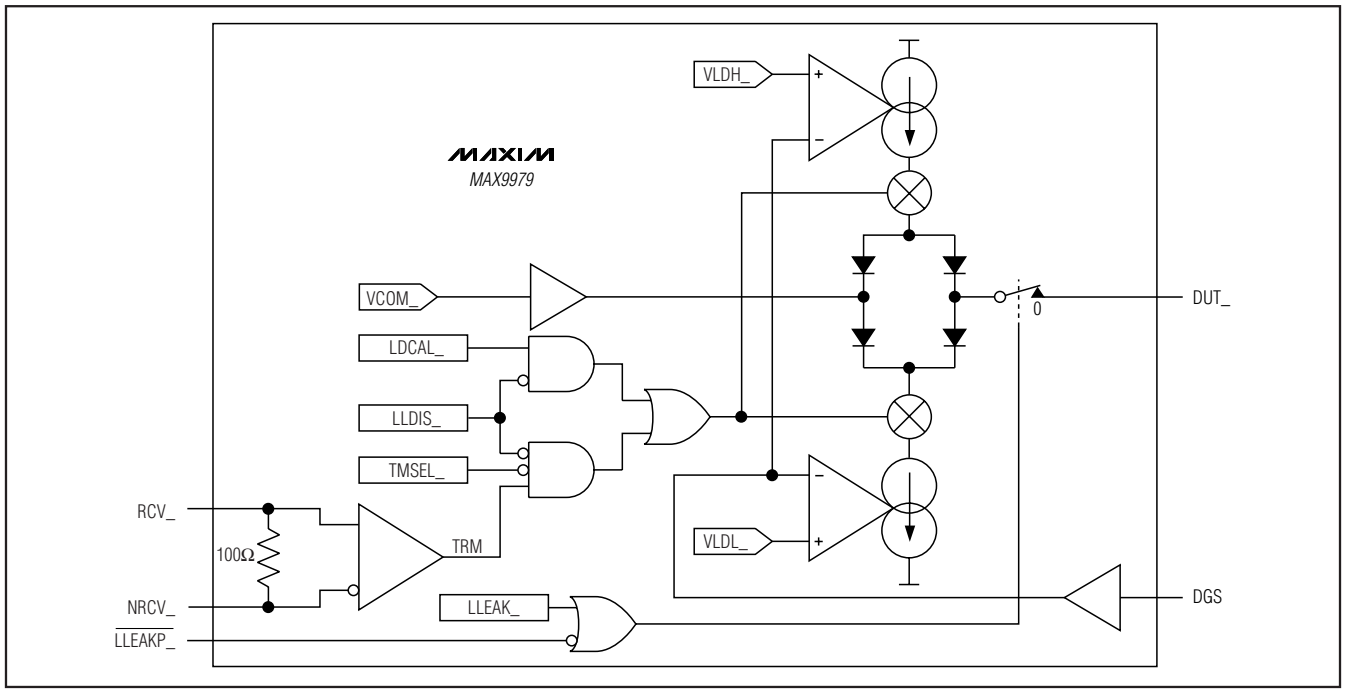



*Figure 5. Active Load Block Diagram (One Channel Shown)*

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

### Comparator Cable-Droop Compensation

Control comparator cable-droop compensation using the same serial bits used for the driver droop compensation, CDRP_. Cable-droop compensation is active for both the single-ended and the differential comparators.

### Active Load

The active load is a linearly programmable current source and sink, a commutation buffer, and a diode bridge (Figure 5). Level-setting DACs VLDH_ and VLDL_ set the sink and source currents from 0 to 20mA. Level-setting DAC VCOM_ sets the commutation buffer output voltage. The source and sink naming convention is referenced to the MAX9979, so current out of the MAX9979 constitutes source current and current into the MAX9979 constitutes sink current.

The programmed source current loads the device under test when $V_{DUT\_} < V_{COM\_}$. The programmed sink current loads the device under test when $V_{DUT\_} > V_{COM\_}$. The high-speed differential inputs (RCV_/NRCV_) and three bits of the control word (LLDIS_, LDCAL_, and TMSEL_) control the load. LLEAKP_ and LLEAK_ place the load into low-leakage mode. The low-leakage controls override other controls. Table 9 details load control logic.

### Load Calibration Enable (LDCAL_)

LDCAL_ allows the load and driver to be simultaneously enabled for diagnostic purposes. LDDIS_ overrides LDCAL_.

### Parametric Measurement Unit (PMU)

The MAX9979 PMU forces and measures voltages from -1.5V to 6.5V, and currents up to ±50mA. The lowest full-scale current range is ±2µA. Available PMU modes are force-voltage/measure voltage (FVMV), force-voltage/measure current (FVMI), force-current/measure current (FIMI), force-current/measure voltage (FIMV), force-nothing/measure voltage (FNMV), and force-nothing/measure nothing (FNMN). Figure 6 presents a block diagram on the PMU.

### PMU Current-Range Selection

Three bits from the control word (RS0, RS1, and RS2) control the full-scale current range for both force-current (FI) and measure-current (MI) modes. The PMU ranges are independent of the programmed PMU mode, except range A, which is not allowed in any calibration mode. In these modes range A defaults to range B (see Table 1). Table 10 presents the PMU current-range control logic.

## Table 9. Load Control Logic

| RCV_ | TMSEL_ | LDDIS_ | LDCAL_ | LLEAKS_ | $\overline{\text{LLEAKP\_}}$ | LOAD STATE |
|---|---|---|---|---|---|---|
| X | X | X | X | 1 | X | Low leak |
| X | X | X | X | X | 0 | Low leak |
| 0 | X | 0 | 0 | 0 | 1 | Off |
| X | X | 1 | X | 0 | 1 | Off |
| 1 | 1 | 0 | 0 | 0 | 1 | Off |
| 1 | 0 | 0 | 0 | 0 | 1 | On |
| X | X | 0 | 1 | 0 | 1 | On |

## Table 10. PMU Current-Range Control

| DIGITAL INPUT | SERIAL-INTERFACE BITS | | | | RANGE |
|---|---|---|---|---|---|
| $\overline{\text{LLEAKP\_}}$ | $\overline{\text{HIZFORCE\_}}$ | RS2_ | RS1_ | RS0_ | |
| X | X | 0 | 0 | 0 | E |
| X | X | 0 | 0 | 1 | D |
| X | X | 0 | 1 | 0 | C |
| X | X | 0 | 1 | 1 | B |
| X | 0 | 1 | X | X | B* |
| 0 | 1 | 1 | X | X | B* |
| 1 | 1 | 1 | X | X | A |

**Range A operation is not allowed for PMU high-impedance modes—PMU defaults to range B.*

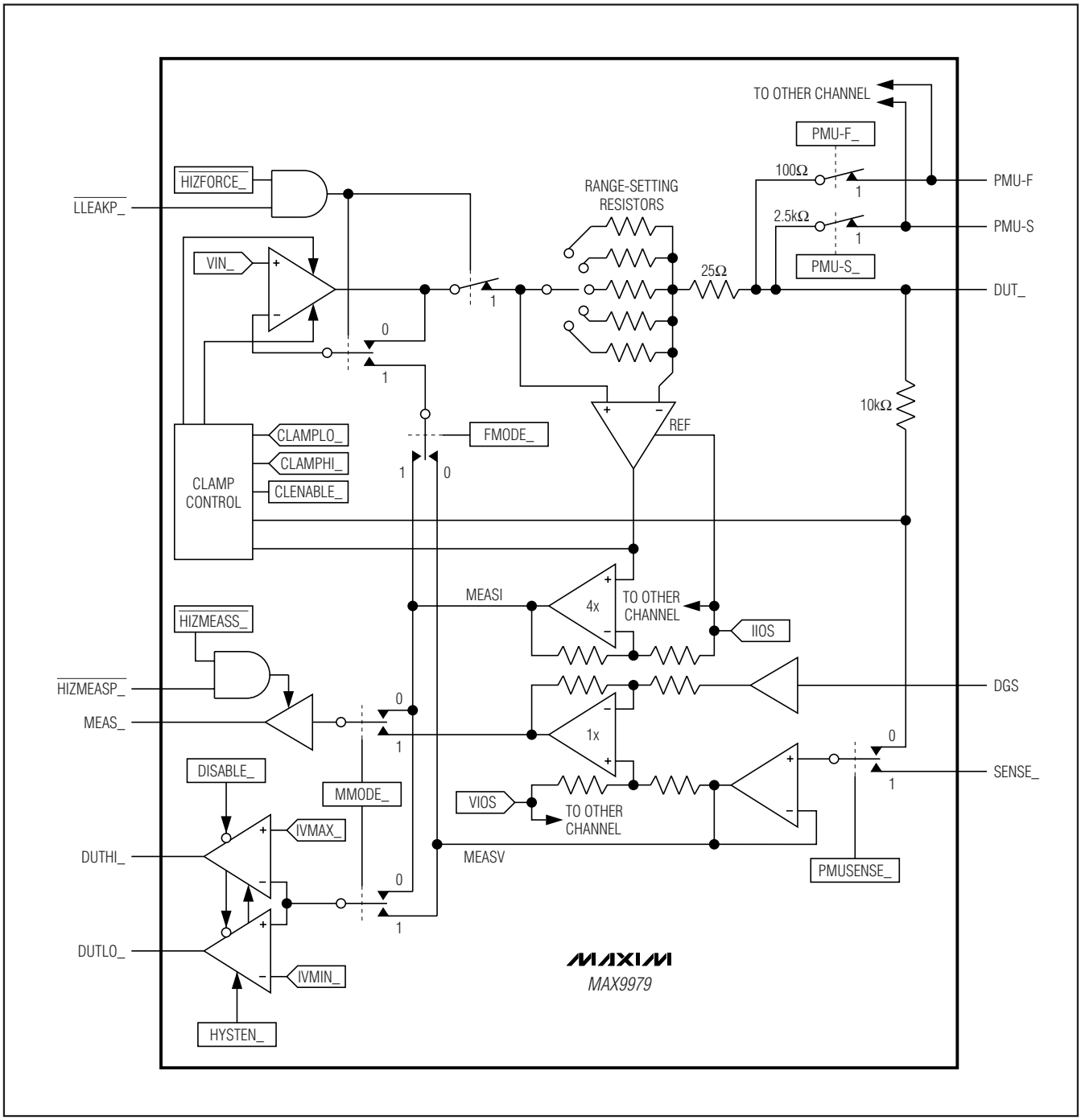



*Figure 6. PMU Block Diagram (One Channel Shown)*

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

### PMU Comparators

Two comparators, configured as a window comparator, monitor the MEASV_ and MEASI_ signals (Figure 6). Level-setting DACs IVMAX_ and IVMIN_ set the high and low thresholds that determine the window (DAC IVMAX_ shares duties with VHH_). Both PMU window comparator outputs are open-drain and share a single serial disable bit ($\overline{\text{DISABLE\_}}$) that puts the outputs in a high-impedance, low-leakage state. MEAS_ includes the influence of VIOS, while the comparator outputs do not. Table 11 presents the PMU comparator output logic.

### PMU Measure Output (MEAS_)

The MEAS_ output presents a voltage proportional to the measured voltage or current. Force logic input $\overline{\text{HIZMEASP\_}}$ or bit $\overline{\text{HIZMEASS\_}}$ low to place MEAS_ in a low-leakage, high-impedance state.

### VIOS Offset Level for PMU Measure Voltage MEAS_ Output

In MV mode, use the VIOS level-setting DAC to offset the MEAS_ output voltage. The valid range of VIOS is 0 to 1.5V, but the VIOS DAC is programmable from -1.25V to +3.75V. The single VIOS DAC is shared by both channels. VIOS allows level shifting the MEAS_ output, useful when MEAS_ is read by a unipolar ADC. The nominal 0x0000 to 0xFFFF code range for VIOS equates to -1.25V to +3.75V. The power-on-reset and $\overline{\text{RST}}$ state of VIOS is 0x4000, or 0V, the level for normal operation. The MEAS_ output tracks DGS. The VIOS DAC range is programmable outside the valid operational range of the VIOS signal, but doing so will not harm the device. Table 23 presents the VIOS DAC transfer function.

### IIOS Reference Level for PMU Measure Current MEAS_ Output

In MI mode, adjust the MEAS_ output around the $I_{DUT\_}$ = 0 center reference using the IIOS level-setting DAC. IIOS is programmable from 0 to 5V, but levels outside of the 2V to 4V range are invalid. The single IIOS DAC is shared by both channels. IIOS allows level shifting the ±4V MI output range to fully above ground at the MEAS_ output, useful when MEAS_ is read by a unipolar ADC. The nominal 0x0000 to 0xFFFF code range for IIOS equates to 0 to 5V. The power-on-reset and $\overline{\text{RST}}$ state of IIOS is 0x4000, or 1.25V. For normal operation, the level of IIOS is 2.5V for a -1.5V to +6.5V MI MEAS_ output. The IIOS DAC range is programmable outside the valid operational range of the IIOS signal, but doing so will not harm the device. Table 23 presents the IIOS DAC transfer function.

The MI MEAS_ output is a buffered version of an internal node that is used to close the force-current loop. The sourcing range of forced current is limited for IIOS levels above 3.5V by the $V_{IN}$ upper limit of approximately 7.5V.

### PMU Sense

Control bit PMUSENSE_ determines which of two inputs reaches the PMU sense amplifier (Figure 6). One input is from DUT_ through an internal 10kΩ resistor, the other input is from external input SENSE_. Not shown in Figure 6 is a third input to the sense amplifier (GND), which is used in VHH and FNMN modes to isolate and protect the amplifier from potential overvoltage and glitches. GND is connected automatically based on mode setting and no discrete control is required. Table 12 presents the PMU sense control logic.

## Table 11. PMU Comparator Output Logic

| $\overline{\text{DISABLE\_}}$ BIT | CONDITION | COMPARATOR OUTPUTS | |
|---|---|---|---|
| | | DUTHI_ | DUTLO_ |
| 0 | X | High impedance | High impedance |
| 1 | $V_{MEASURE} > V_{IVMAX}$ and $V_{IVMIN}$ | 0 | 1 |
| 1 | $V_{IVMAX} > V_{MEASURE} > V_{IVMIN}$ | 1 | 1 |
| 1 | $V_{IVMAX}$ and $V_{IVMIN} > V_{MEASURE}$ | 1 | 0 |
| 1 | $V_{IVMIN} > V_{MEASURE} > V_{IVMAX}$* | 0 | 0 |

**Normal operation is with $V_{IVMAX} > V_{IVMIN}$. This condition has $V_{IVMIN} > V_{IVMAX}$. This does not cause any problems with the operation of the comparators.*

## Table 12. PMU Sense Control Logic

| DIGITAL INPUT | SERIAL-INTERFACE BITS | | | | PMU MODE | SENSE PATH |
|---|---|---|---|---|---|---|
| $\overline{\text{LLEAKP\_}}$ | $\overline{\text{HIZFORCE\_}}$ | FMODE_ | MMODE_ | PMUSENSE_ | | |
| 1 | 1 | X | X | 0 | FyMy* | Internal |
| 1 | 1 | X | X | 1 | FyMy* | External |
| 1 | 0 | 0 | X | 0 | FVMy* (calibration) | Internal |
| 1 | 0 | 0 | X | 1 | FVMy* (calibration) | External |
| 1 | 0 | 1 | 0 | X | FNMN | GND |
| 1 | 0 | 1 | 1 | 0 | FNMV (calibration) | Internal |
| 1 | 0 | 1 | 1 | 1 | FNMV (calibration) | External |
| 0 | X | X | 0 | X | FNMN | GND |
| 0 | X | X | 1 | 0 | FNMV (calibration) | Internal |
| 0 | X | X | 1 | 1 | FNMV (calibration) | External |

**y = V or I.*

### *PMU Analog Signal Polarities*

In FV mode, DUT_ voltage is proportional to level-setting DAC voltage $V_{IN\_}$. In FI mode, the current flowing out of DUT_ is equal to:

$$\frac{(V_{IN} - V_{IIOS})}{4 \times R_{RANGE}}$$

Positive current is defined as flowing out of the PMU. In FN mode, the PMU output is high impedance. Table 13 presents the range resistor values. Table 23 presents the DAC transfer functions.

### *PMU Voltage Clamps*

Voltage clamps are available on the PMU output only in the FI mode. Program the clamps with level-setting DACs CLAMPLO_ and CLAMPHI_. The PMU voltage clamps handle the full ±50mA and are triggered by the voltage at DUT_ independent of the voltage at SENSE_. The voltage clamps override the PMU only, and do not limit the voltage of external sources. If an external source drives DUT_ beyond a voltage clamp level, the PMU will current limit safely. When a PMU voltage clamp is active and at its limit, the MV and MI functions remain valid. Do not let external voltage levels at DUT_ exceed the absolute maximum rating limits.

### *PMU Current Clamps*

Current clamps are available on the PMU output only in the FV mode. Program the clamps with level-setting DACs CLAMPLO_ and CLAMPHI_. The PMU current clamps handle the full current range (±50mA for range A, ±2mA for range B, etc.). If the clamp currents are exceeded, the PMU enters a constant-voltage mode. The current clamp circuits override the PMU only, and do not limit external sources. When a PMU current clamp is active, the MV and MI functions are still valid.

### *PMU Clamp Enable*

The CLENABLE_ bit in the PMU register enable the voltage and current clamps. Table 14 presents the clamp enable control logic.

## Table 13. Range Resistor Values

| RANGE | RESISTOR VALUE (Ω) |
|---|---|
| A | 20 |
| B | 500 |
| C | 5k |
| D | 50k |
| E | 500k |

## Table 14. Clamp Enable Control Logic

| CLENABLE_ BIT | MODE |
|---|---|
| 1 | Clamps enabled |
| 0 | Clamps disabled |

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

### PMU Voltage/Current-Limit Flags

The PMU features two comparators, arranged as a window comparator, to flag current or voltage levels, allowing fast go/no-go testing. The comparators monitor the load current or voltage, and compare it to level-setting DACs IVMAX and IVMIN. The MMODE_ bit selects whether the window comparator monitors MEASV_ or MEASI_ (Figure 6). If MMODE_ selects MEASV_ then the PMUSENSE_ bit selects either the SENSE_ input or DUT_ (Figure 6).

### Independent Control of PMU Feedback Switch and Measure Switch

Two single-pole/double-throw (SPDT) switches determine the mode of operation of the PMU. One switch determines whether the sensed DUT_ current or DUT_ voltage is fed back to the input, and thus determines which of these parameters is forced. The other switch determines whether the sensed DUT_ current or DUT_ voltage is presented at MEAS_. Independent control of these switches and the force high-impedance state allow for flexible modes of operation beyond the traditional force-voltage/measure-current (FVMI) and force-current/measure-voltage (FIMV) modes. The modes supported are:

- FVMI: Force-voltage/measure-current mode
- FIMV: Force-current/measure-voltage mode
- FVMV: Force-voltage/measure-voltage mode
- FIMI: Force-current/measure-current mode
- FNMV: Force-nothing/measure-voltage mode
- FNMN: Force-nothing/measure-nothing mode

### PMU Measure Output High-Impedance Control

The MEAS_ output features a low-leakage, high-impedance state. To activate this state, either place the $\overline{\text{HIZMEASS\_}}$ bit low or force the $\overline{\text{HIZMEASP\_}}$ logic input low. The two controls are logically ANDed together (Figure 6). The $\overline{\text{HIZMEASP\_}}$ input allows multiplexing between PMU measure outputs without the use of the serial interface. At power-up, $\overline{\text{HIZMEASS\_}}$ defaults low, placing MEAS_ in a high-impedance state. Table 15 presents the high-impedance control logic for the MEAS_ output.

### PMU Low-Leakage Mode

The PMU output features a low-leakage, high-impedance state. To activate this state, either place the $\overline{\text{HIZFORCE\_}}$ bit low or force the LLEAKP_ logic input low. The two controls are logically ANDed together (Figure 6). At power-up, $\overline{\text{HIZFORCE\_}}$ defaults low, placing the PMU in a low-leakage state. Table 1 presents the low-leakage logic for the PMU output.

**Table 15. Measure Output High-Impedance Control Logic**

| $\overline{\text{HIZMEASS\_}}$ BIT | $\overline{\text{HIZMEASP\_}}$ INPUT | MEAS_ STATE |
|---|---|---|
| 1 | 1 | Measure output enabled |
| 1 | 0 | High impedance |
| 0 | 1 | High impedance |
| 0 | 0 | High impedance |

### PMU DUT Ground Sense (DGS)

All the DAC and MEAS_ outputs track with respect to the DUT ground sense input (DGS). Connect DGS to the ground of the device under test.

### PMU DUT_ Node Force and Sense Switches

The MAX9979 features additional PMU force (PMU-F) and PMU sense (PMU-S) connections, through serial-controlled switches, that are shared between channels (Figure 6) and can be used to connect an external PMU. The force switch is maximum 100Ω, and the sense switch is maximum 2.5kΩ.

### PMU DUT_ Voltage Swing vs. DUT_ Current and Power-Supply Voltages

Two issues limit the DUT_ voltage that the PMU delivers. The first issue is the headroom required by the amplifiers and other on-chip circuitry at zero output current. The second issue is the headroom required with sense resistor and additional circuit voltage drops at full-scale current. When the PMU is sourcing or sinking DUT_ current, the voltage range is reduced linearly. This compliance curve applies to both FV and FI modes and is independent of $V_{DGS}$. Because the forced DUT_ voltage in FV mode is = DGS + $V_{IN}$, $V_{DUT\_}$ is further limited by the $V_{DGS}$ and the -2.5V to +7.5V $V_{IN}$ range. Force output capabilities of the PMU are presented in Figure 7.

These limitations are based on the guaranteed performance of the MAX9979. Operating the DUT node outside these limits will not harm the MAX9979, as long as the absolute maximum rating limits are observed. With the above considerations, it is possible to extend the range of the DUT swing beyond the limits of Figure 7. However, some specifications, such as linearity, will begin to degrade. Performance while operating outside the limits shown in Figure 7 is not guaranteed.

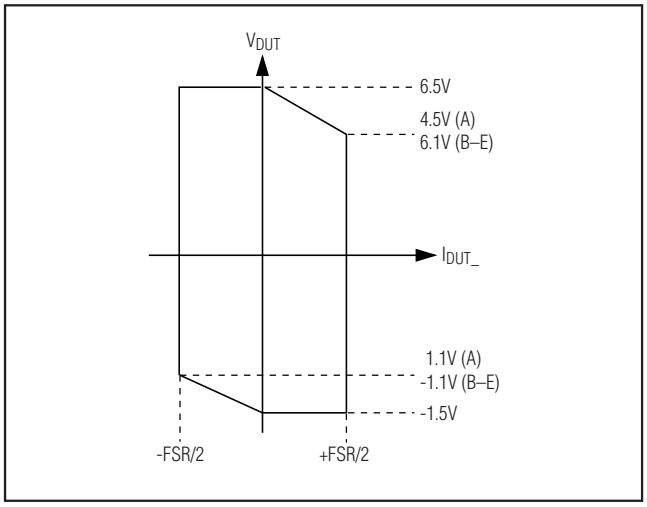



*Figure 7. Output-Voltage Range*

### Serial Interface

An SPI-compatible serial interface and the logic-controlled inputs shown in Table 1 control the MAX9979. The serial interface, detailed in Figure 8, operates with clock speeds up to 50MHz and includes the signals $\overline{CS}$, SCLK, DIN, $\overline{RST}$, $\overline{LOAD}$, and DOUT. Serial-interface timing is shown in Figure 9 and timing specifications are detailed in the *Electrical Characteristics* section.

#### Loading Data into the MAX9979

Load data into the 24-bit shift register from DIN on the rising edge of SCLK, while $\overline{CS}$ is low (Figure 8). The MAX9979 is updated when the control and level-setting data are latched into the control and level-setting registers. The control and level-setting registers are separated from the shift register by the input and channel-select registers. Two methods allow data to transfer from the shift register to the control and level-setting registers, depending on the state of external digital input $\overline{LOAD}$.

Holding $\overline{LOAD}$ high during the rising edge of $\overline{CS}$ allows the shift register data to transfer only into the input and channel-select registers. Force $\overline{LOAD}$ low to transfer the data into the control and level-setting registers. Changes update on the falling edge of $\overline{LOAD}$, which allows preloading of data and facilitates synchronizing updates across multiple devices.

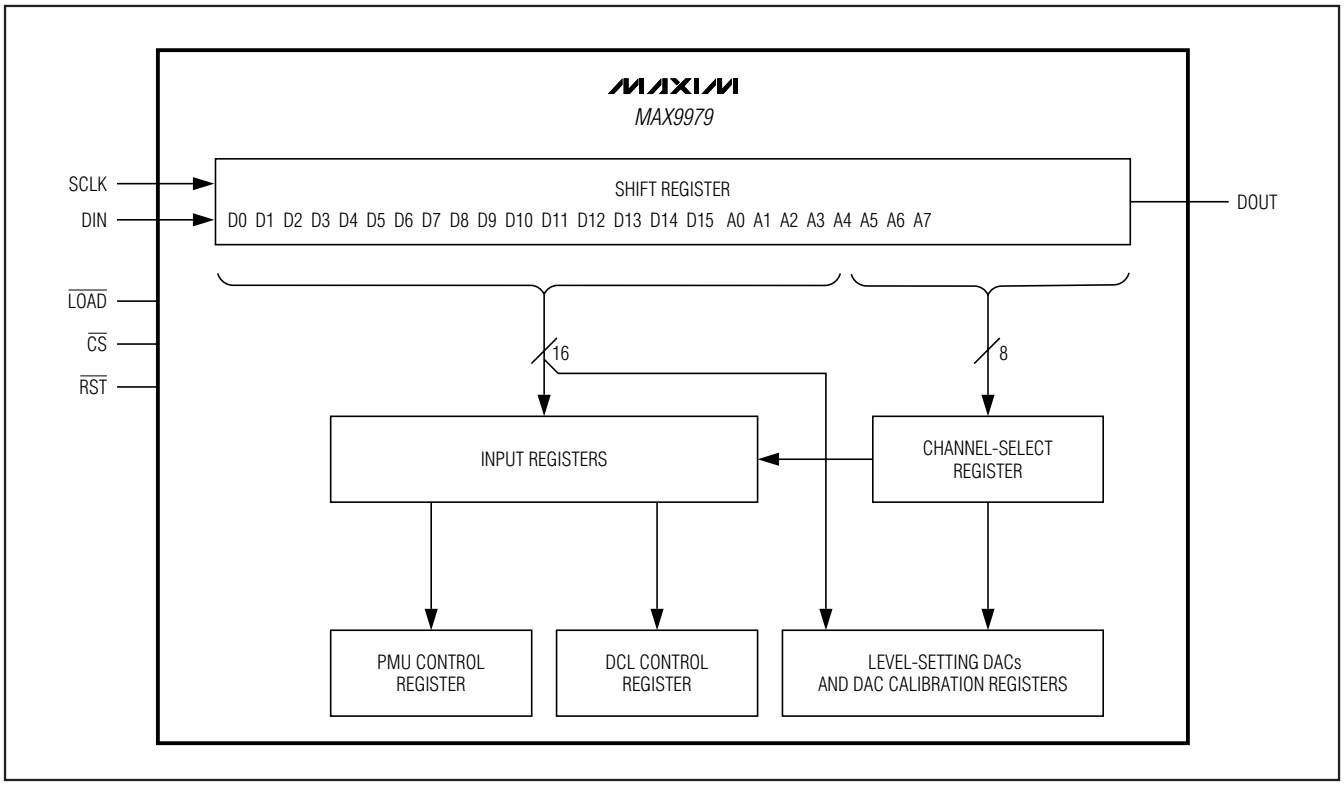



*Figure 8. Serial-Interface Block Diagram*

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

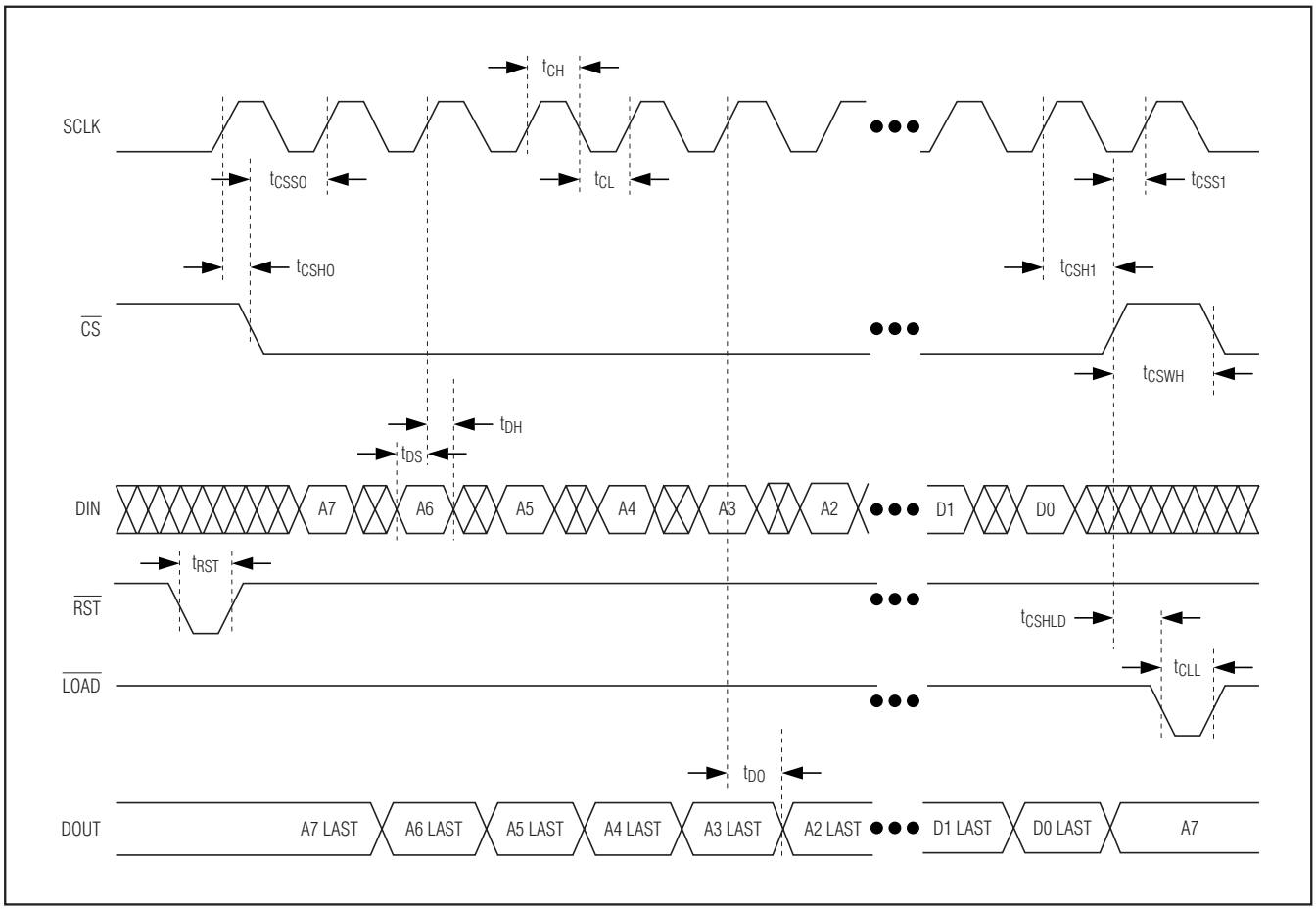



*Figure 9. Serial-Interface Timing*

Holding $\overline{LOAD}$ low during the rising edge of $\overline{CS}$ forces the input and channel-select registers to become transparent and all data transfers through these registers directly to the control and level-setting registers. Changes update on the rising edge of $\overline{CS}$. Figures 10 and 11 show how $\overline{LOAD}$ and $\overline{CS}$ function, and also the data configuration of SCLK, DIN, and DOUT.

The calibration registers change on the rising edge of $\overline{CS}$, regardless of the state of $\overline{LOAD}$.

### DOUT

DOUT is a buffered version of the last bit in the serial-interface shift register. The complete contents of the shift register can be read at DOUT during the next write cycle. To shift data out without modifying any registers, perform a write with address bits A4 and A5 set to 0. Use DOUT to daisy chain multiple devices, and/or to verify that data were properly shifted in during the previous communication.

### Controlling the MAX9979

Control and level-setting registers are selected to receive data based on the channel and mode-select bits (A0–A7). Table 16 presents the control register bits and their functions. Level-setting DAC data and control-register data are contained in the 16 data bits D0–D16. Tables 15, 16, and 17 detail the bit functions. Clock in bit A7 first, and bit D0 last, as shown in Figure 8.

Bit A6 allows access to the DAC calibration registers. Use the calibration registers to adjust the gain and offset of each DAC. Set bit A6 to write to the calibration registers (Table 18). See the *Level-Setting DACs* section for more information.

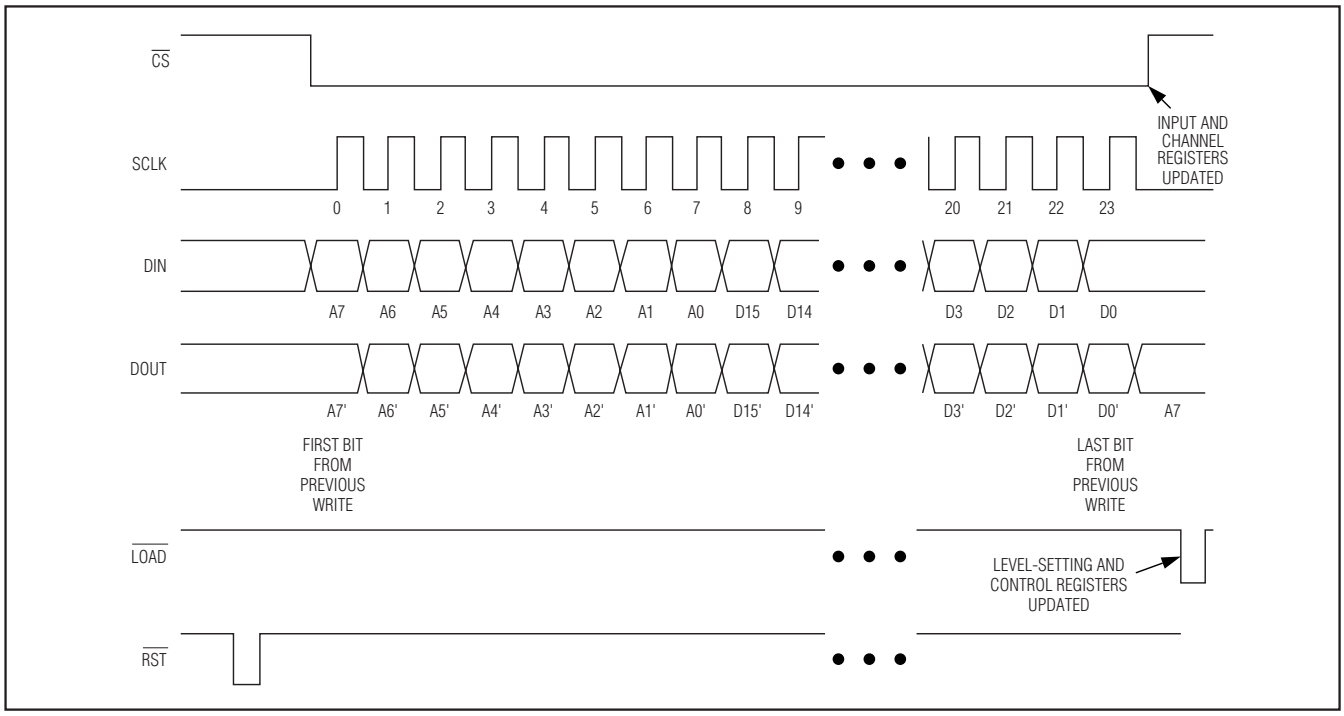



*Figure 10. Using $\overline{LOAD}$ to Update the Level-Setting and Control Registers*

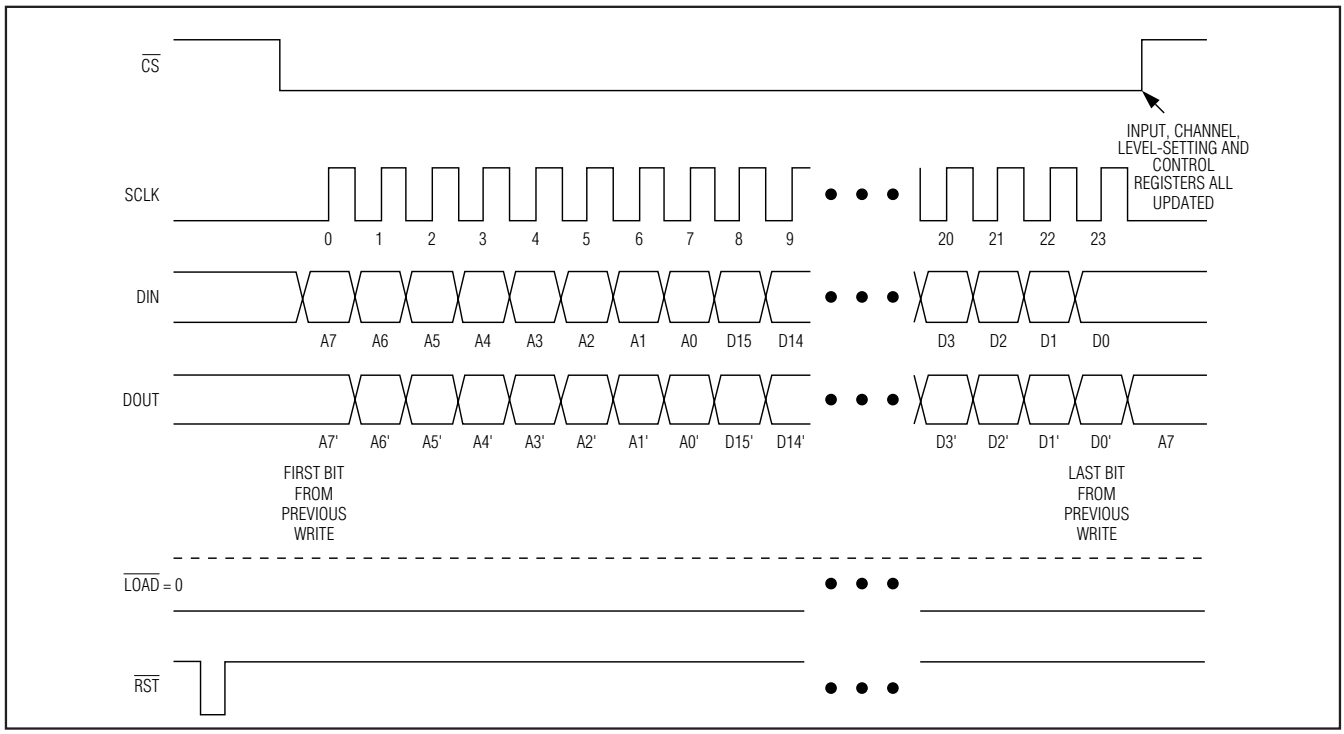



*Figure 11. Using $\overline{CS}$ to Update the Level-Setting and Control Registers ($\overline{LOAD}$ Held Low)*

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

## Table 16. MAX9979 Control and Calibration Register Bits

| REGISTER | FUNCTION |
|---|---|
| CDRP_ | Driver and comparator cable-droop compensation |
| CLENABLE_ | PMU clamp enable |
| DIFFERENTIAL0 | Select DATA1/NDATA1 as data control for both channels 1 and 2 (Figure 3) |
| DIFFERENTIAL1 | Enable differential comparator outputs (Figure 4) |
| $\overline{\text{DISABLE\_}}$ | PMU comparator output disable |
| ENVHHS_ | VHH_ mode enable |
| FMODE_ | PMU force-mode control |
| GCAL_ | DAC gain calibration |
| $\overline{\text{HIZFORCE\_}}$ | PMU DUT_ high-impedance control |
| $\overline{\text{HIZMEASS\_}}$ | PMU measure output high-impedance control |
| HYST_ | High-speed comparator hysteresis select |
| HYSTEN_ | PMU comparator hysteresis enable |
| INVERT_ | DATA_/NDATA_ polarity control |
| LDCAL_ | Load calibration enable |
| LDDIS_ | Load disable |
| LLEAKS_ | DCL low-leak enable |
| MMODE_ | PMU measure-mode control |
| OCAL_ | DAC offset calibration |
| PMU-F_ | Force switch enable (Figure 6) |
| PMU-S_ | Sense switch enable (Figure 6) |
| PMUSENSE_ | PMU MEASV input control |
| RO_ | Driver output resistance select |
| RS_ | PMU current range select |
| SC_ | Driver slew-rate control |
| TMSEL_ | Driver terminate select control |
| TMUX_ | Factory use only. Program to 0. |

## Table 17. Serial-Input Data Overview

| BIT | FUNCTION |
|---|---|
| A7 | Not used. Write 0 or 1 |
| A6 | Calibration register write enable |
| A5 | Channel 1 write enable |
| A4 | Channel 0 write enable |
| A3–A0 | Register address (see Table 18) |
| D15–D0 | Register data (see Table 19) |

## Table 18. Register Address Bits

| BITS | | | | REGISTER | |
|---|---|---|---|---|---|
| A3 | A2 | A1 | A0 | A6 = 0 | A6 = 1 |
| 0 | 0 | 0 | 0 | DCL control | DCL calibration |
| 0 | 0 | 0 | 1 | DHV level | DHV calibration |
| 0 | 0 | 1 | 0 | DLV level | DLV calibration |
| 0 | 0 | 1 | 1 | DTV level | DTV calibration |
| 0 | 1 | 0 | 0 | CHV level/PMU IVMAX | CHV calibration |
| 0 | 1 | 0 | 1 | CLV level/PMU IVMIN | CLV calibration |
| 0 | 1 | 1 | 0 | CPHV level | CPHV calibration |
| 0 | 1 | 1 | 1 | CPLV level | CPLV calibration |
| 1 | 0 | 0 | 0 | PMU control | — |
| 1 | 0 | 0 | 1 | VIN level | VIN calibration |
| 1 | 0 | 1 | 0 | VCOM level | VCOM calibration |
| 1 | 0 | 1 | 1 | VLDH level | VLDH calibration |
| 1 | 1 | 0 | 0 | VLDL level | VLDL calibration |
| 1 | 1 | 0 | 1 | VIOS/IIOS* level | VIOS/IIOS* calibration |
| 1 | 1 | 1 | 0 | CLAMPHI/VHH level | CLAMPHI/VHH calibration |
| 1 | 1 | 1 | 1 | CLAMPLO level | CLAMPLO calibration |

**Channel 0 register programs the VIOS level; channel 1 register programs the IIOS level. Select channels with bits A4 and A5.*

## Table 19. Data Bit Assignments*

| BIT | DCL CONTROL REGISTER** | DCL CALIBRATION REGISTER** | PMU CONTROL REGISTER** | LEVEL-SETTER REGISTER | DAC GAIN AND OFFSET CALIBRATION REGISTERS | |
|---|---|---|---|---|---|---|
| | | | | | VIN | ALL OTHERS |
| D0 | SC0 | RO0 | FMODE_ | Bit 0 (LSB) | OCAL0 | OCAL0 |
| D1 | SC1 | RO1 | MMODE_ | Bit 1 | OCAL1 | OCAL1 |
| D2 | LLEAKS | RO2 | RS0_ | Bit 2 | OCAL2 | OCAL2 |
| D3 | TMSEL | RO3 | RS1_ | Bit 3 | OCAL3 | OCAL3 |
| D4 | LDDIS | HYST0 | RS2_ | Bit 4 | OCAL4 | OCAL4 |
| D5 | INVERT | HYST1 | CLENABLE_ | Bit 5 | OCAL5 | OCAL5 |
| D6 | DIFFERENTIAL | HYST2 | $\overline{\text{HIZFORCE\_}}$ | Bit 6 | OCAL6 | OCAL6 |
| D7 | LDCAL | CDRP0 | $\overline{\text{HIZMEASS\_}}$ | Bit 7 | OCAL7 | OCAL7 |
| D8 | ENVHHS | CDRP1 | $\overline{\text{DISABLE\_}}$ | Bit 8 | GCAL0 | GCAL0 |
| D9 | TMUX0 = 0 | CDRP2 | PMUSENSE_ | Bit 9 | GCAL1 | GCAL1 |
| D10 | TMUX1 = 0 | — | HYSTEN_ | Bit 10 | GCAL2 | GCAL2 |

**The data bits enter the shift register in the order, MSB to LSB.*

***The DCL control, DCL calibration, and PMU control registers default to 0x0004, 0x0008, and 0x0003 respectively at power-up.*

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

**Table 19. Data Bit Assignments* (continued)**

| BIT | FUNCTION | | | | | |
|---|---|---|---|---|---|---|
| | DCL CONTROL REGISTER** | DCL CALIBRATION REGISTER** | PMU CONTROL REGISTER** | LEVEL-SETTER REGISTER | DAC GAIN AND OFFSET CALIBRATION REGISTERS | |
| | | | | | VIN | ALL OTHERS |
| D11 | TMUX2 = 0 | — | PMU-F | Bit 11 | GCAL3 | GCAL3 |
| D12 | TMUX3 = 0 | — | PMU-S | Bit 12 | GCAL4 | GCAL4 |
| D13 | — | — | — | Bit 13 | GCAL5 | GCAL5 |
| D14 | — | — | — | Bit 14 | GCAL6 | — |
| D15 | — | — | — | Bit 15 (MSB) | — | — |

*The data bits enter the shift register in the order, MSB to LSB.*

***The DCL control, DCL calibration, and PMU control registers default to 0x0004, 0x0008, and 0x0003 respectively at power-up.*

### Level-Setting DACs

The MAX9979 includes 28 level-setting DACs that provide the DC voltage levels for the various control and monitor circuits of the 2-channel MAX9979. Some of the DACs are shared between the MAX9979 channels, and some perform dual functions within a channel (Figure 12). Important details about the operation of shared DACs are:

- VIOS share a common DAC level for both channels. VIOS DAC simultaneously updates the VIOS1 and VIOS2 levels.
- IIOS share a common DAC level for both channels. The IIOS DAC simultaneously updates the IIOS1 and IIOS2 levels.
- CLAMPHI_ and VHH_ share a common DAC level. The CLAMPHI_/VHH_ DAC simultaneously updates the CLAMPHI_ and VHH_ levels. Note that the VHH_ output is 0 to +13V. If CLAMPHI_ is set to a negative value and the VHH_ mode is selected, the VHH_ output limits close to 0V.
- CHV_ and IVMAX_ share a common DAC level. The CHV_/IVMAX_ DAC simultaneously updates the CHV_ and IVMAX_ levels.
- CLV_ and IVMIN_ share a common DAC level. The CLV_/IVMIN_ DAC simultaneously updates the CLV_ and IVMIN_ levels.

A 16-bit code that varies between 0x0000 and 0xFFFF sets all DAC levels. Table 20 presents a list of the DACs and their default values.

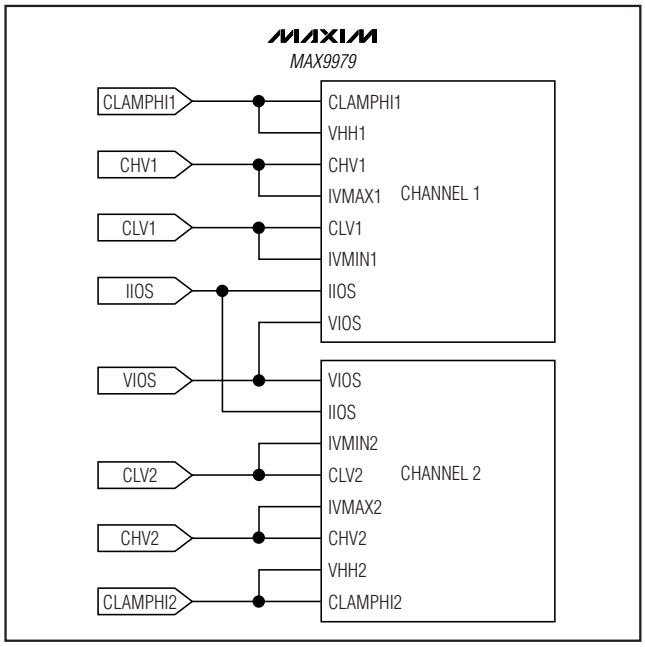



*Figure 12. Arrangement of Shared DACs*

### Calibrating DAC Gain and Offset

DAC calibration registers adjust the gain and offset of each DAC. Each DAC has at least one calibration register. All DAC calibration registers are programmed with a 14-bit code, except VIN_, which uses a 15-bit code (Table 19). The codes are divided into two fields, one field each for gain (GCAL_) and offset (OCAL_). VIN_ has a 7-bit field for gain and an 8-bit field for offset. All other DACs have a 6-bit field for gain and an 8-bit field for offset.

The VCH_, VCL_, and VIN_ DACs have duplicate calibration registers that are selected and addressed as a function of the selected DCL/PMU modes. The VCH_ and VCL_ registers each have three separate calibration registers that are used by the window comparator, the differential comparator, and the PMU comparator, respectively. The VIN_ register features six duplicate calibration registers that are selected as a function of the PMU force mode. These registers are individually addressed by first selecting the appropriate mode, then performing the register write. After the calibration registers are programmed, the appropriate register is automatically switched in as a function of the operating mode.

Table 20 presents a list of the DAC registers and their default values. Calibration registers are programmed to default values only during a power-on reset. Asserting $\overline{RST}$ does not force the calibration registers to their default values. Table 21 summarizes the DAC register addresses. Figure 13 shows how the calibration registers affect the DAC outputs.

## Table 20. DAC Power-Up and Reset Default Values

| DAC | DESCRIPTION | LEVEL-SETTING REGISTER POWER-UP AND $\overline{RST}$ VALUE | CALIBRATION REGISTER POWER-UP VALUE* |
|---|---|---|---|
| DHV_ | Driver high | 0x4000 | 0x2080 |
| DLV_ | Driver low | 0x4000 | 0x2080 |
| DTV_ | Driver term | 0x4000 | 0x2080 |
| CHV_/IVMAX_ | High comparator/PMU high comparator | 0x4000 | 0x2080 |
| CLV_/IVMIN_ | Low comparator/PMU low comparator | 0x4000 | 0x2080 |
| CPHV_ | High high-impedance clamp | 0x4000 | 0x2080 |
| CPLV_ | Low high-impedance clamp | 0x4000 | 0x2080 |
| VIN_ | PMU force value | 0x4000 | 0x4080 |
| VCOM_ | Load commutation voltage | 0x4000 | 0x2080 |
| VLDH_ | Load source current | 0x4000 | 0x2080 |
| VLDL_ | Load sink current | 0x4000 | 0x2080 |
| VIOS | PMU measure voltage offset | 0x4000 | 0x2080 |
| IIOS | PMU force/measure current offset | 0x4000 | 0x2080 |
| CLAMPHI_/VHH_ | PMU high clamp/driver super voltage | 0x4000 | 0x2080 |
| CLAMPLO_ | PMU low clamp | 0x4000 | 0x2080 |

**Calibration registers not affected by $\overline{RST}$.*

## Table 21. DAC Level-Setting and Calibration Register Addresses

| DAC | DESCRIPTION | LEVEL-SETTING REGISTER ADDRESS | | | CALIBRATION REGISTER ADDRESS | | | NOTES |
|---|---|---|---|---|---|---|---|---|
| | | Ch 0 | Ch 1 | Both | Ch 0 | Ch 1 | Both | |
| DHV_ | Driver high | 0x11 | 0x21 | 0x31 | 0x51 | 0x61 | 0x71 | — |
| DLV_ | Driver low | 0x12 | 0x22 | 0x32 | 0x52 | 0x62 | 0x72 | — |
| DTV_ | Driver term | 0x13 | 0x23 | 0x33 | 0x53 | 0x63 | 0x73 | — |
| CHV_/IVMAX_ | High comparator/PMU high comparator | 0x14 | 0x24 | 0x34 | 0x54 | 0x64 | 0x74 | 1, 3 |
| CLV_/IVMIN_ | Low comparator/PMU low comparator | 0x15 | 0x25 | 0x35 | 0x55 | 0x65 | 0x75 | 2, 3 |
| CPHV_ | High high-impedance clamp | 0x16 | 0x26 | 0x36 | 0x56 | 0x66 | 0x76 | — |
| CPLV_ | Low high-impedance clamp | 0x17 | 0x27 | 0x37 | 0x57 | 0x67 | 0x77 | — |
| VIN_ | PMU force value | 0x19 | 0x29 | 0x39 | 0x59 | 0x69 | 0x79 | 3 |
| VCOM_ | Load commutation voltage | 0x1A | 0x2A | 0x3A | 0x5A | 0x6A | 0x7A | — |
| VLDH_ | Load source current | 0x1B | 0x2B | 0x3B | 0x5B | 0x6B | 0x7B | — |
| VLDL_ | Load sink current | 0x1C | 0x2C | 0x3C | 0x5C | 0x6C | 0x7C | — |
| VIOS | PMU measure voltage offset | 0x1D | — | — | 0x5D | - | — | 4 |
| IIOS | PMU force/measure current offset | — | 0x2D | — | — | 0x6D | — | 5 |
| CLAMPHI_/VHH_ | PMU high clamp/driver super voltage | 0x1E | 0x2E | 0x3E | 0x5E | 0x6E | 0x7E | 3, 6 |
| CLAMPLO_ | PMU low clamp | 0x1F | 0x2F | 0x3F | 0x5F | 0x6F | 0x7F | — |

**Note 1:** A common DAC is used for both the CHV_ and IVMAX_ levels.

**Note 2:** A common DAC is used for both the CLV_ and IVMIN_ levels.

**Note 3:** The CHV_ and CLV_ levels each have a pair of calibration registers. One is active when using the window comparator; the other is active when using the differential comparator. The VIN_ level has six calibration registers corresponding to the force voltage and the five ranges of force current modes of the PMU. The CLAMPHI_, VHH_, IVMAX_, and IVMIN_ levels each have their own dedicated calibration register. Addressing any of these calibration registers requires device mode settings (Table 22) as well as the register's address.

**Note 4:** The VIOS level is common to both channels. A channel 0 DAC is used to generate VIOS.

**Note 5:** The IIOS level is common to both channels. A channel 1 DAC is used to generate IIOS.

**Note 6:** A common DAC is used for both the CLAMPHI_ and VHH_ levels.

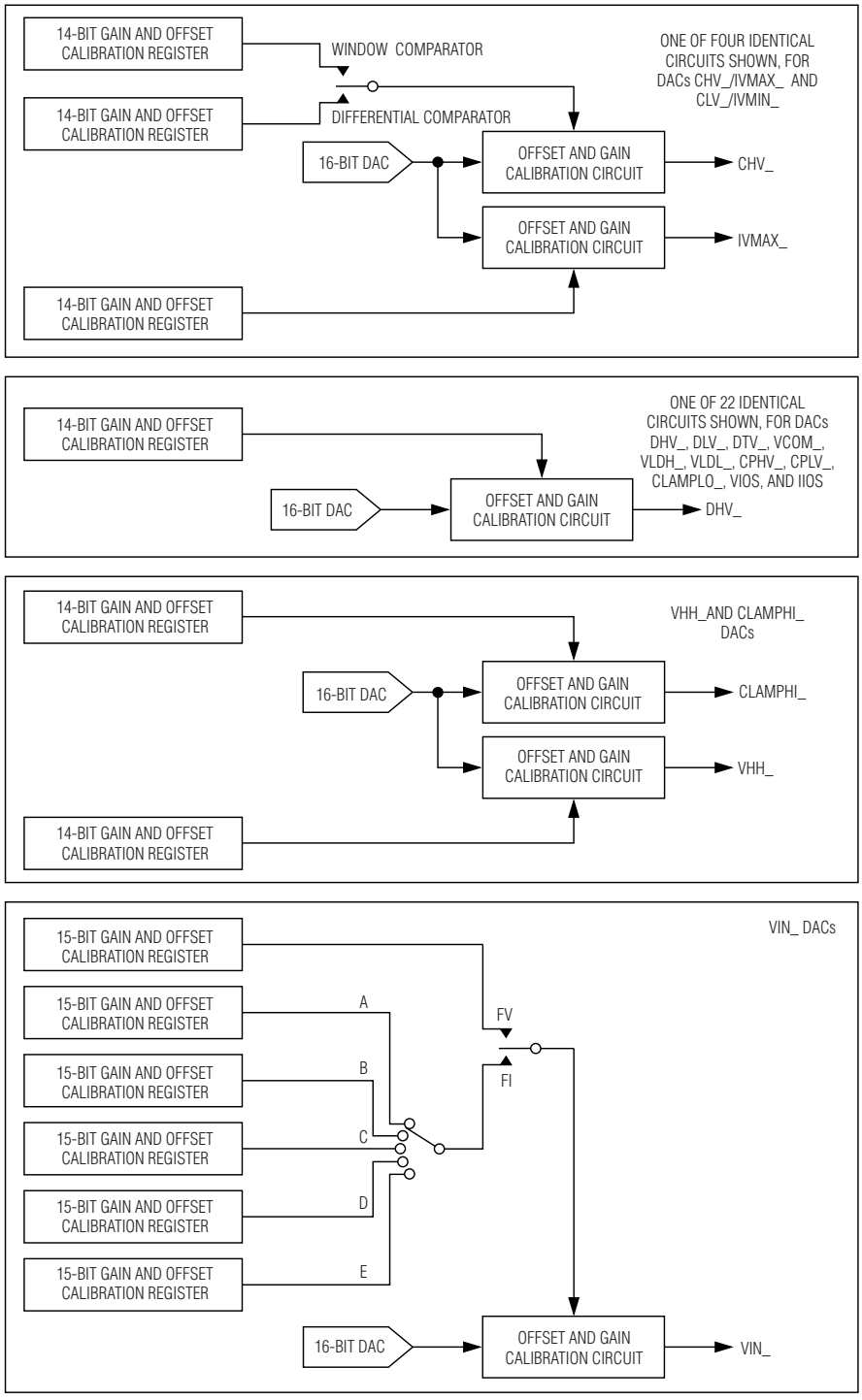



*Figure 13. DAC Calibration Registers*

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

An example calibration sequence follows:

1) Power up the MAX9979. This sets the level-setting DACs to their default 0V values, and the gain and offset calibration registers to their default midscale values (Table 20).
2) Gain calibration (gain must be calibrated before calibrating offset).
   a. Program a level-setting DAC to its minimum value and measure the output voltage ($V_{OUT\_MIN}$). Then, reprogram the DAC to its maximum value and again measure the output voltage ($V_{OUT\_MAX}$). Calculate the gain using the following equation:

$$GAIN = \frac{V_{OUT\_MAX} - V_{OUT\_MIN}}{V_{SET\_MAX} - V_{SET\_MIN}}$$

where $V_{SET\_MAX}$ and $V_{SET\_MIN}$ are the desired gain calibration points.

   b. Set the DACs gain calibration register until the gain is as close to 1 as possible. This calibrates the gain for the DAC. Record the gain calibration register value for later use.
3) Offset calibration (must be done after the gain calibration).
   a. Set the level of the DAC to the desired offset calibration point (e.g., midscale).
   b. Measure $V_{OUT\_}$ and compare it to the expected output.
   c. Adjust the offset calibration register until $V_{OUT\_}$ is as close as possible to the expected voltage. Record the value of the offset calibration register for later use.
4) Repeat the above procedure for all DACs that need calibration, recording each of the gain and offset calibration register settings for later use.

The prior procedure only needs to be done once. Each time the power is cycled, simply reprogram the gain and offset registers using the recorded values.

Table 22 presents the mode settings required to access the calibration registers of the shared DACs. In some cases there is more than one way to access the register.

## Table 22. Mode-Control Settings to Access Calibration Registers of Shared DACs

| CALIBRATION REGISTER | | SERIAL-INTERFACE BITS | | | | | | |
|---|---|---|---|---|---|---|---|---|
| DAC | MODE | $\overline{HIZFORCE\_}$ | DIFFERENTIAL1 | FMODE_ | MMODE_ | RS_ BIT | | |
| | | | | | | 2 | 1 | 0 |
| CLV_, CHV_ | Window | 0 | 0 | X | X | X | X | X |
| | Differential | 0 | 1 | X | X | X | X | X |
| IVMAX_, IVMIN_ | — | 1 | X | X | X | X | X | X |
| CLAMPHI_ | — | 1 | X | X | X | X | X | X |
| VHH_ | — | 0 | X | X | X | X | X | X |
| VIN_ | FV* | 0 | X | X | 0 | X | X | X |
| | | 1 | X | 0 | X | | | |
| | FI Range A | 1 | X | 1 | X | 1 | X | X |
| | FI Range B* | 0 | X | X | 1 | 1 | X | X |
| | | 0 | X | X | 1 | 0 | 1 | 1 |
| | | 1 | X | 1 | X | | | |
| | FI Range C* | 0 | X | X | 1 | 0 | 1 | 0 |
| | | 1 | X | 1 | X | | | |
| | FI Range D* | 0 | X | X | 1 | 0 | 0 | 1 |
| | | 1 | X | 1 | X | | | |
| | FI Range E* | 0 | X | X | 1 | 0 | 0 | 0 |
| | | 1 | X | 1 | X | | | |

**Any of these conditions allow access to the calibration register.*

### DAC Output Level Transfer Functions

Each of the MAX9979 analog DAC levels is set with a transfer function that includes the 16-bit DAC code setting, the gain code setting, and the offset code setting. The $V_{DAC}$ and $V_{VINDAC}$ expressions below present the basic DAC transfer functions. Each DAC has a voltage output range of -2.5V to +7.5V (typ). Thirteen of these DACs are identical and generate a potential according to the following equation:

$$V_{DAC} = \left( \left( \left( \frac{DAC_{CODE}}{16384} - 1 \right) \times (V_{REF} - V_{DGS}) + \right) \right.$$
$$\left. (OFFSET_{CODE} \times 0.001) - 0.128 \right)$$
$$\times \left( 0.98 + 0.02 \times \left( \frac{GAIN_{CODE}}{32} \right) \right) + V_{DGS}$$

A separate DAC (VIN_) is used for the PMU force value. This DAC has a finer gain adjustment resolution and follows the equation:

$$V_{VINDAC} = \left( \left( \frac{DAC_{CODE}}{16384} - 1 \right) \times (V_{REF} - V_{DGS}) \right.$$
$$\left. + (OFFSET_{CODE} \times 0.001) - 0.128 \right)$$
$$\times \left( 0.98 + 0.02 \times \left( \frac{GAIN_{CODE}}{64} \right) \right) + V_{DGS}$$

For all DACs, the offset code is an integer value between 0 and 255. The VIN_DAC gain code is an integer value between 0 and 127, and for all other DACs the gain code is an integer value between 0 and 63. Offset and gain codes are based on the calibration register settings.

## Table 23. DAC Transfer Functions

| LEVEL | LEVEL TRANSFER FUNCTION |
|---|---|
| DHV_ | $V_{DAC}$ x DHV_ gain + DHV_ offset |
| DLV_ | $V_{DAC}$ x DLV_ gain + DLV_ offset |
| DTV_ | $V_{DAC}$ x DTV_ gain + DTV_ offset |
| CHV_ | $V_{DAC}$ x CHV_ gain + CHV_ offset |
| IVMAX_ | $V_{DAC}$ x IVMAX_ gain + IVMAX_ offset |
| CLV_ | $V_{DAC}$ x CLV_ gain + CLV_ offset |
| IVMIN_ | $V_{DAC}$ x IVMIN_ gain + IVMIN_ offset |
| CPHV_ | $V_{DAC}$ x CPHV_ gain + CPHV_ offset |
| CPLV_ | $V_{DAC}$ x CPLV_ gain + CPLV_ offset |
| VIN_ (FVMI) | $V_{VINDAC}$ x PMU_FV_ gain + PMU_FV_ offset |
| VIN_ (FIMV 50mA) | ($V_{VINDAC}$ - $V_{IIOS}$) x (50mA/4V) x PMU_FI_ gain + PMU_FI_ offset |
| VIN_ (FIMV 2mA) | ($V_{VINDAC}$ - $V_{IIOS}$) x (2mA/4V) x PMU_FI_ gain + PMU_FI_ offset |
| VIN_ (FIMV 200_A) | ($V_{VINDAC}$ - $V_{IIOS}$) x (200_A/4V) x PMU_FI_ gain + PMU_FI_ offset |
| VIN_ (FIMV 20_A) | ($V_{VINDAC}$ - $V_{IIOS}$) x (20_A/4V) x PMU_FI_ gain + PMU_FI_ offset |
| VIN_ (FIMV 2_A) | ($V_{VINDAC}$ - $V_{IIOS}$) x (2_A/4V) x PMU_FI_ gain + PMU_FI offset |
| VCOM_ | $V_{DAC}$ x VCOM_ gain + VCOM_ offset |
| VLDH_ | ($V_{DAC}$ - DGS) x (20mA/6V) x VLDH_ gain + VLDH_ offset |
| VLDL_ | ($V_{DAC}$ - DGS) x (20mA/6V) x VLDL_ gain + VLDL_ offset |
| VIOS | (($V_{DAC}$ + DGS)/2) x VIOS gain + VIOS offset |
| IIOS | (($V_{DAC}$ + REF)/2) x IIOS gain + IIOS offset |
| VHH_ | ($V_{DAC}$ - DGS) x 2 x VHH_ gain + VHH_ offset + DGS |
| CLAMPHI_ (Voltage) | $V_{DAC}$ x CLAMPHI_ gain + CLAMPHI_ offset |
| CLAMPHI_ (Current) | ($V_{DAC}$ - $V_{IIOS}$) x FSR/2V x CLAMPHI_ gain + CLAMPHI_ offset |
| CLAMPLO_ (Voltage) | $V_{DAC}$ x CLAMPLO_ gain + CLAMPLO_ offset |
| CLAMPLO_ (Current) | ($V_{DAC}$ - $V_{IIOS}$) x FSR/2V x CLAMP_LO_ gain + CLAMPLO_ offset |

- Values for PMU_FI_ gain and PMU_FI_ offset are different for each PMU current range.
- VLDH_ and VLDL_ levels less than zero are truncated.
- Full-scale range is dependent upon the PMU current range. Values are 100mA, 4mA, 400µA, 40µA, and 4µA for ranges A–E, respectively.
- Values for CLAMPHI_ gain, CLAMPLO_ gain, CLAMPHI_ offset, and CLAMPLO_ offset vary with PMU force mode and current range.

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

The $V_{DAC}$ voltages are then utilized for the various signal paths within the MAX9979 (i.e., driver level DHV_). Each of these signal paths have inherent gain and offset errors, denoted as _gain and _offset terms in the Level Transfer Function column in Table 23. These error terms are presented to convey the non-ideal gain and offset of the signal paths—they do not have a specified value. The $GAIN_{CODE}$ and $OFFSET_{CODE}$ features of each DAC are designed to correct for these errors to make the level transfer function expressions, and therefore, the final signal path outputs (e.g., DHV_) more ideal.

## Applications Information

### Device Power-Up State

Upon power-up, the DCL enters low-leak mode and the PMU enters high-impedance mode. The DCL control, DCL calibration, and PMU control registers default to 0x0004, 0x0008, and 0x0003, respectively. For initial power-up values for the level-setting registers, see Table 20. Power supplies may be powered on in any sequence.

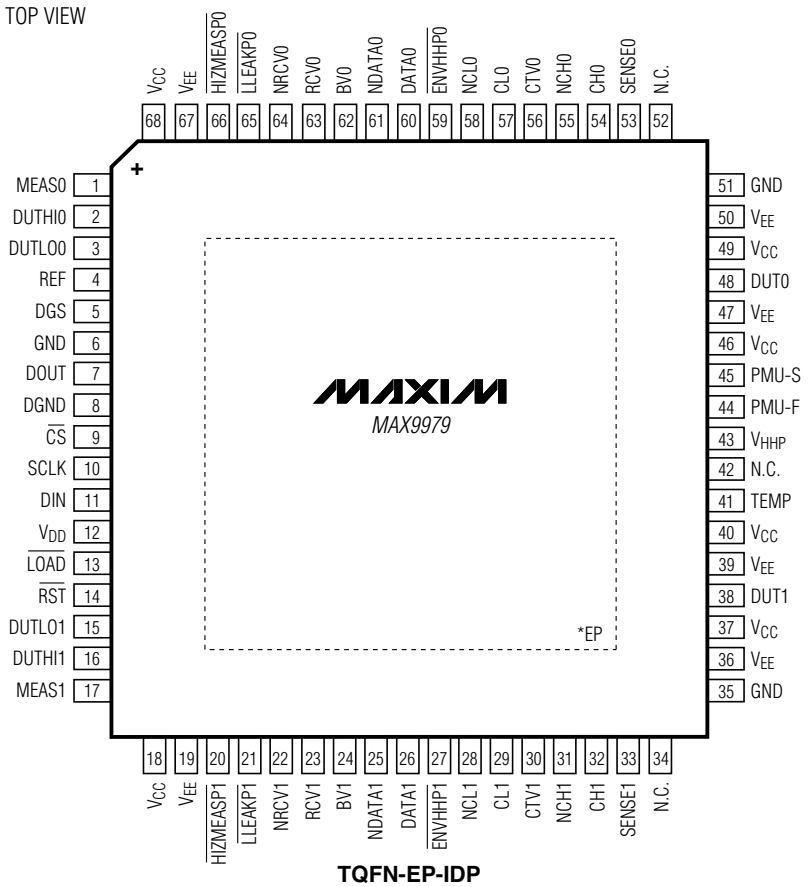
### Power-Supply Considerations

Bypass each supply input to GND and REF to DGS with 0.1µF capacitors (Figure 13). Additionally, use bulk bypassing of at least 10µF where the power-supply connections meet the circuit board.

### Exposed Pad

The exposed pad is internally connected to ground. Connect to a open copper PCB ground plane or heatsink to maximize thermal performance. Not intended as an electrical connection point.

## Pin Configuration

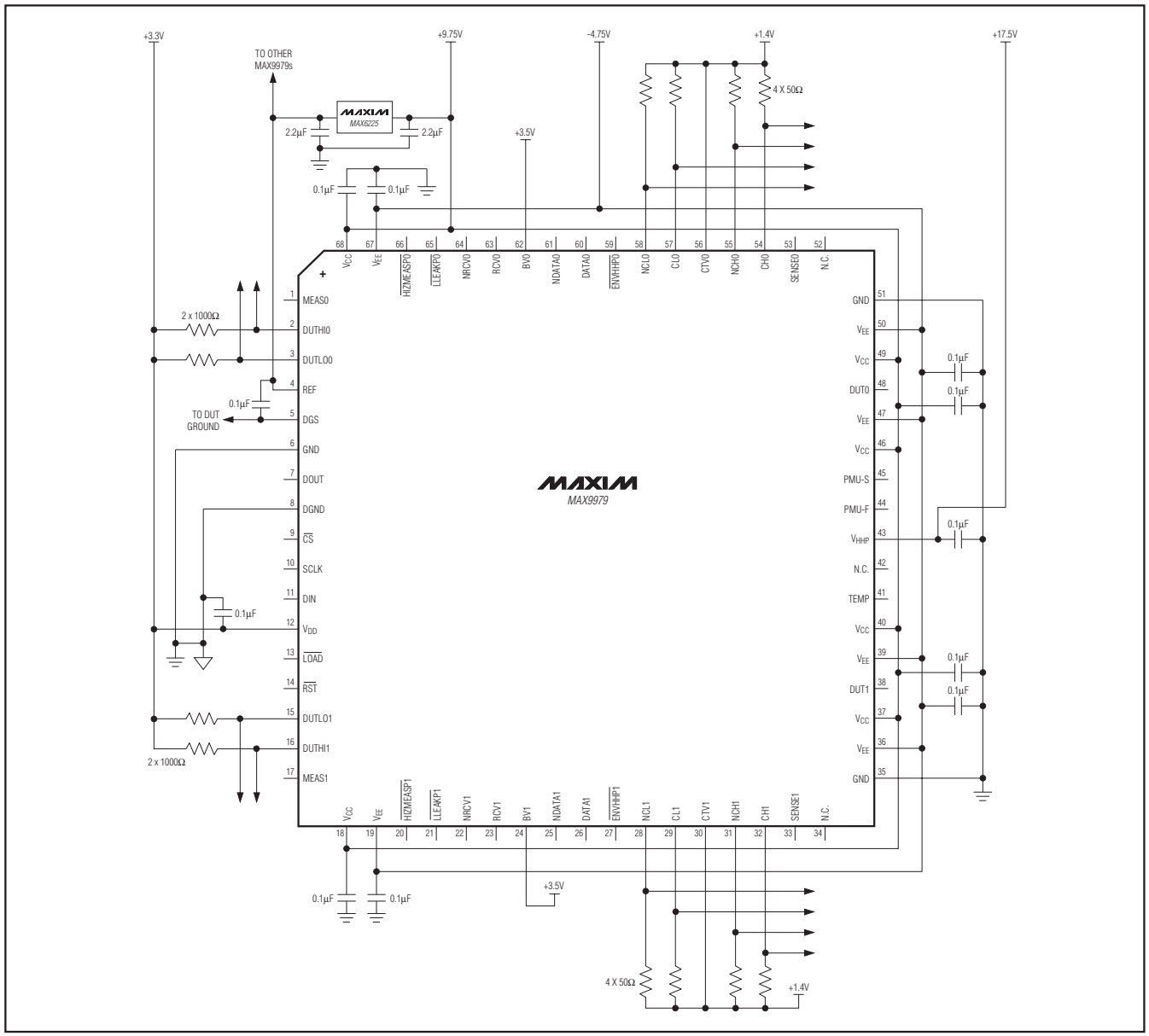



**TQFN-EP-IDP**

*EP = EXPOSED PAD.

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

## Typical Operating Circuit




## Chip Information

PROCESS: BiCMOS

## Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 68 TQFN-EP-IDP | T6800RN+6 | 21-0192 | 90-0090 |

# Dual 1.1Gbps Pin Electronics with Integrated PMU and Level-Setting DACs

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 6/08 | Initial release | — |
| 1 | 10/08 | Corrected error in Table 2 and formula on page 57 | 36, 57 |
| 2 | 12/08 | Added new Tables 6 and 7 and renumbered subsequent tables | 37, 38, 41, 42, 44, 45, 46, 48, 50–54, 56, 57, 58 |
| 3 | 4/09 | Made spec changes and clarifications | 5–8, 20, 57 |
| 4 | 6/09 | Corrected *Typical Operating Circuit* | 59 |
| 5 | 1/11 | Updated *Pin Description, Exposed Pad* section, and *Package Information* | 33, 58, 59 |
| 6 | 8/11 | Clarified use of exposed die attach pad | 33, 58 |