
HM628511HI Series

4M High Speed SRAM (512-kword $\times$ 8-bit)

HITACHI

ADE-203-1035A (Z)

Rev. 1.0

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Description

The HM628511HI Series is a 4-Mbit high speed static RAM organized 512-k word $\times$ 8-bit. It has realized high speed access time by employing CMOS process (4-transistor + 2-poly resistor memory cell) and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. It is packaged in 400-mil 36-pin plastic SOJ.

Features

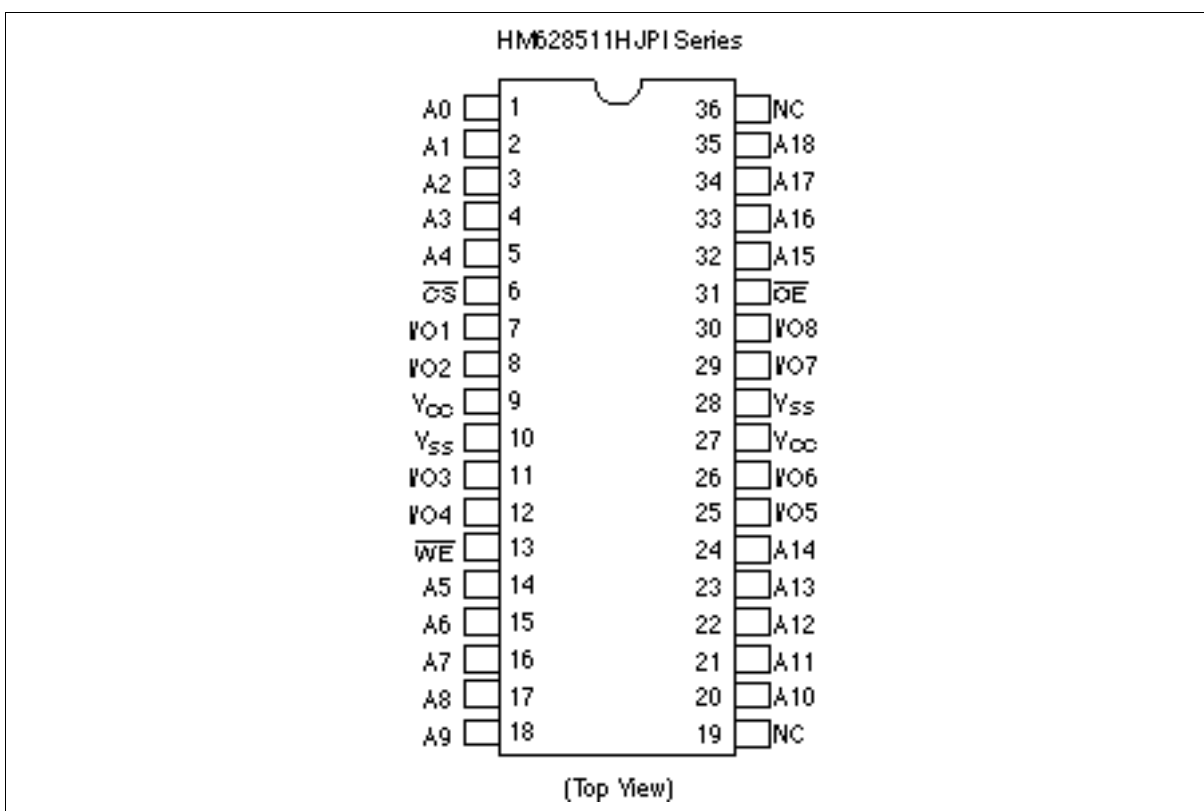
- Single 5.0 V supply : 5.0 V $\pm$ 10 %
- Access time 12 / 15 ns (max)
- Completely static memory
 - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
 - All inputs and outputs
- Operating current : 160 / 140 mA (max)
- TTL standby current : 60 / 50 mA (max)
- CMOS standby current : 5 mA (max)
- Center V_{CC} and V_{SS} type pinout
- Temperature range: -40 to 85°C

HM628511HI Series

Ordering Information

Type No.	Access time	Package
HM628511HJPI-12	12 ns	400-mil 36-pin plastic SOJ (CP-36D)
HM628511HJPI-15	15 ns	

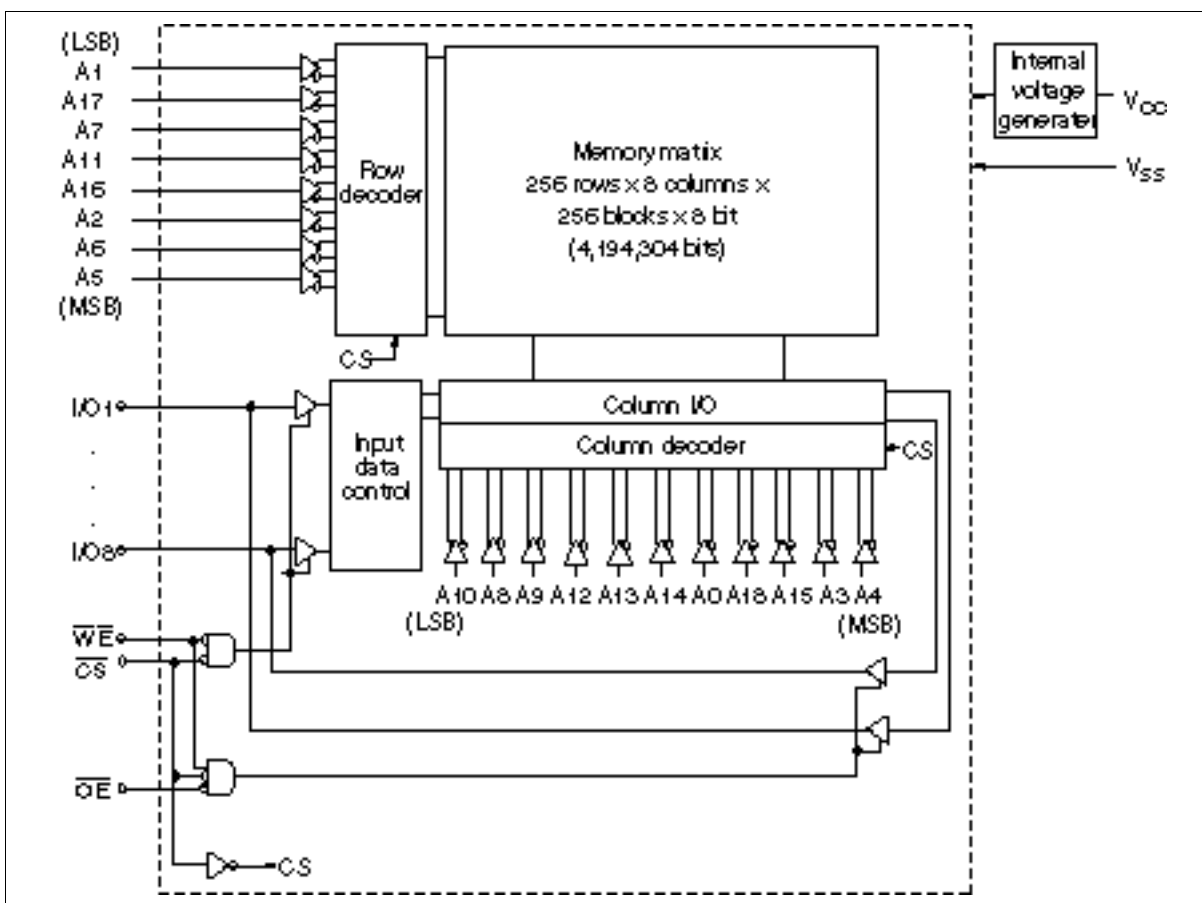
Pin Arrangement



Pin Description

Pin name	Function
A0 to A18	Address input
I/O1 to I/O8	Data input/output
CS	Chip select
OE	Output enable
WE	Write enable
V _{CC}	Power supply
V _{SS}	Ground
NC	No connection

Block Diagram



HM628511HI Series

Operation Table

CS	OE	WE	Mode	V _{CC} current	I/O	Ref. cycle
H	×	×	Standby	I _{SB} , I _{SB1}	High-Z	—
L	H	H	Output disable	I _{CC}	High-Z	—
L	L	H	Read	I _{CC}	Dout	Read cycle (1) to (3)
L	H	L	Write	I _{CC}	Din	Write cycle (1)
L	L	L	Write	I _{CC}	Din	Write cycle (2)

Note: ×: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V _{SS}	V _{CC}	−0.5 to +7.0	V
Voltage on any pin relative to V _{SS}	V _T	−0.5 ^{*1} to V _{CC} +0.5 ^{*2}	V
Power dissipation	P _T	1.0	W
Operating temperature	T _{opr}	−40 to +85	°C
Storage temperature	T _{stg}	−55 to +125	°C
Storage temperature under bias	T _{bias}	−40 to +85	°C

Notes: 1. V_T (min) = −2.0 V for pulse width (under shoot) 8 ns

2. V_T (max) = V_{CC}+2.0 V for pulse width (over shoot) 8 ns

Recommended DC Operating Conditions (T_a = −40 to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC} ^{*3}	4.5	5.0	5.5	V
	V _{SS} ^{*4}	0	0	0	V
Input voltage	V _{IH}	2.2	—	V _{CC} + 0.5 ^{*2}	V
	V _{IL}	−0.5 ^{*1}	—	0.8	V

Notes: 1. V_{IL} (min) = −2.0 V for pulse width (under shoot) 8 ns

2. V_{IH} (max) = V_{CC}+2.0 V for pulse width (over shoot) 8 ns

3. The supply voltage with all V_{CC} pins must be on the same level.

4. The supply voltage with all V_{SS} pins must be on the same level.

HM628511HI Series

DC Characteristics ($T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0\text{V}$)

Parameter		Symbol	Min	Typ* ¹	Max	Unit	Test conditions
Input leakage current		I_{LI}	—	—	2	μA	$V_{in} = V_{SS}$ to V_{CC}
Output leakage current		I_{LO}	—	—	2	μA	$V_{in} = V_{SS}$ to V_{CC}
Operation power supply current	12 ns cycle	I_{CC}	—	—	160	mA	Min cycle $CS = V_{IL}$, $I_{out} = 0\text{ mA}$ Other inputs = V_{IH}/V_{IL}
	15 ns cycle	I_{CC}	—	—	140		
Standby power supply current	12 ns cycle	I_{SB}	—	—	60	mA	Min cycle, $CS = V_{IH}$, Other inputs = V_{IH}/V_{IL}
	15 ns cycle	I_{SB}	—	—	50		
		I_{SB1}	—	0.1	5	mA	
Output voltage		V_{OL}	—	—	0.4	V	$I_{OL} = 8\text{ mA}$
		V_{OH}	2.4	—	—	V	$I_{OH} = -4\text{ mA}$

Notes: 1. Typical values are at $V_{CC} = 5.0\text{ V}$, $T_a = +25^\circ\text{C}$ and not guaranteed.

Capacitance ($T_a = +25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance* ¹		C_{in}	—	—	6	pF	$V_{in} = 0\text{ V}$
Input/output capacitance* ¹		$C_{I/O}$	—	—	8	pF	$V_{I/O} = 0\text{ V}$

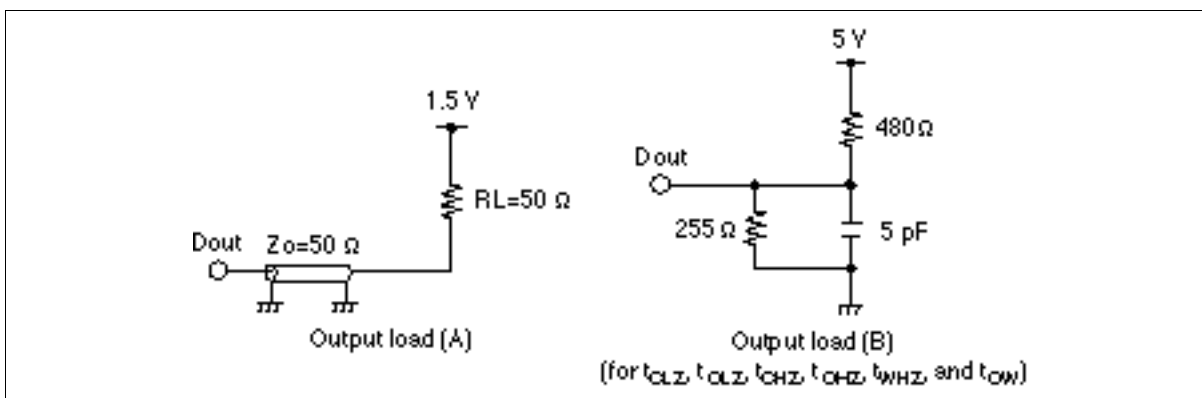
Note: 1. This parameter is sampled and not 100% tested.

HM628511HI Series

AC Characteristics ($T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, unless otherwise noted.)

Test Conditions

- Input pulse levels: 3.0 V/0.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures (Including scope and jig)



Read Cycle

		HM628511HI					
		-12		-15			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t _{RC}	12	—	15	—	ns	
Address access time	t _{AA}	—	12	—	15	ns	
Chip select access time	t _{ACS}	—	12	—	15	ns	
Output enable to outpput valid	t _{OE}	—	6	—	7	ns	
Output hold from address change	t _{OH}	3	—	3	—	ns	
Chip select to output in low-Z	t _{CLZ}	3	—	3	—	ns	1
Output enable to output in low-Z	t _{OLZ}	0	—	0	—	ns	1
Chip deselect to output in high-Z	t _{CHZ}	—	6	—	7	ns	1
Output disable to output in high-Z	t _{OHZ}	—	6	—	7	ns	1

Write Cycle

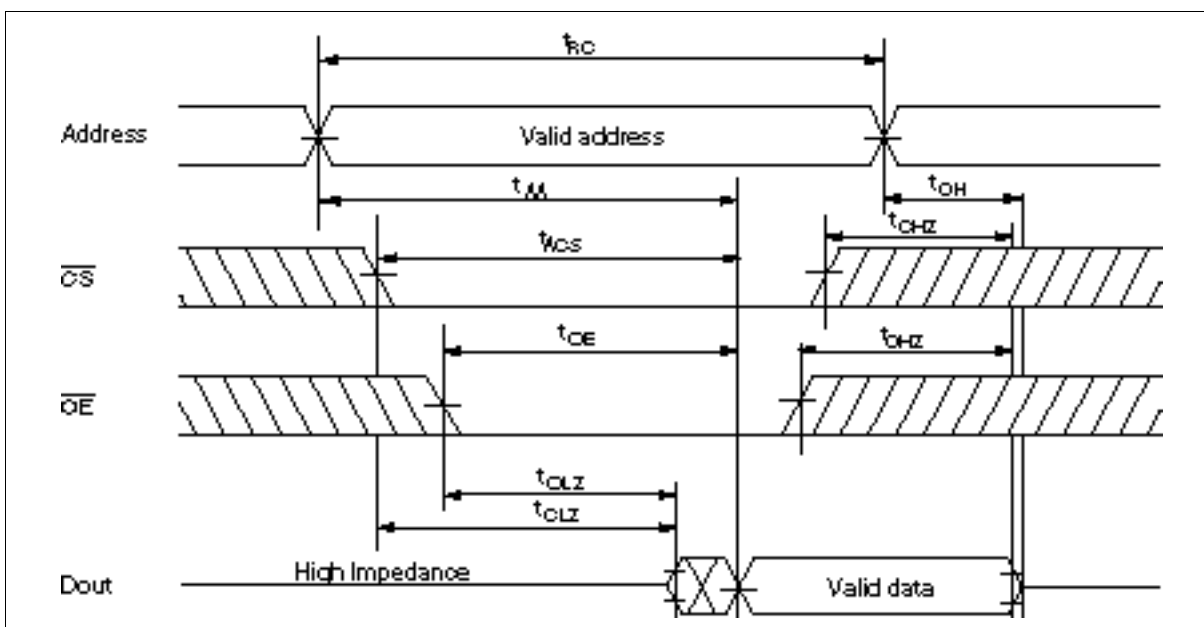
		HM628511HI					
		-12		-15			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write cycle time	t _{WC}	12	—	15	—	ns	
Address valid to end of write	t _{AW}	8	—	10	—	ns	
Chip select to end of write	t _{CW}	8	—	10	—	ns	9
Write pulse width	t _{WP}	8	—	10	—	ns	8
Address setup time	t _{AS}	0	—	0	—	ns	6
Write recovery time	t _{WR}	0	—	0	—	ns	7
Data to write time overlap	t _{DW}	6	—	7	—	ns	
Data hold from write time	t _{DH}	0	—	0	—	ns	
Write disable to output in low-Z	t _{OW}	3	—	3	—	ns	1
Output disable to output in high-Z	t _{OHZ}	—	6	—	7	ns	1
Write enable to output in high-Z	t _{WHZ}	—	6	—	7	ns	1

- Note:
1. Transition is measured ± 200 mV from steady voltage with Load (B). This parameter is sampled and not 100% tested.
 2. Address should be valid prior to or coincident with CS transition low.
 3. WE and/or CS must be high during address transition time.
 4. If CS and OE are low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
 5. If the CS low transition occurs simultaneously with the WE low transition or after the WE transition, output remains a high impedance state.
 6. t_{AS} is measured from the latest address transition to the later of CS or WE going low.
 7. t_{WR} is measured from the earlier of CS or WE going high to the first address transition.
 8. A write occurs during the overlap of a low CS and a low WE. A write begins at the latest transition among CS going low and WE going low. A write ends at the earliest transition among CS going high and WE going high. t_{WP} is measured from the beginning of write to the end of write.
 9. t_{CW} is measured from the later of CS going low to the the end of write.

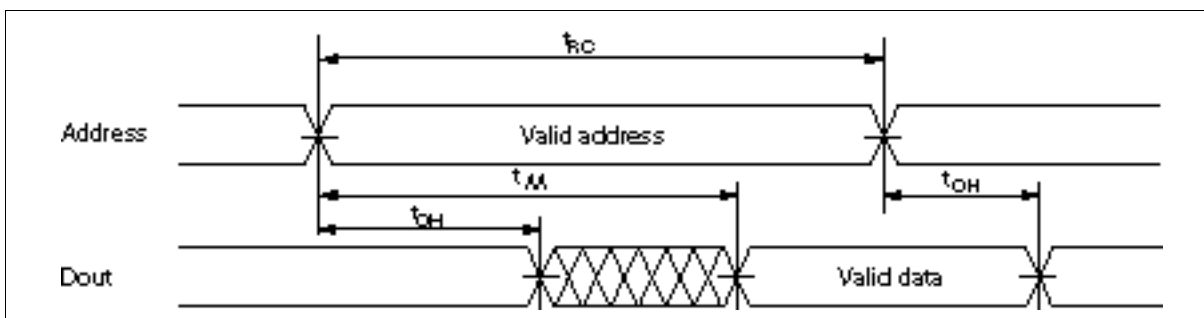
HM628511HI Series

Timing Waveforms

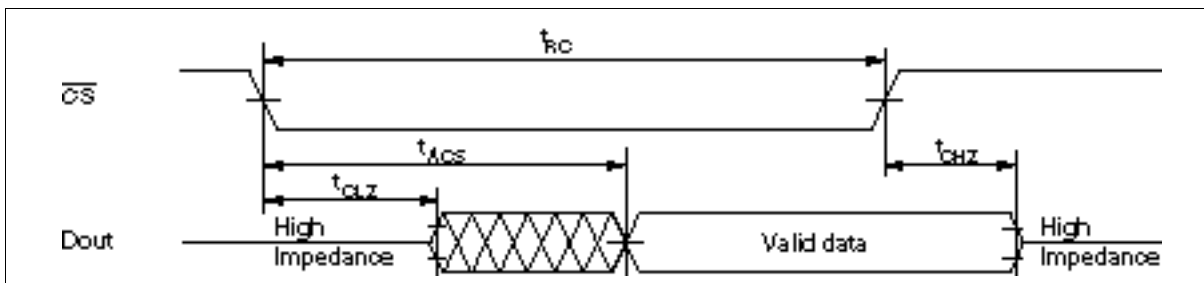
Read Timing Waveform (1) ($WE = V_{IH}$)



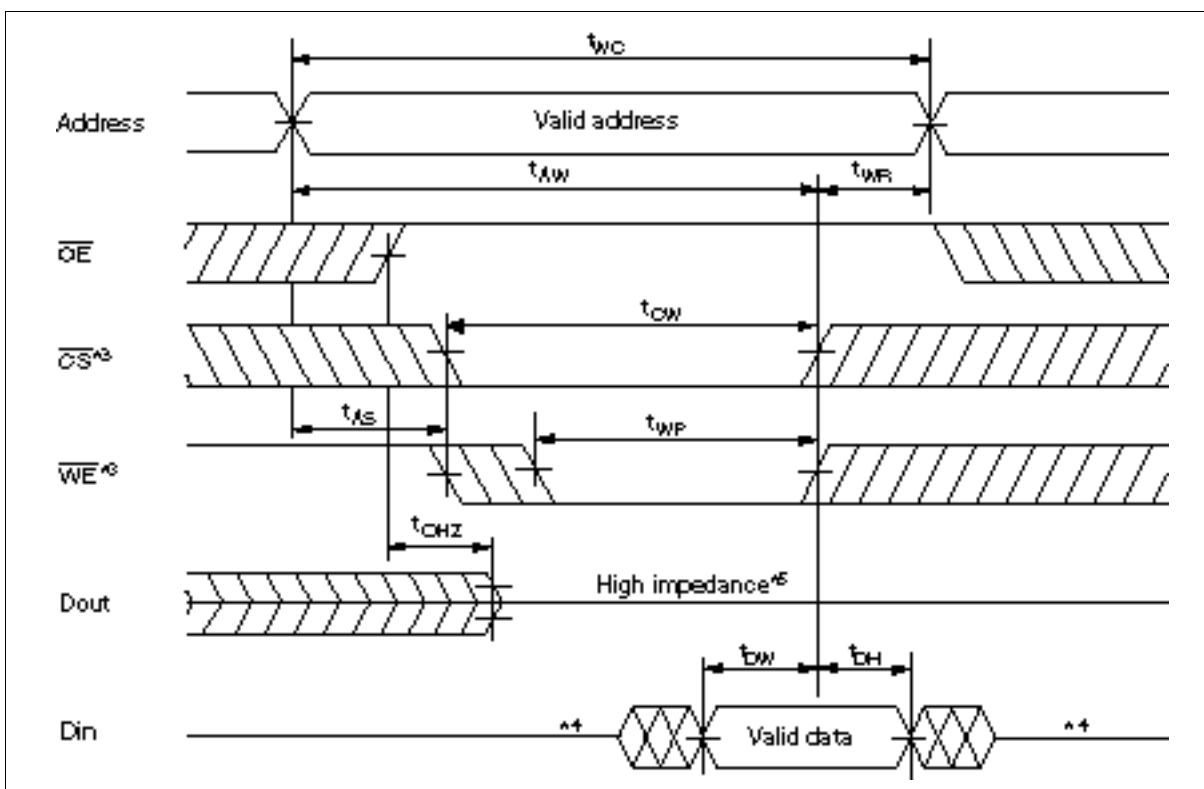
Read Timing Waveform (2) ($WE = V_{IH}$, $CS = V_{IL}$, $OE = V_{IL}$)



Read Timing Waveform (3) ($WE = V_{IH}$, $CS = V_{IL}$, $OE = V_{IL}$)*²

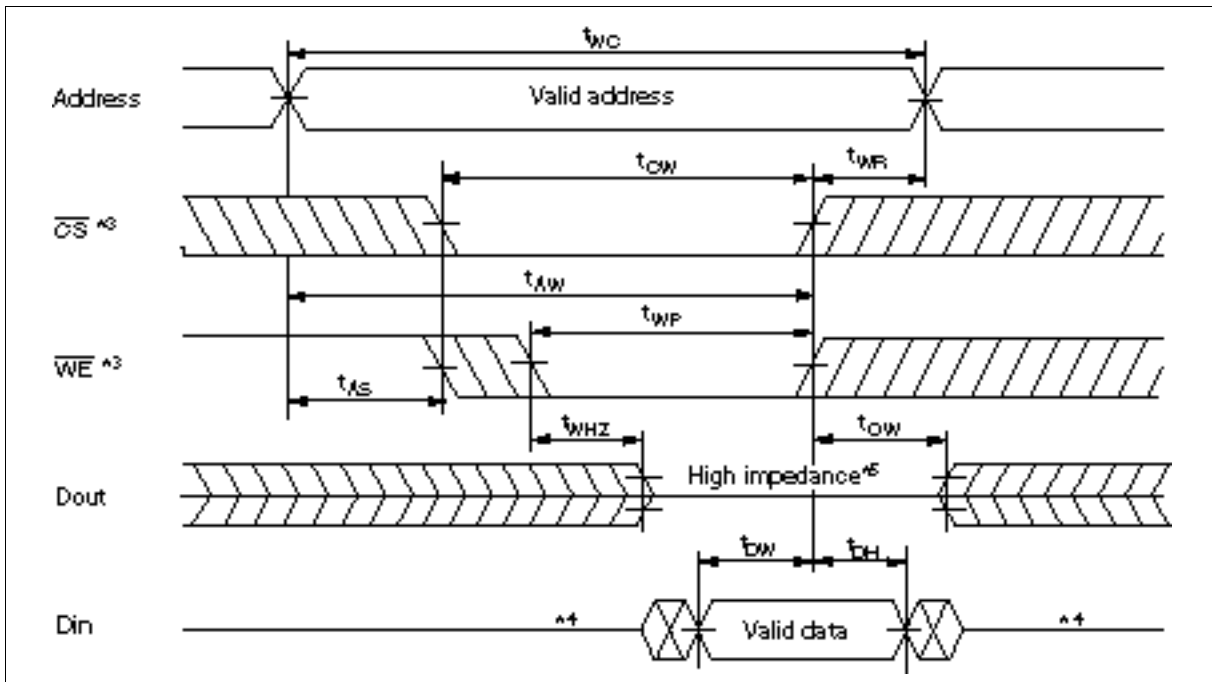


Write Timing Waveform (1) (WE Controlled)



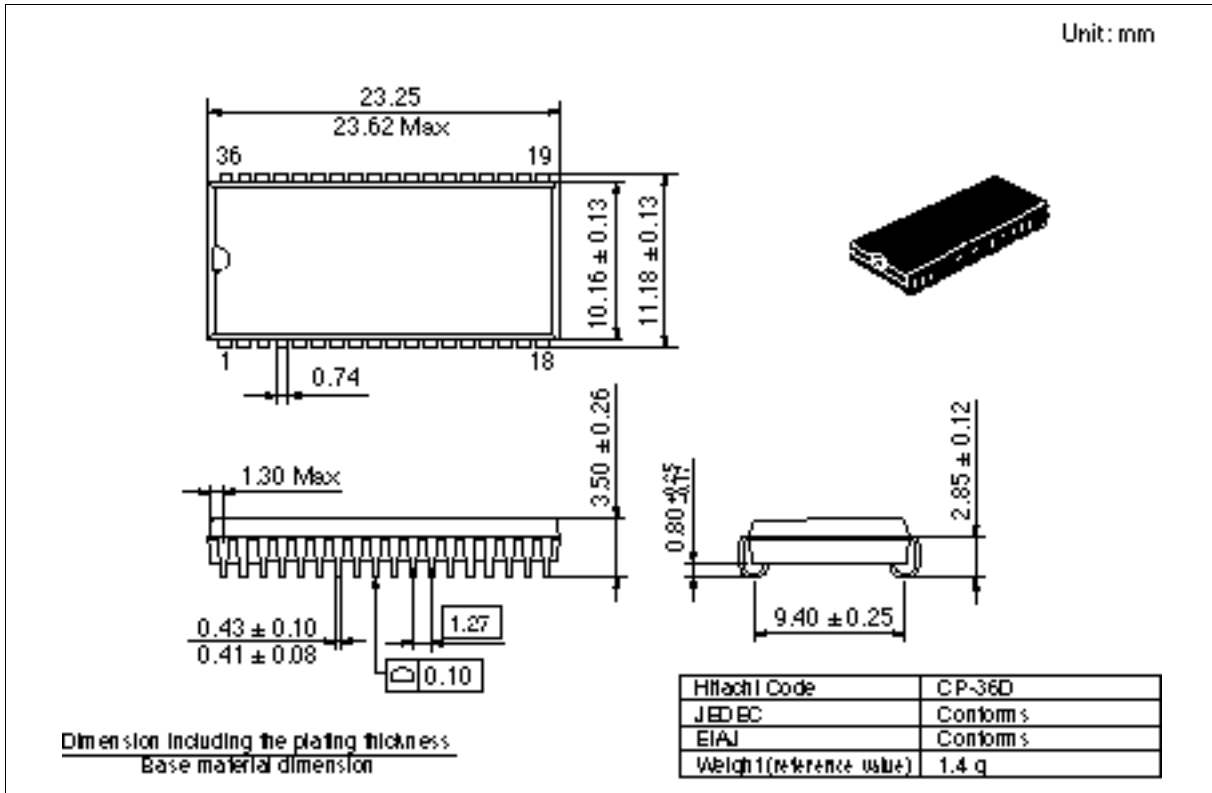
HM628511HI Series

Write Timing Waveform (2) (CS Controlled)



Package Dimensions

HM628511HJPI Series (CP-36D)



HM628511HI Series

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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Apr. 15, 1999	Initial issue		
