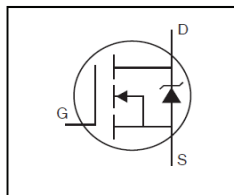


Features

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to T_{jmax}
- Lead-Free, RoHS Compliant
- Automotive Qualified *

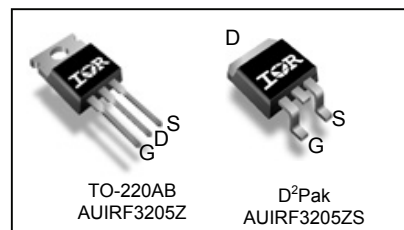


HEXFET® Power MOSFET

V_{DS}	55V
$R_{DS(on)}$ max.	6.5mΩ
I_D (Silicon Limited)	110A
I_D (Package Limited)	75A

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRF3205Z	TO-220	Tube	50	AUIRF3205Z
AUIRF3205ZS	D²-Pak	Tube	50	AUIRF3205ZS
		Tape and Reel Left	800	AUIRF3205ZSTRL

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	110	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	78	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Package Limited)	75	
I_{DM}	Pulsed Drain Current ①	440	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	170	W
	Linear Derating Factor	1.1	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②	180	mJ
$E_{AS} \text{ (tested)}$	Single Pulse Avalanche Energy Tested Value ⑥	250	
I_{AR}	Avalanche Current ①	See Fig.15,16, 12a, 12b	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw ⑦	10 lbf•in (1.1N•m)	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	—	0.90	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ⑦	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient ⑦	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ⑧	—	40	

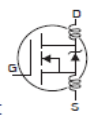
HEXFET® is a registered trademark of Infineon.

*Qualification standards can be found at www.infineon.com

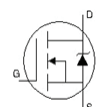
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	55	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.051	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	4.9	6.5	mΩ	V _{GS} = 10V, I _D = 66A ③
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Trans conductance	71	—	—	S	V _{DS} = 25V, I _D = 66A
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 55V, V _{GS} = 0V
		—	—	250		V _{DS} = 55V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V _{GS} = -20V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

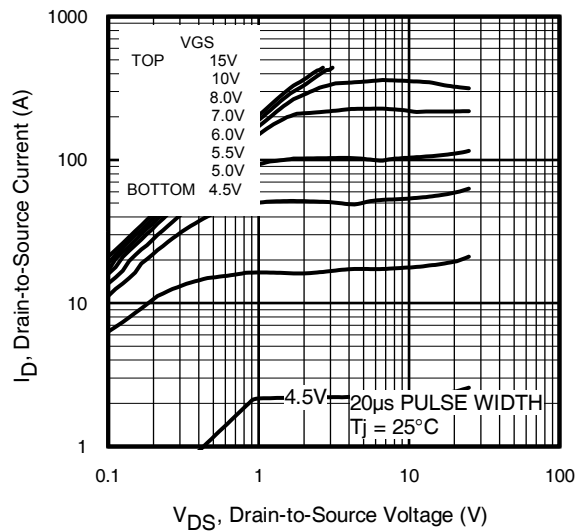
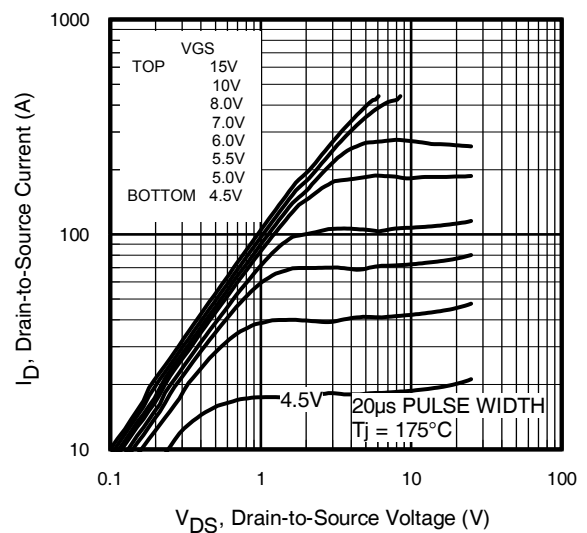
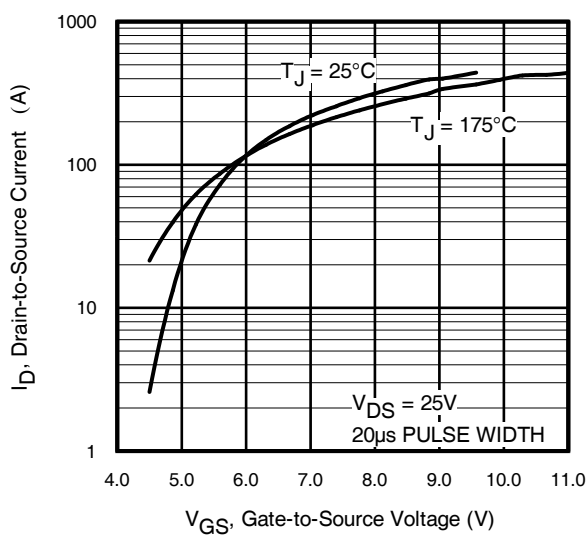
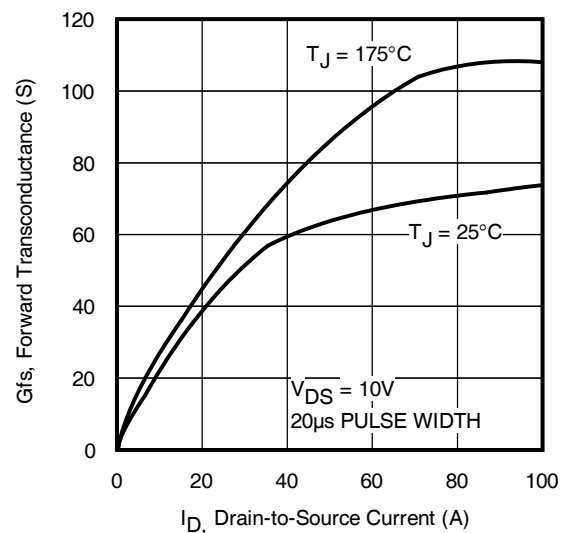
Q _g	Total Gate Charge	—	76	110	nC	I _D = 66A
Q _{gs}	Gate-to-Source Charge	—	21	—		V _{DS} = 44V
Q _{gd}	Gate-to-Drain Charge	—	30	—		V _{GS} = 10V ③
t _{d(on)}	Turn-On Delay Time	—	18	—	ns	V _{DD} = 28V
t _r	Rise Time	—	95	—		I _D = 66A
t _{d(off)}	Turn-Off Delay Time	—	45	—		R _G = 6.8Ω,
t _f	Fall Time	—	67	—		V _{GS} = 10V ③
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact: 
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	3450	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	550	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	310	—		f = 1.0MHz
C _{oss}	Output Capacitance	—	1940	—		V _{GS} = 0V, V _{DS} = 1.0V f = 1.0MHz
C _{oss}	Output Capacitance	—	430	—		V _{GS} = 0V, V _{DS} = 44V f = 1.0MHz
C _{oss eff.}	Effective Output Capacitance	—	640	—		V _{GS} = 0V, V _{DS} = 0V to 44V ④

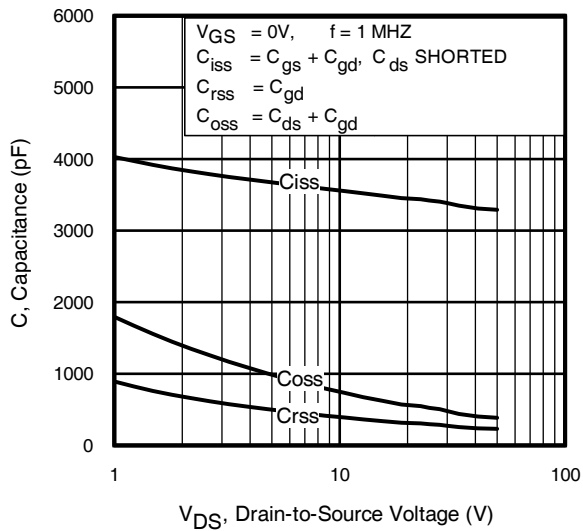
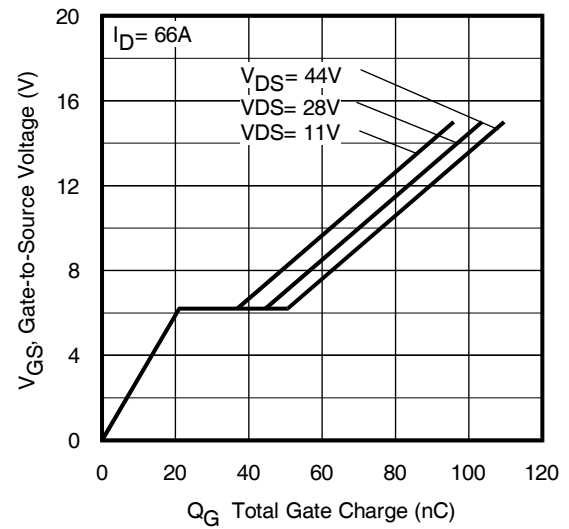
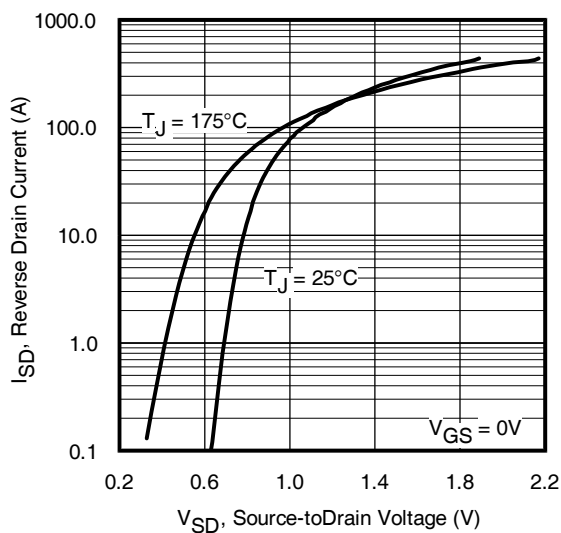
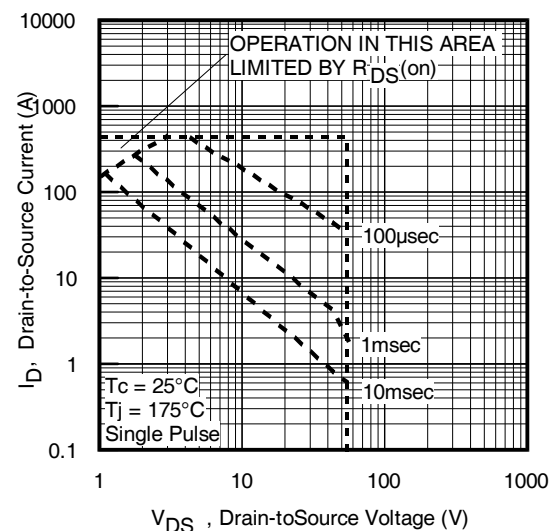
Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	75	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	440		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 66A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	—	28	42	ns	T _J = 25°C, I _F = 66A, V _{DD} = 25V
Q _{rr}	Reverse Recovery Charge	—	25	38	nC	di/dt = 100A/μs ③
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig.11)
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.08mH, R_G = 25Ω, I_{AS} = 66A, V_{GS} = 10V. Part not recommended for use above this value.
- ③ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.
- ④ C_{oss eff.} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑤ Limited by T_{Jmax}, see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population, starting T_J = 25°C, L = 0.08mH, R_G = 25Ω, I_{AS} = 66A, V_{GS} = 10V.
- ⑦ This is only applied to TO-220AB package.
- ⑧ This is applied to D² Pak, When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
- ⑨ R_θ is measured at T_J of approximately 90°C


Fig. 1 Typical Output Characteristics

Fig. 2 Typical Output Characteristics

Fig. 3 Typical Transfer Characteristics

Fig. 4 Typical Forward Trans conductance vs. Drain Current


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 7 Typical Source-to-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

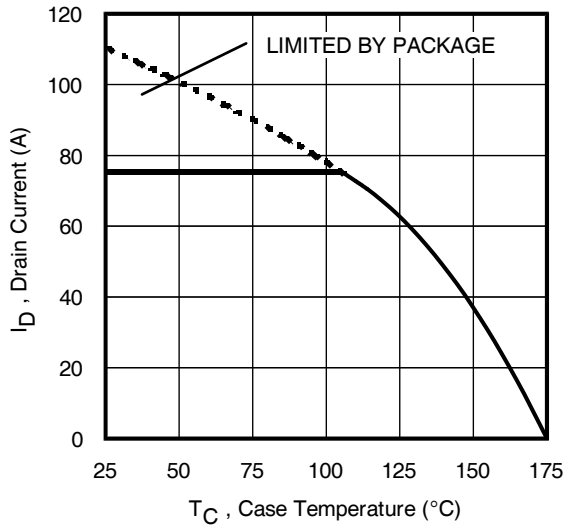


Fig 9. Maximum Drain Current vs. Case Temperature

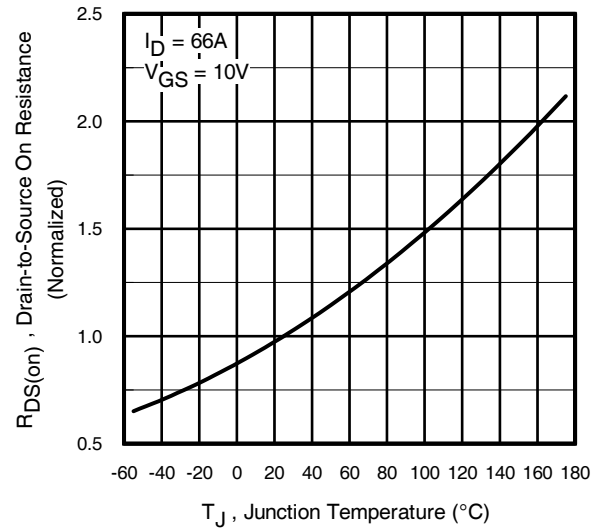


Fig 10. Normalized On-Resistance vs. Temperature

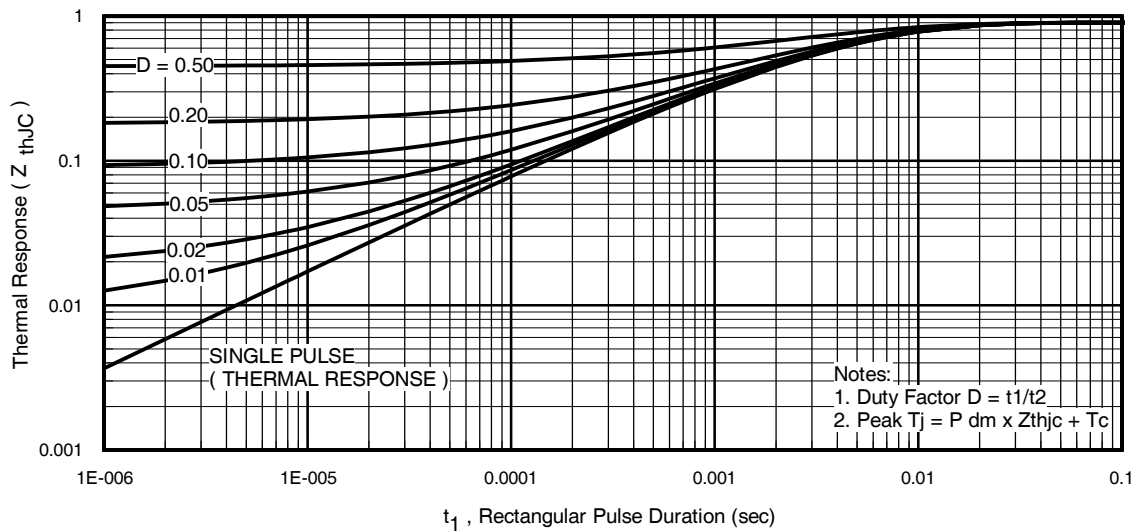
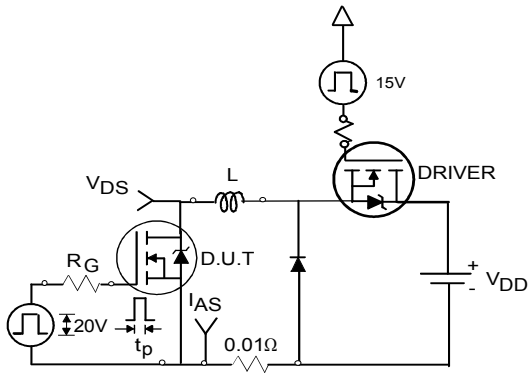
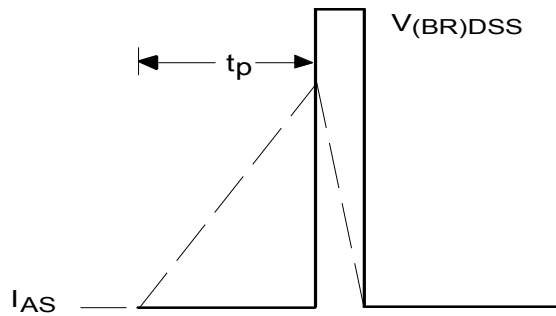
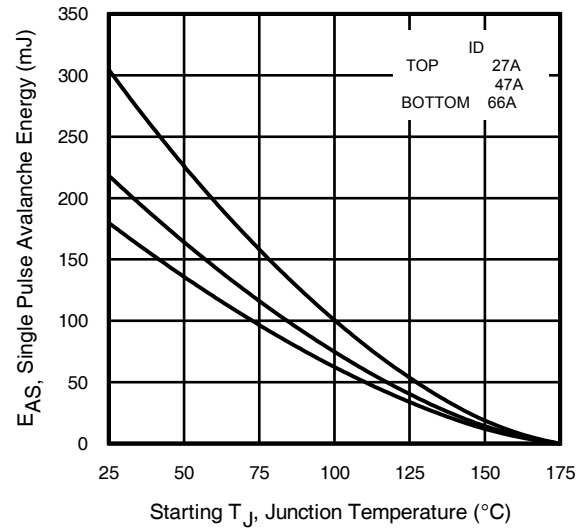
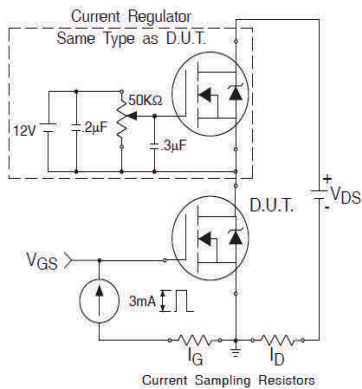
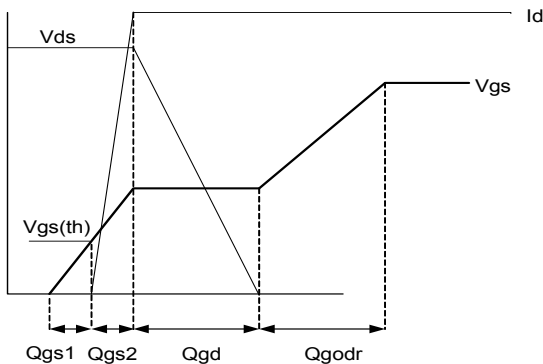
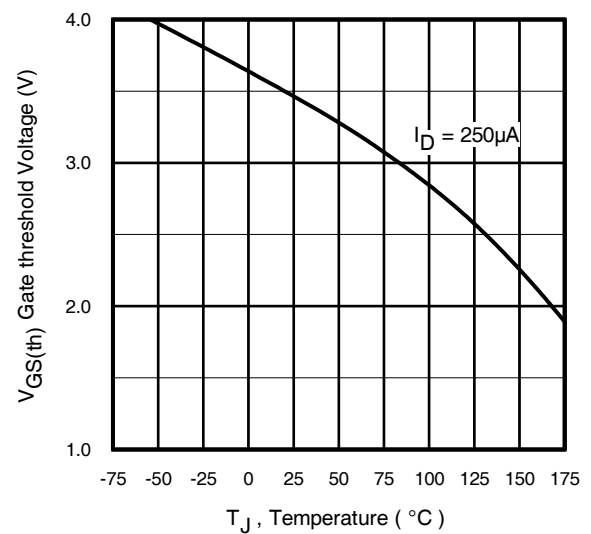


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig 12a. Unclamped Inductive Test Circuit

Fig 12b. Unclamped Inductive Waveforms

Fig 12c. Maximum Avalanche Energy vs. Drain Current

Fig 13a. Gate Charge Test Circuit

Fig 13b. Gate Charge Waveform

Fig 14. Threshold Voltage vs. Temperature

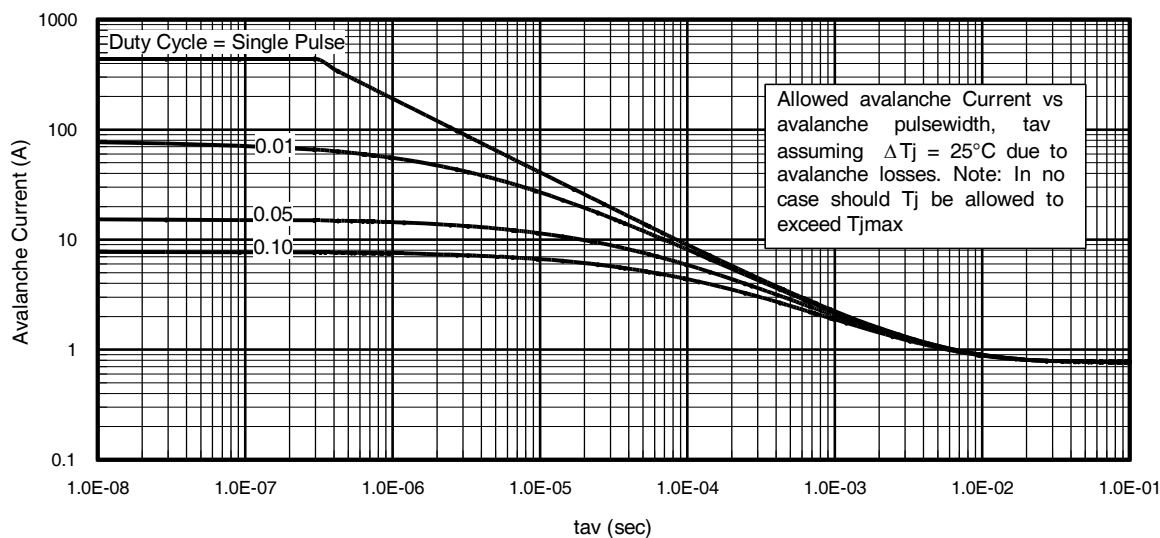


Fig 15. Avalanche Current vs. Pulse width

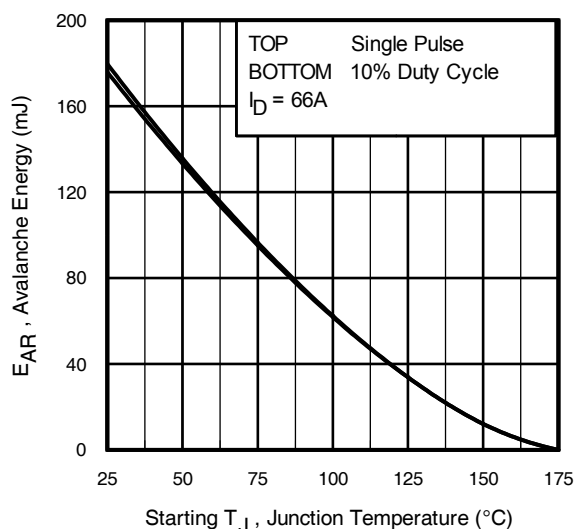


Fig 16. Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.infineon.com)**

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

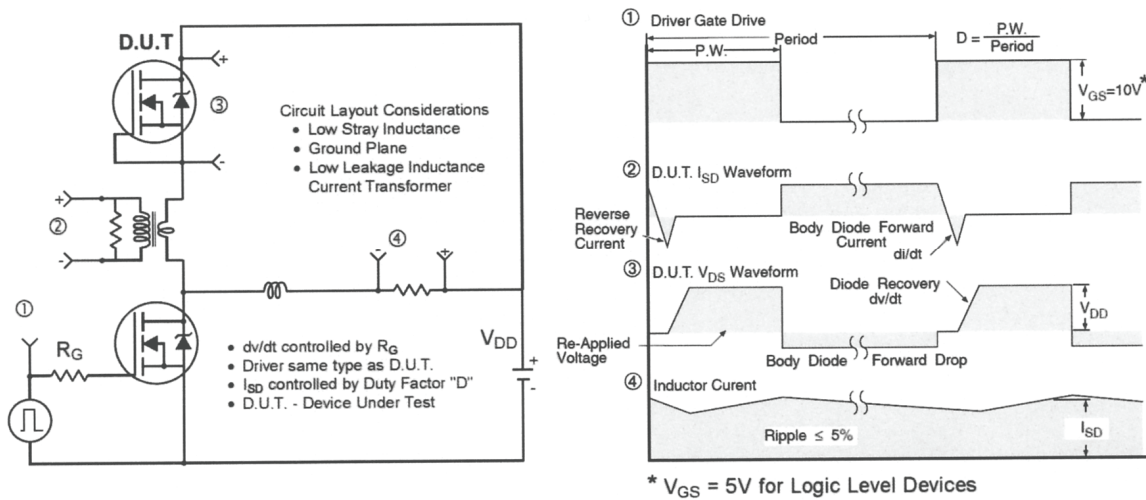


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

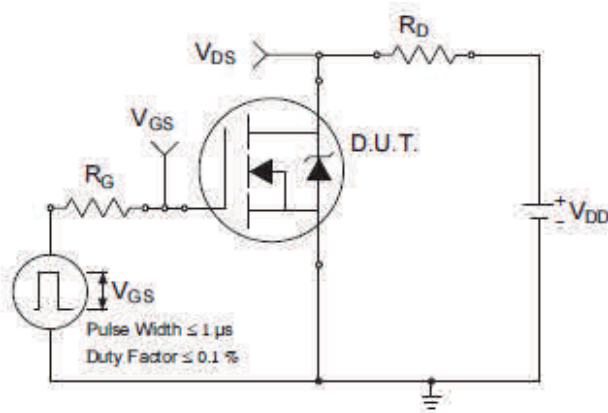


Fig 18a. Switching Time Test Circuit

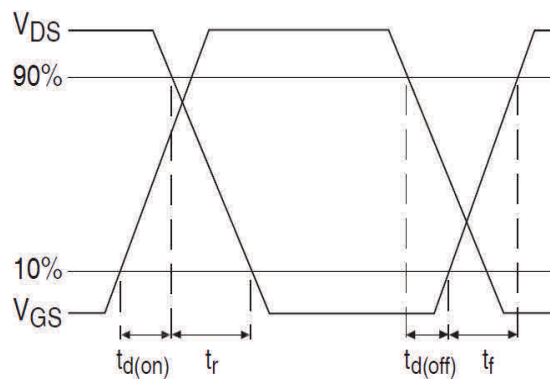
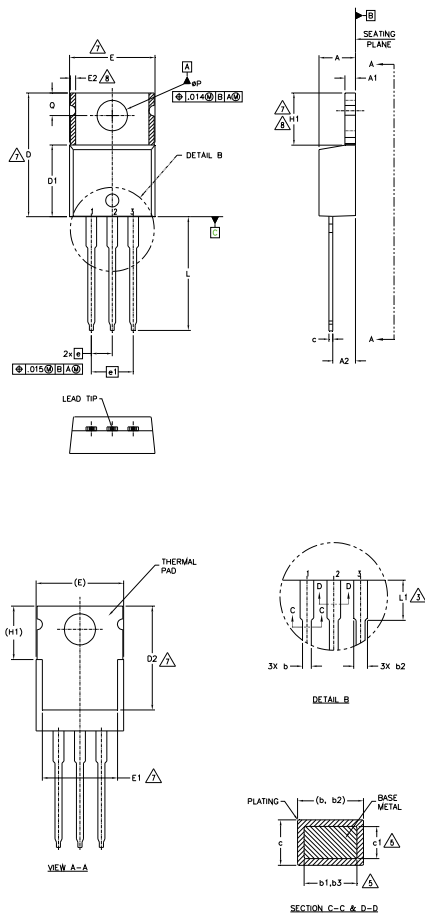


Fig 18b. Switching Time Waveforms

TO-220AB Package Outline (Dimensions are shown in millimeters (inches))

NOTES:

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	3.56	4.83	.140	.190	5	
A1	1.14	1.40	.045	.055		
A2	2.03	2.92	.080	.115		
b	0.38	1.01	.015	.040		
b1	0.38	0.97	.015	.038		
b2	1.14	1.78	.045	.070	5	
b3	1.14	1.73	.045	.068		
c	0.36	0.61	.014	.024		
c1	0.36	0.56	.014	.022	5	
D	14.22	16.51	.560	.650	4	
D1	8.38	9.02	.330	.355	7	
D2	11.68	12.88	.460	.507		
E	9.65	10.67	.380	.420		
E1	6.86	8.89	.270	.350	4,7	
E2	—	0.76	—	.030	7	
e	2.54 BSC		.100 BSC		8	
e1	5.08 BSC		.200 BSC		7,8	
H1	5.84	6.86	.230	.270		
L	12.70	14.73	.500	.580		
L1	3.56	4.06	.140	.160		3
øP	3.54	4.08	.139	.161		
Q	2.54	3.42	.100	.135		

LEAD ASSIGNMENTS
HEXFET

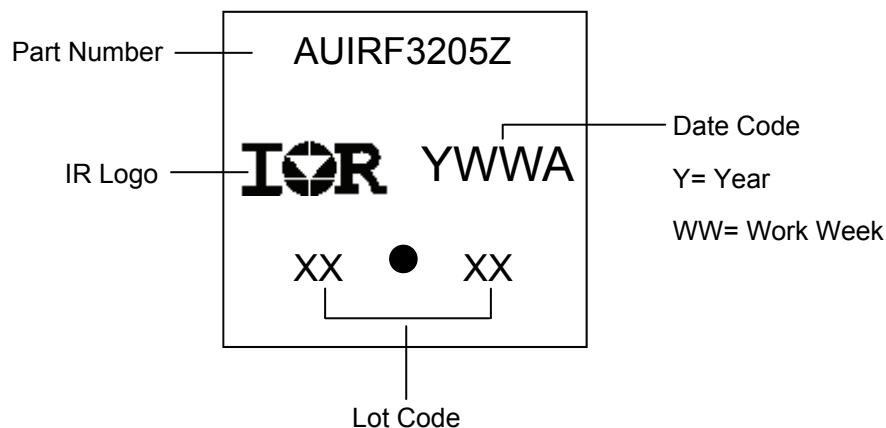
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

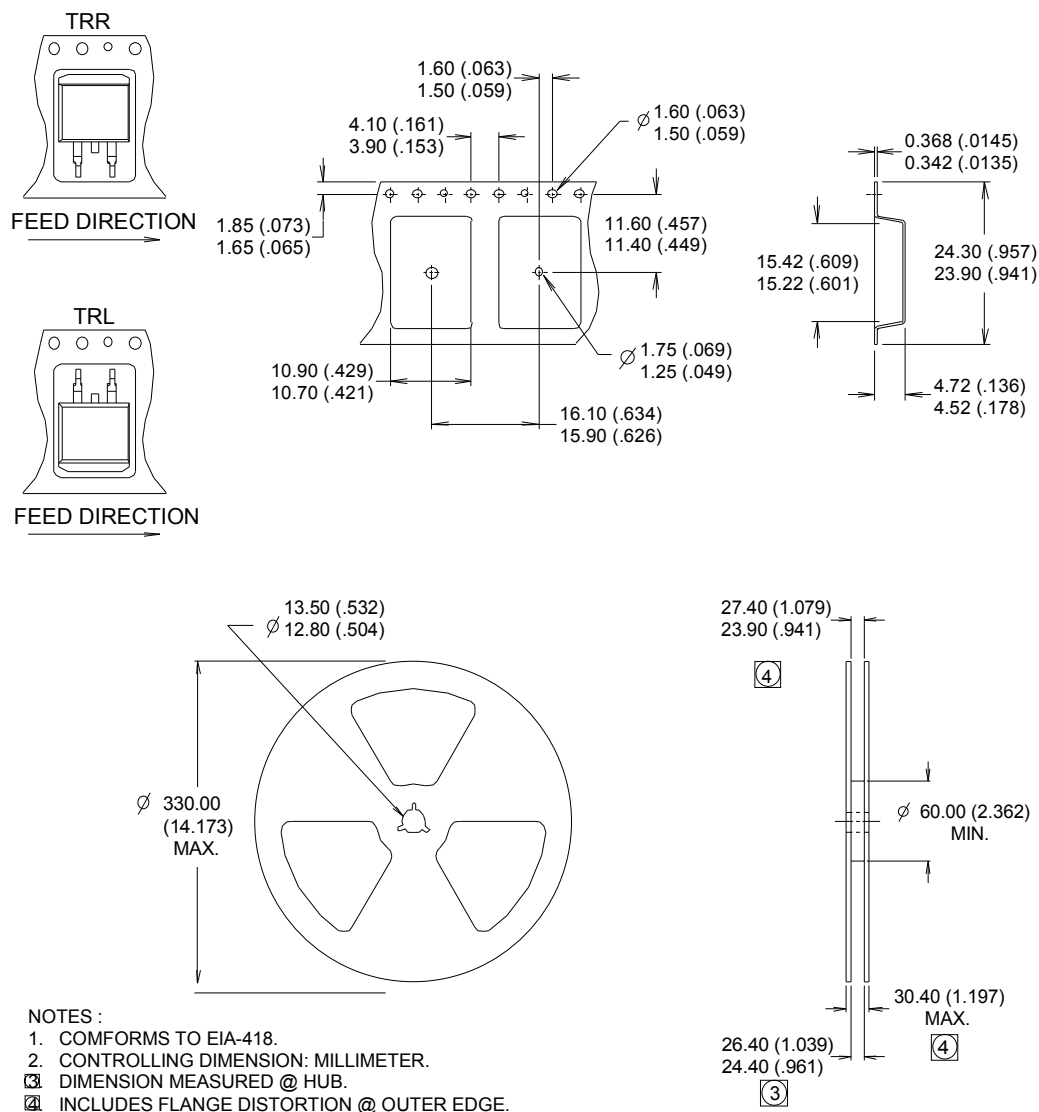
DIODES

- 1.- ANODE
- 2.- CATHODE
- 3.- ANODE

TO-220AB Part Marking Information


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

2015-11-13

D²Pak (TO-263AB) Tape & Reel Information (Dimensions are shown in millimeters (inches))


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		TO-220 Pak	N/A
		D ² -Pak	MSL1
ESD	Machine Model	Class M4 (+/- 425V) [†] AEC-Q101-002	
	Human Body Model	Class H1C (+/- 2000V) [†] AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 1125V) [†] AEC-Q101-005	
RoHS Compliant		Yes	

† Highest passing voltage.

Revision History

Date	Comments
11/13/2015	- Updated datasheet with corporate template - Corrected ordering table on page 1.

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