



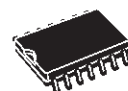
74LCX125

LOW VOLTAGE CMOS QUAD BUS BUFFERS (3-STATE) WITH 5V TOLERANT INPUTS AND OUTPUTS

- 5V TOLERANT INPUTS AND OUTPUTS
- HIGH SPEED:
 $t_{PD} = 6 \text{ ns (MAX.)}$ at $V_{CC} = 3V$
- POWER-DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 24 \text{ mA (MIN)}$
- PCI BUS LEVELS GUARANTEED AT 24mA
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC} \text{ (OPR)} = 2.0V \text{ to } 3.6V$ (1.5V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 125
- LATCH-UP PERFORMANCE EXCEEDS 500mA
- ESD PERFORMANCE:
 $HBM > 2000V$; $MM > 200V$

DESCRIPTION

The LCX125 is a low voltage CMOS QUAD BUS BUFFERS fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. It is ideal for low power and high



M
(Micro Package)



T
(TSSOP Package)

ORDER CODES :

74LCX125M

74LCX125T

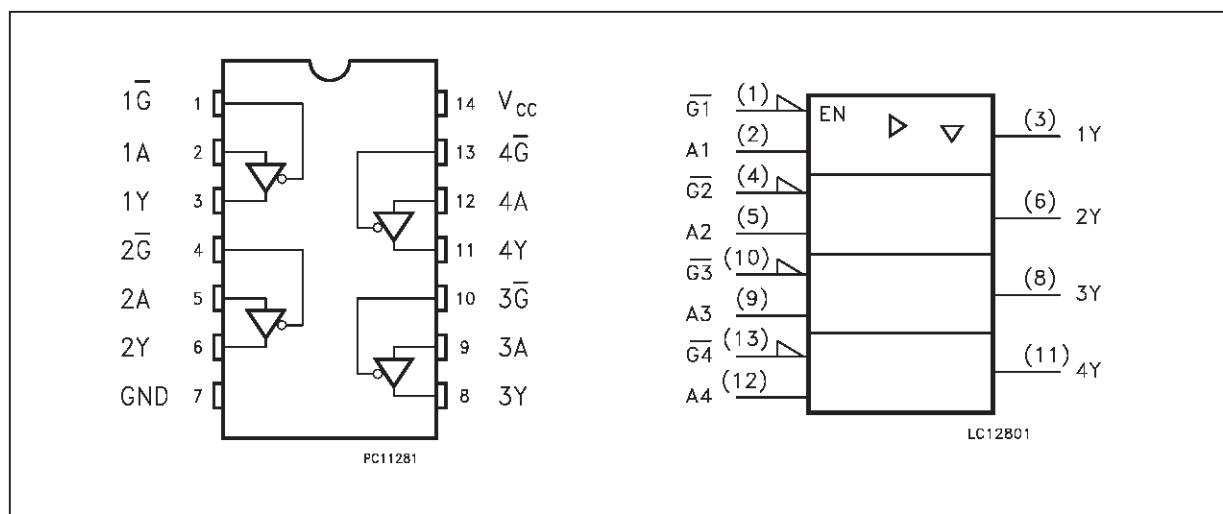
speed 3.3V applications; it can be interfaced to 5V signal environment for both inputs and outputs.

The device requires the 3-STATE control input $\overline{G}$ to be set high to place the output in to the high impedance state.

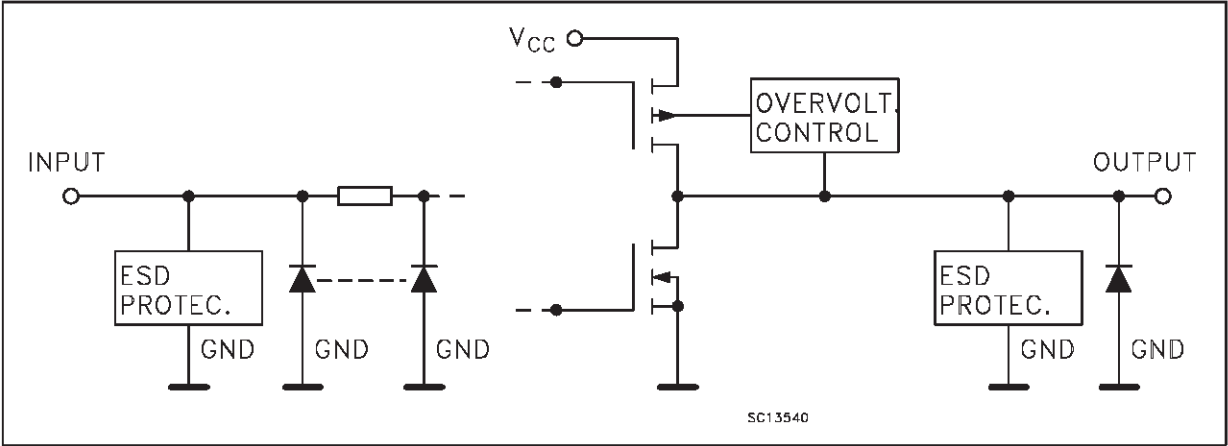
.It has same speed performance at 3.3V than 5V, AC/ACT family, combined with a lower power consumption.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	$\overline{G1}$ to $\overline{G4}$	Output Enable Inputs
2, 5, 9, 12	A1 to A4	Data Inputs
3, 6, 8, 11	Y1 to Y4	Data Outputs
7	GND	Ground (0V)
14	V _{CC}	Positive Supply Voltage

TRUTH TABLE

A	$\overline{G}$	Y
X	H	Z
L	L	L
H	L	H

X: "H" or "L"
Z: High Impedance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to + 7.0	V
V _I	DC Input Voltage	-0.5 to + 7.0	V
V _O	DC Output Voltage (OFF state)	-0.5 to + 7.0	V
V _O	DC Output Voltage (High or Low State) (note1)	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	- 50	mA
I _{OK}	DC Output Diode Current (note2)	± 50	mA
I _O	DC Output Source/Sink Current	± 50	mA
I _{CC}	DC Supply Current per Supply Pin	± 100	mA
I _{GND}	DC Ground Current per Supply Pin	± 100	mA
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

1) I_O absolute maximum rating must be observed

2) V_O < GND, V_O > V_{CC}

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	2.0 to 3.6	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage (OFF state)	0 to 5.5	V
V_O	Output Voltage (High or Low State)	0 to V_{CC}	V
I_{OH}, I_{OL}	High or Low Level Output Current ($V_{CC} = 3.0$ to $3.6V$)	± 24	mA
I_{OH}, I_{OL}	High or Low Level Output Current ($V_{CC} = 2.7$ to $3.0V$)	± 12	mA
T_{op}	Operating Temperature:	-40 to +85	°C
dt/dv	Input Transition Rise or Fall Rate ($V_{CC} = 3.0V$) (note 2)	0 to 10	ns/V

1) Truth Table guaranteed: 1.5V to 3.6V

2) V_{IN} from 0.8V to 2.0V

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value		Unit
		V _{CC} (V)		-40 to 85 °C			
				Min.	Max.		
V _{IH}	High Level Input Voltage	2.7 to 3.6		2.0		V	
V _{IL}	Low Level Input Voltage				0.8	V	
V _{OH}	High Level Output Voltage	2.7 to 3.6	V _I = V _{IH} or V _{IL}	I _O =-100 μA	V _{CC} -0.2	V	
		2.7		I _O =-12 mA	2.2		
		3.0		I _O =-18 mA	2.4		
				I _O =-24 mA	2.2		
V _{OL}	Low Level Output Voltage	2.7 to 3.6	V _I = V _{IH} or V _{IL}	I _O =100 μA		0.2	V
		2.7		I _O =12 mA		0.4	
		3.0		I _O =16 mA		0.4	
		3.0		I _O =24 mA		0.55	
I _I	Input Leakage Current	2.7 to 3.6	V _I = 0 to 5.5 V			±5	μA
I _{off}	Power Off Leakage Current	0	V _I or V _O = 5.5V			100	μA
I _{OZ}	3 State Output Leakage Current	2.7 to 3.6	V _I = V _{IH} or V _{IL} V _O = 0 to 5.5V			±5	μA
I _{CC}	Quiescent Supply Current	2.7 to 3.6	V _I = V _{CC} or GND			10	μA
			V _I or V _O = 3.6 to 5.5V			±10	
ΔI _{CC}	ICC incr. per input	2.7 to 3.6	V _{IH} = V _{CC} -0.6V			500	μA

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value			Unit
		V _{CC} (V)		T _A = 25 °C			
				Min.	Typ.	Max.	
V _{OLP}	Dynamic Low Voltage Quiet Output (note 1)	3.3	C _L = 50 pF V _{IL} = 0 V V _{IH} = 3.3V		0.8		V
V _{OLV}					-0.8		

1) Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, Input $t_r = t_f = 2.5 \text{ ns}$)

Symbol	Parameter	Test Condition		Value		Unit
		V _{CC} (V)	Waveform	-40 to 85 °C		
				Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Time	2.7	1		6.5	ns
		3.0 to 3.6		1.0	6.0	
t _{PZL} t _{PZH}	Output Enable Time to HIGH and LOW level	2.7	2	1.0	8.0	ns
		3.0 to 3.6		1.0	7.0	
t _{PLZ} t _{PHZ}	Output Disable Time from HIGH and LOW level	2.7	2	1.0	7.0	ns
		3.0 to 3.6		1.0	6.0	
t _{OSLH} t _{OSHL}	Output to Output Skew Time (note 1, 2)	3.0 to 3.6			1.0	ns

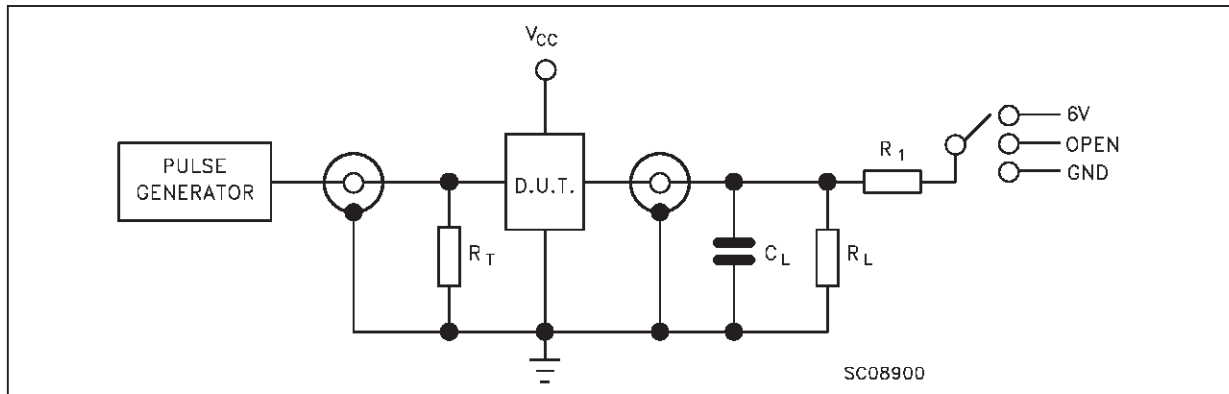
1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHM} - t_{PLHL}|$, $t_{OSHL} = |t_{PHLM} - t_{PHHL}|$)

2) Parameter guaranteed by design

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value			Unit
		V _{CC} (V)		T _A = 25 °C			
				Min.	Typ.	Max.	
C _{IN}	Input Capacitance	3.3	V _{IN} = 0 to V _{CC}		6		pF
C _{OUT}	Output Capacitance	3.3	V _{IN} = 0 to V _{CC}		10		pF
C _{PD}	Power Dissipation Capacitance (note 1)	3.3	f _{IN} = 10MHz V _{IN} = 0 or V _{CC}		40		pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC0}/4$ (per gate)

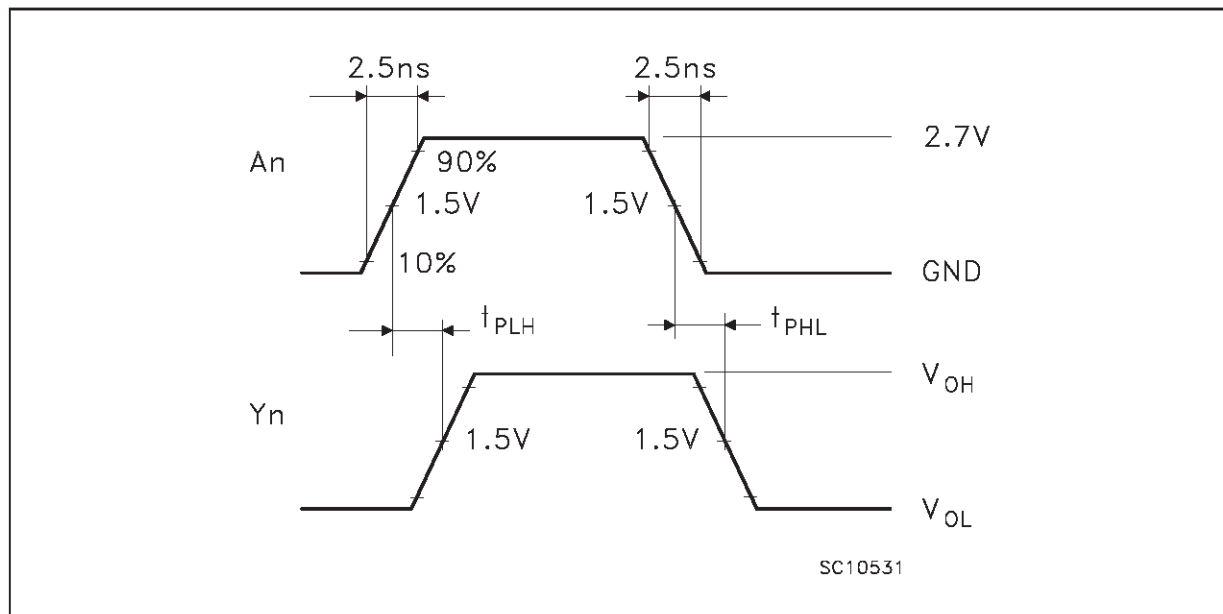
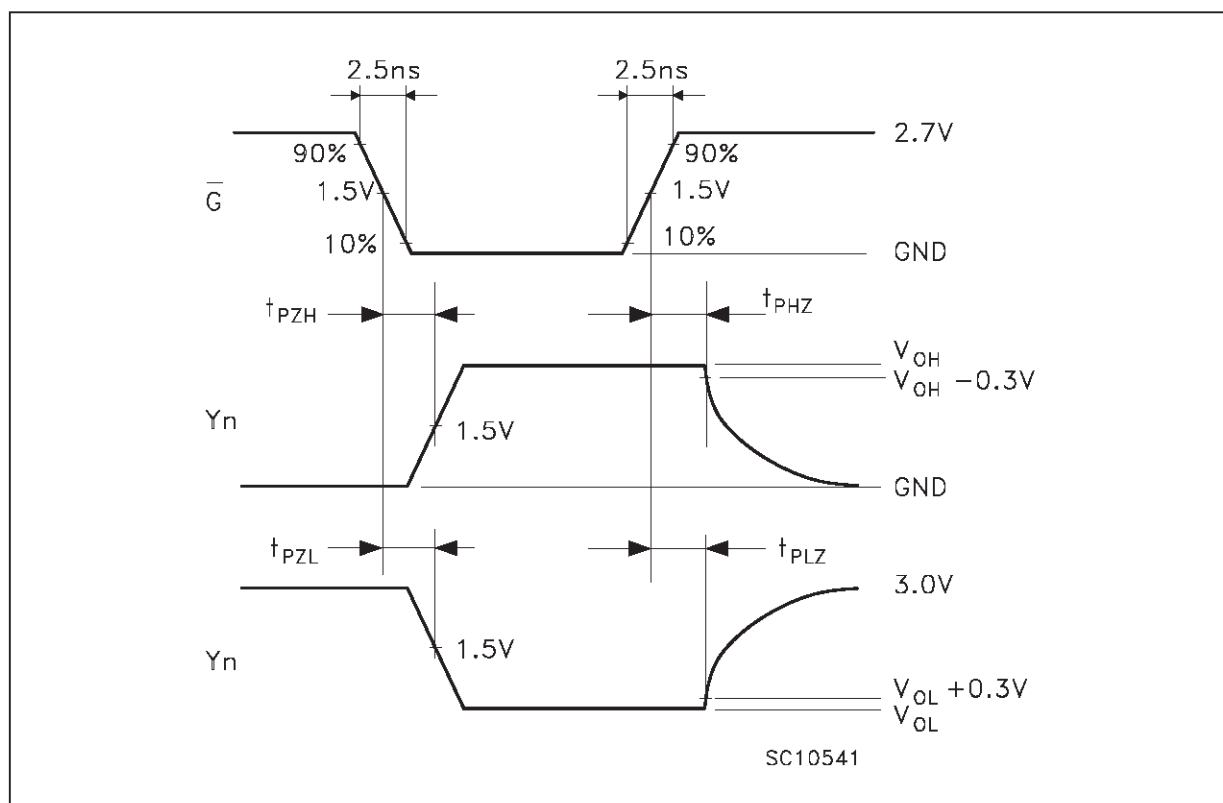
TEST CIRCUIT

TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6V
t_{PZH} , t_{PHZ}	GND

$C_L = 50 \text{ pF}$ or equivalent (includes jig and probe capacitance)

$R_L = R_1 = 500 \Omega$ or equivalent

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAYS ($f=1\text{MHz}$; 50% duty cycle)**WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME** ($f=1\text{MHz}$; 50% duty cycle)

SO-14 MECHANICAL DATA

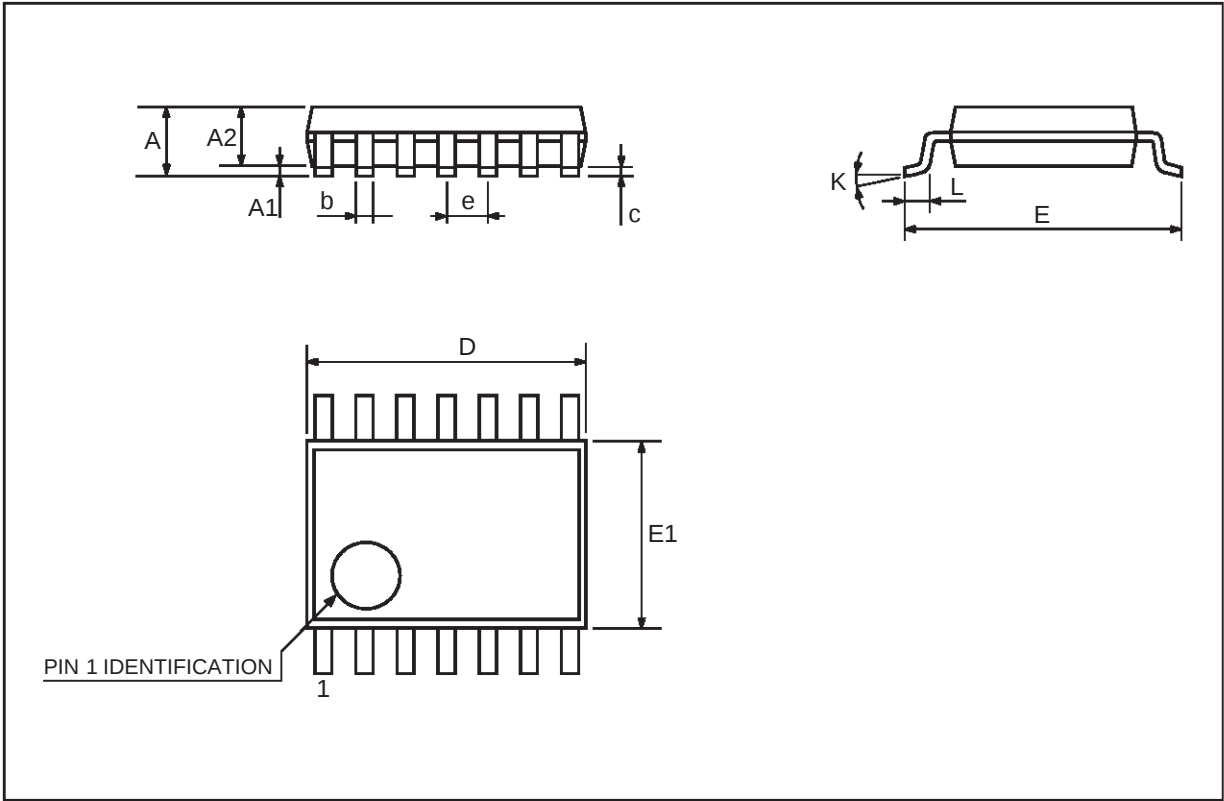
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8 (max.)					



P013G

TSSOP14 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



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